SE (comp) / sem-IV / COA / 03/12/2014

P. (1)

QP Code :12476

CBSGS

(3 Hours) **[Total Marks : 80**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **three** questions from remaining **five** questions.
(3) Assume suitable data if **required.**
(4) Draw neat diagram wherever **necessary.**

1. Solve any **four :** **2**
   (a) What are the types of pipeline hazards ?
   (b) Explain in brief memory mapped I/O.
   (c) Explain in detail cache coherence.
   (d) Draw flow chart of Booth's algorithm.
   (e) Define stored program concept and draw Von Neumann's Architecture.

2. (a) Explain in detail different types of addressing modes. **1**
   (b) Multiply $(-2)_{10}$ and $(-5)_{10}$ using Booth's Algorithm. **1**

3. (a) Explain Wilke's Engine (Hardwired Control Unit) in detail. **1**
   (b) Explain virtual memory with reference to memory hierarchy, segments and pages. **1**

4. (a) Explain features of RISC and CISC processors. **1**
   (b) Explain six stage instruction pipeline with suitable diagram. **1**

5. (a) Explain various high speed memories such as interleaved memories and caches. **1**
   (b) Explain LRU page replacement policy with suitable example. **1**

6. (a) What is Bus Arbitration ? Explain any two techniques of Bus Arbitration. **1**
   (b) Write short note (any **two**) : **1**
      (i) Nano programming
      (ii) DMA (Direct Memory Access)
      (iii) Plotter.
