15/12/14. SE-EE. Sem III (CBSGS)

QP Code: 12543

(3 Hours)	[Total Marks: 8
N.B: (1) Question No. 1 is compulsory. (2) Attempt any three questions from remaining. (3) Assume switchle data.	
 (3) Assume suitable data wherever necessary. (a) Prove A. (A+B) = A, stating all the rules used. (b) Explain two opamp parameters. (c) Convert following:— (i) (101101)₂ to gray code (ii) (247.6875)₁₀ to octal. 	4 4 4
(d) Design full adder using NAND gate. (e) Explain hazards in combinational logic circuits.	4
 (a) Explain 555 timer working as monostable multivibrator. (b) Explain an instrumentation amplifier and mention to applications (a) Design mod-12 asynchronous counter using JK flip flop. (b) Minimize the second counter using JK flip flop. 	10 10
(b) Minimize the expression using K map and implement using gates. $F = \sum m(0, 5, 9, 12, 13, 14, 15) + d(1, 2, 3, 4)$	10 10
4. (a) Explain successive approximation type ADC.(b) Explain noise margin and fan our.	10 10
 (a) Implement following expression F(A, B, C) = ∑m(0, 2, 5, 6, 7) us (i) 8:1 Mux (one) (ii) 4:1 Mux (two) (b) Explain high pass filter along with its frequency response. 	
6. (a) Explain carry look ahead adder.	10
(b) Convert JK to SR flip flop.(c) Write short note on interfacing of logic families.	10 5 5

GN-Con: 11495-14.