Analysis and Implementation of H-Bridge Multilevel Inverter

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Declaration

We, hereby declare that the dissertation titled "**Analysis and Implementation of H-Bridge Multilevel Inverter**" submitted herein for the award of Degree in **Bachelor of Engineering** has been carried out by us in the*Anjuman-I-Islam's Kalsekar Technical Campus*, panvel. The work is original and has not been submitted earlier as a whole or in part for the award of the degree / diploma at this or any other Institution / University.

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CERTIFICATE

*This is to certify that the dissertation entitled "**Analysis and Implementation of H-Bridge MultilevelInverter**" being submitted by **BE STUDENTS** (stated above)in partial fulfillment of requirementsfor the award of degree of **Bachelor of Engineering**in **Electrical Engineering**is a record of the students own work carried out by them under my supervision and guidance at the Department of Electrical Engineering **Anjuman-I-Islam's Kalsekar Technical Campus,panvel**.The work is comprehensive, complete and fit for evaluation.*

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ABSTRACT

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as inverter. The voltage source inverters produce an output voltage or a current with levels either 0 or positive or negativeV_{dc}. They are known as two-level inverters. Multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. Multilevel inverter has advantage like minimum harmonic distortion.

Multi-level inverters are emerging as the new breed of power converter options for high power applications. They typically synthesize the stair –case voltage waveform (from several dc sources) which has reduced harmonic content.

In this project work, voltage THD analysis of H-bridge multilevel inverter and hardware model of Three-level single phase cascade H-Bridge inverter has been developed using MOSFETS/IGBTS. Gating signals for these MOSFETS/IGBTS have been generated by designing comparators. In order to maintain the different voltage levels at appropriate intervals, the conduction time intervals of MOSFETS/IGBTS have been maintained by controlling the pulse width of gating pulses (by varying the reference signals magnitude of the comparator). The results of hardware are compared with simulation results. Simulation models (designed in SIMULINK) have been developed up to five levels and THD in all the cases have been identified.

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LIST OF FIGURES

LIST OF TABLES

NOMENCLATURE

MLI	Multilevel Inverter
V_{dc}	DC Link Voltage
V_C	Voltage across Capacitor
V_o	Output Voltage
NPC	Neutral Point Clamped
THD	Total Harmonic Distortion

Index

CHAPTER 1

INTRODUCTION

Chapter 1

INTRODUCTION

1.1 INTRODUCTION

The power electronics device which converts DC power to AC power at required output voltage and frequency level is known as an inverter. Two categories into which inverters can be broadly classified are two level inverters and multilevel inverters. One advantage that multilevel inverters have compared to two level inverters is minimum harmonic distortion. Multilevel converters have seen an increasing popularity in the last years for medium- and high-voltage applications.

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources.

The concept of multilevel converters has been introduced since 1975. The term multilevel began with the three-level converter. Subsequently, several multilevel converter topologies have been developed. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform. Capacitors, batteries, and renewable energy voltage sources can be used as the multiple dc voltage sources. The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected.

1.2 THESIS OBJECTIVE AND ACHIEVEMENTS

This thesis deals with the superior performance of the multilevel inverter by using SPWM technique

1. Study of multilevel inverters and its basic topologies.
2. Collecting information about simulation work and requisite theory / formulae.
3. Simulation of the multilevel inverter, study of the obtained simulated results.
4. Voltage THD Analysis of three level inverter and five level inverter.
5. Making hardware of single leg of three level inverter..

1.3 STRUCTURE OF THESIS

This thesis is organized into eight Chapters. The structure and description of the thesis can be described as follows.

1. Chapter 1 provides a brief introduction, overview behind the thesis, the thesis objectives and achievements and organization of the thesis.
2. Chapter 2 provides the basic background and brief review of the working and different topologies of multilevel inverter.
3. Chapter 3 provides an overview of the multilevel inverter, its different topologies and its operating principle.
4. Chapter 4 presents the introduction of proposed PWM techniques used for multilevel inverter.
5. Thus, in Chapter 5 presents the simulation results for all three topologies.
6. Chapter 6 presents the introduction of proposed H-bridge inverter and brief explanation of working of H-bridge inverter, simulation results and Voltage THD analysis.
7. Chapter 7 provides the hardware implementation of single leg three level H-bridge inverter.
8. Chapter 8 concludes this thesis highlighting the major contributions of this research. A brief future directive based on this thesis is also include.

CHAPTER 2

LITERATURE

REVIEW

Chapter 2

LITERATURE REVIEW

1. J. Rodrıguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.-this paper has provided brief summary of multilevel inverter topologies and there control strategies. Different application using different inverter circuits were also discussed.

2. T.Prathiba , P.Renuga " A comparative study of Total Harmonic Distortion in Multilevel inverter topologies in the paper " Journal of Information Engineering and Applications ISSN 2224-5782 (print) ISSN 2225-0506 (online)Volume- 2, No.3, 2012,pp.26-36.-This paper proposes the three multilevel topologies (3LNPC, 3L FC-VSI, and the 5-level CHB) and they cover different needs for different type of applications. The multi carrier PWM modulation control techniques are introduced in these topologies to get reduced harmonics at the output voltage THD and to improve the efficiency of the inverter. Thus the proposed inverter topologies with the proposed modulation method control techniques are validated through the detailed simulation analysis along with the conventional two level voltage source inverter, and it was shown that the output voltage levels are increased in the multi-level inverters to approach near sine wave and to get the higher voltage and reduced Total Harmonic Distortion.

3. PardasaniHitendra K. Arora Kapildev N. "Simulation of Three Level Inverter Using Sinusoidal Pulse Width Modulation Technique by MATLAB," National Conference on Recent Trends in Engineering & Technology 13-14 May 2011- This paper has included about Three Level Inverter and Neutral Point Clamped Three Level Inverter which is used to convert uncontrolled D.C. in to controlled A.C. using Sinusoidal Pulse Width Modulation (SPWM) technique which is widely used in industrial applications like speed control of Induction Motor, Brushless D.C. Motor etc.

4. Kapil Jain, PradyumnChaturvedi , " MATLAB -based Simulation & Analysis of Three -level SPWM Inverter" International Journal of Soft Computing and Engineering (IJSCE) ISSN: 2231-2307, Volume-2, Issue-1, March 2012,pp. 56-59-This paper briefly explains theory of sinusoidal pulse width modulation (SPWM) for two and three level inverter and performance of both inverters was tested using RL load. It has shown that load current for three level inverter are much more sinusoidal and improvement in the line current

waveform and decrease in the THD from two level to three level inverter and decrease in the THD as the frequency is increased.

5. R. Chibani, E.M. Berkouk and M.S. Boucherit, "Input DC Voltages of Three-level Neutral Point Clamped Voltage Source Inverter Balancing Using a New Kind of Clamping Bridge", International Journal of Computer and Electrical Engineering, Vol. 2, No. 5, October, 2010 1793-8163.pp 879-886-This technique permit an economic and simple electronic implementation, whereas in the space vector modulation control the computational burden, the complexity of the algorithms and the number of instructions are drastic especially when the number of levels of the inverter is greater than three.

6. Xiaoming Yuan, Ivo Barbi, " Soft-Switched Three-Level Capacitor Clamping Inverter with Clamping Voltage Stabilization," IEEE Transactions on Industry Electronics, vol. 36, no. 4,July/Aug. 2002, pp. 1165-1173-This paper proposes a zero-voltage-switching scheme for the three-level capacitor clamping inverter. The proposed small-rating auxiliary circuit ensures not only zero-voltage switching of the main switches and zero-current switching of the auxiliary switches, but the clamping capacitor voltage of the inverter is also stabilized.

7. Yang Han, Lin Xu, Gang Yao, Li-Dan Zhou, Mansoor, Chen Chen, "Operation Principles and Control Strategies of Cascaded H-bridge Multilevel Active Power Filter," ISSN 1392 – 1215 2009. No. 3(91) ELECTRONICS AND ELECTRICAL ENGINEERING,pp.71-76- This paper reports the operation principles of the cascaded H-bridge multilevel active power filters (APFs). The phase shift cascaded PWM (PSCPMW) is adopted to generate the gating signals for each H-bridge module.

8. SubhransuSekhar Dash, P.Palanivel and S.Premalatha, "Performance Analysis of Multilevel Inverters Using Variable Switching Frequency Carrier Based PWM Techniques" International Conference on Renewable Energies and Power Quality (ICREPQ'12) Santiago de Compostela (Spain), 28th to 30th March, 2012-In this paper, various pulse width modulation techniques are proposed, which can minimize total harmonic distortion and enhance the output voltages in five-level inverters.Two methodologies adopting phasedisposition and phase opposition disposition pulse widthmodulation concepts are proposed in this paper.

9. Giuseppe Carrara, Simone Gardella, Mario Marchesoni, RaffaeleSalutari, and Giuseppe Sciutto, "A New Multilevel PWM Method: A Theoretical Analysis", IEEE Trans. On Power Electronics, Vol. 7, No. 3, pp. 497-505, July 1992. Authors focused on generalization of the PWM "subharmonic" method to control single-phase or three phase multilevel voltage source inverters (VSI).

10. B. Shanthi and S.P. Natarajan, “Comparative Study on Unipolar Multicarrier PWM Strategies for Five Level Flying Capacitor Inverter”, International Conference on “Control, Automation, Communication and Energy Conservation, pp. 1-7, Jun 2009. -investigated on comparison of unipolar multicarrier Pulse Width Modulation (PWM) techniques for the Flying Capacitor Multi Level Inverter (FCMLI). This literature presents the different types of unipolar PWM strategies for the chosen inverter.

CHAPTER 3

OVERVIEW OF A MULTILEVEL INVERTER

Chapter 3

OVERVIEW OF A MULTILEVEL INVERTER

3.1 MULTILEVEL INVERTER

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The commutation of the switches permits the addition of the capacitor voltages that reach high voltage at the output.Fig.3.1 explains the functional diagram of multilevel inverters.

In Fig.3.1 (a) the output $V_o$can take two possible values i.e. 0 and V_C. In Fig.3.1 (b) the output V_o can take three possible values i.e. 0, V_c and $2V_c$. In Fig.3.1(c) the output V_o can take four possible values i.e. 0, V_c, $2V_c$ and $3V_c$. It can be extended further. The number of possible outputs represents the level of the inverter. In this thesis, at several places the term 'n-level' is used in place of 'multilevel'. The values of n in Fig.3.1 (a), Fig.3.1 (b) and Fig.3.1(c) are 2, 3 and 4 respectively. Here, n = 2 represents conventional two-level inverter whereas n > 2 represent multilevel inverters. With the increase in n the output has more number of steps leading to sinusoidal waveform. This is the basic idea behind various topologies of multilevel inverters.

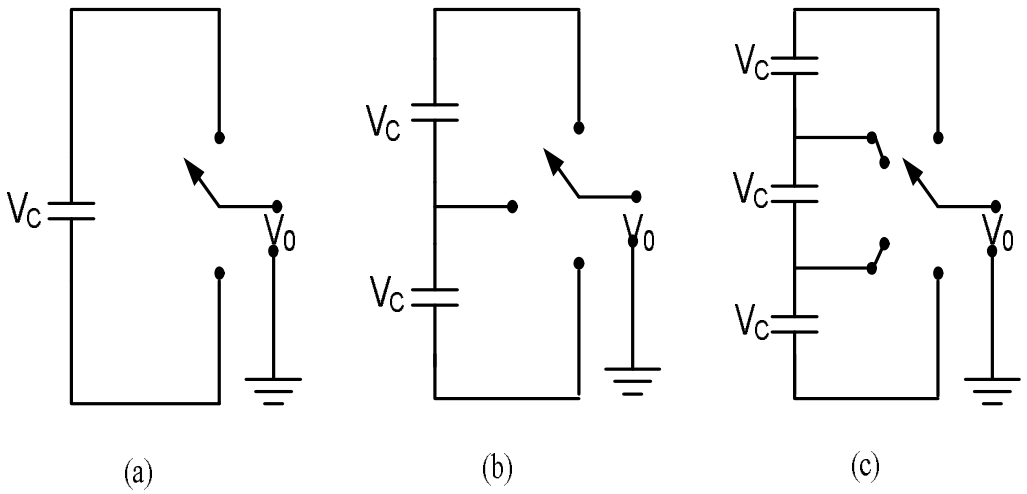


Figure 3.1: One phase leg of an inverter with (a) two levels, (b) three levels, and (c) n levels

Advantagesof Multilevel Inverter

1. They are suitable for medium to high power applications.

2. They can generate output voltages with extremely low distortion and dv/dt.

3. They draw input current with very low distortion.

4. They generate smaller common-mode (CM) voltage, thus reducing the stress of the motor bearing. In addition, we can use sophisticated modulation methods, then CM voltage can be eliminated.

Disadvantagesof Multilevel Inverter

1. Require a large number of power semiconductor switches.

2. Another disadvantage of multilevel converters concerns the idea of controlling the switches. The increased number of switches will result in more complicated control.

3.2 TOPOLOGIES OF MULTILEVEL INVERTER

The Multilevel inverter are broadly classified into three types of topologies:

1. Neutral Point Clamped (Diode Clamped)
2. Capacitor Clamped (Flying Capacitors)
3. Cascaded H-Bridge

3.2.1 Neutral Point Clamped Topology

The neutral point clamped (NPC) topology is also known as diode clamped topology. Theoretically, for a NPC inverter n can take any integer value. The main advantage of the NPC topology is that it requires only one DC source similar to two-level inverter, and gives better performance .However, the number of power components is more than two-level inverter. Fig. 3.2 shows 3-level NPC inverter topology. It consists of two DC-link capacitors, twelve controllable power semiconductor switches with freewheeling diodes and six clamping diodes.

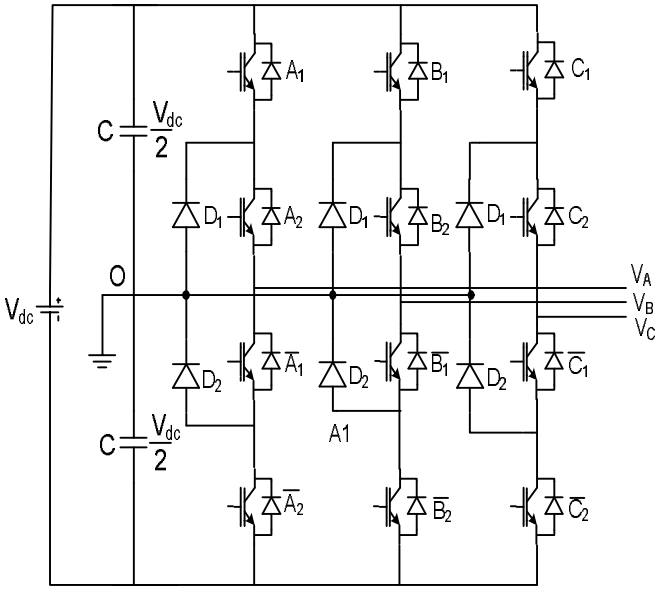


Figure 3.2: Three-Level Neutral Point Clamped Topology

The minimum numbers of components for other levels of NPC topology are given in table [3.1]. In this table, the term 'Capacitor' signifies the capacitors in DC-link, the term 'Switches' signifies controllable power semiconductor switches with freewheeling diodes and the term Diodes' signifies the clamping diodes.

Table 3.1: Number of Components in NPC Topology

Level	Capacitor	Switches	Diodes
3	**2**	**12**	**6**
4	**3**	**18**	**9**
5	**4**	**24**	**12**
.	.	.	.
.	.	.	.
n	(n-1)	6(n-1)	3(n-1)

Principle of Operation of one Leg

Table 3.1: Switching state in NPC Topology

SWITCHING STATE	**A_1**	**A_2**	**V_{DC}**
1	**ON**	**ON**	$+\frac{V_{DC}}{2}$
0	**ON**	**OFF**	**0**
-1	**OFF**	**OFF**	$-\frac{V_{DC}}{2}$

When n>3, different diodes have to support different voltage levels,. The other main disadvantage of this topology is the voltage fluctuation of its DC-link capacitors. For example, ideally the voltage across the two DC-link capacitors should be Vdc/2 as shown in Fig.3.2. However, in practice due to current flowing through the point O in Fig.3.2, the voltage across two capacitors is not the same leading to some undesirable effects. This problem is commonly known as 'neutral point fluctuation' or 'DC-link unbalancing' problem. To summarize, with the increase in level n, not only the number of clamping diodes increase but also the problem of ensuring the DC-link balance becomes more severe. Due to these reasons, the NPC topology is mainly used for 3-level inverter.

3.2.2 Capacitor Clamped Topology

It is also known as flying capacitor topology. For this topology n can take any integer value similar to NPC topology. The voltage clamping is done by using capacitors floating with respect to the earth potential. Fig. 3.3 shows its 3-level topology. For this topology, the voltage synthesis is more flexible than the NPC topology. However, this topology also exhibits the capacitor voltage unbalancing problem. Since this topology offers more redundancy as compared to NPC topology, the capacitor voltage unbalancing can be reduced by utilizing these redundancies.

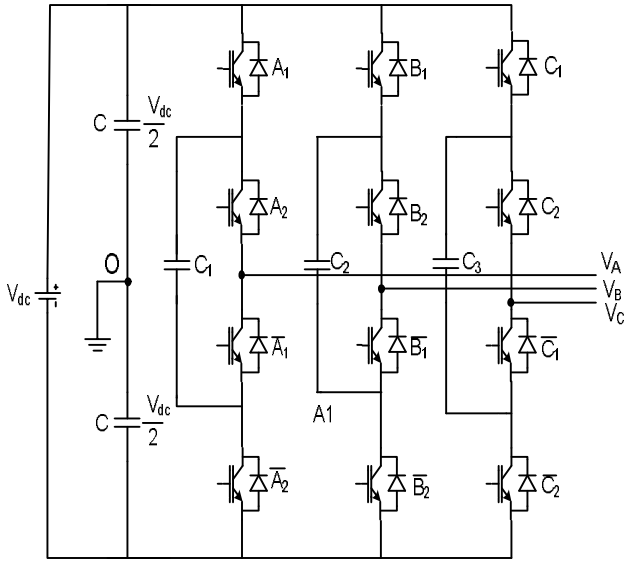


Figure 3.3: Three-Level Capacitor Clamped Topology

The main disadvantage of this topology is that it needs a large number of bulky capacitors e.g. a n-level capacitor clamped inverter needs a minimum of 3n-5 independent capacitors. The use of large number of bulky capacitors, most of which need pre-charge circuit, along with the voltage balancing problem of its capacitors inhibit the industrial use of this topology.

3.2.1. Principle of Operation of one Leg

Table 3.3: Switching state in Capacitor Clamped Topology

SWITCHING STATE	A_1	A_2	V_{DC}
1	ON	ON	$+\frac{V_{DC}}{2}$
0	ON	OFF	0
-1	OFF	OFF	$-\frac{V_{DC}}{2}$

3.2.3 Cascaded H-Bridge Topology

In this topology the H-bridges are cascaded in every phase. With the increase in H-bridges in a phase, the output voltage waveform tends to be more sinusoidal. Figure. 3.4 shows its 3-level topology. It consists of two identical H-bridges in each phase. In n-level topology, (n-1)/2 identical H-Bridges are used in every phase.

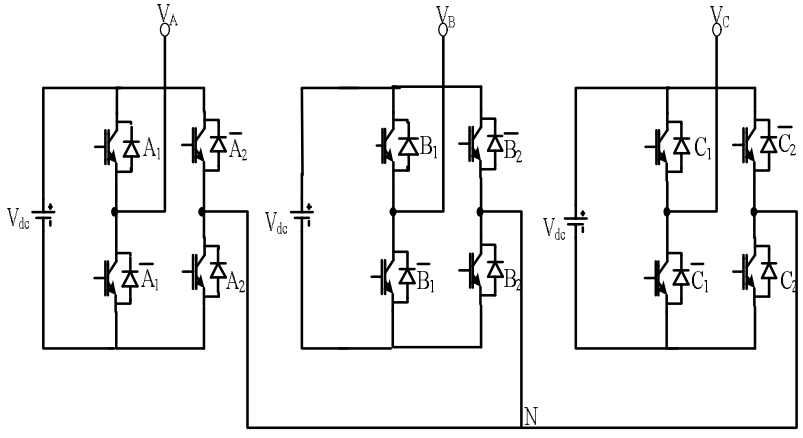


Figure 3.4: Three-level Cascaded H-Bridge Topology

Identical H-bridges lead to reduction of manufacturing cost which is considered an attractive feature of this topology. However, voltage level at which each bridge operates is different.

There must be a separate DC source for the DC bus of every individual H-bridge, Figure. 3.4 Hence, this topology is useful for collecting energy from renewable energy resources e.g. solar panels and fuel cell. Due to the isolated DC-links, this topology does not have the DC-link unbalancing problem due to neutral point current as in NPC topology explained in [3.2.1].

3.2.2. Principle of Operation of one Leg

Table 3.4: Switching state in H-BridgeTopology

SWITCHING STATE	A_1	A_2	V_{DC}
1	ON	ON	$+V_{DC}$
0	ON	OFF	0
-1	OFF	OFF	$-V_{DC}$

CHAPTER 4
MODULATION TECHNIQUE

Chapter 4

MODULATION TECHNIQUE

The pulse width modulation (PWM) is a preferred mean of modulating power through the inverter. The typical desired features of a PWM technique are low THD, low switching losses, better DC-link utilization, less computation and simple implementation.

A number of modulation strategies are used in multilevel power conversion applications. They can generally be classified into three categories:

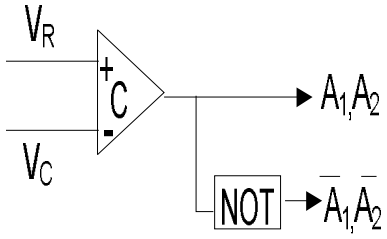
- Fundamental Frequency switching strategies
- Space Vector PWM strategies
- Carrier based PWM strategies

Of all the PWM methods for cascaded multilevel inverter, carrier based PWM methods and space vector methods are often used but when the number of output level is more than five, the space vector method will be very complicated with the increase of switching states.

So the carrier based PWM method is preferred under this condition in multilevel inverters. This project work focused on carrier based PWM techniques which have been extended for use in multilevel inverter topologies by using multiple carriers.

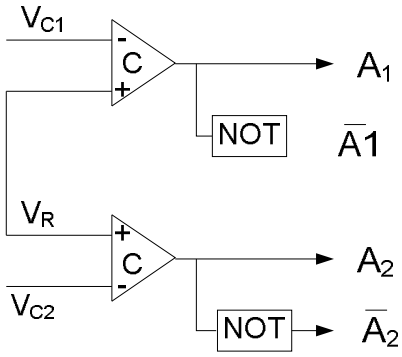
The carrier based PWM switching can be divided into two switching scheme which are PWM with Bipolar voltage switching and PWM with Unipolar voltage switching.

For Bipolar control scheme, diagonally opposite switches are switched simultaneously to get two level output waveform.



Where V_R is the Reference wave and V_C is the Carrier wave

For Unipolar switching control scheme, the full bridge inverter is used to synthesize a three level pulse width output waveform. The switches in the two legs of the inverter are not switched simultaneously, as in bipolar voltage switching scheme.



Where V_R is the Reference wave and V_{C1} and V_{C2} are the Carrier wave

In multilevel case, SPWM techniques with three different disposed (level shift) triangular carriers were proposed as follows:

1) All the carriers are alternatively in opposition (APO disposition)
2) All the carriers above the zero value reference are in phase among them, but in opposition with those below (PO disposition)
3) All the carriers are in phase (PH disposition)

An n-level Cascaded H-bridge inverter using level shifted modulation requires (n–1) triangular carriers, all having the same frequency and amplitude. The frequency modulation index is given by $m_f = f_{cr}/ f_m$, where f_m is modulating frequency and fcr are carrier waves frequency. The amplitude modulation index m_a is defined by $m_a = V_m/ V_{cr}$ (m-1) for $0 \leq m_a \leq 1$ Where V_m is the peak value of the modulating wave and $V_{cr}$is the peak value of the each carrier wave, different (level shift) triangular carriers are explain as below:

4.1: ALTERNATE PHASE DISPOSITION (APOD)

As can be seen in the figure for a five level inverter a total of four carrier waves are used.

1) They are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees.
2) The converter switches to + V_{dc} / 2 when the sine wave is higher than all carrier waveforms
3) The converter switches to V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers
4) The converter switches to 0 when the sine wave is lower than the two uppermost carrier waveform and greater than two lowermost carriers
5) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

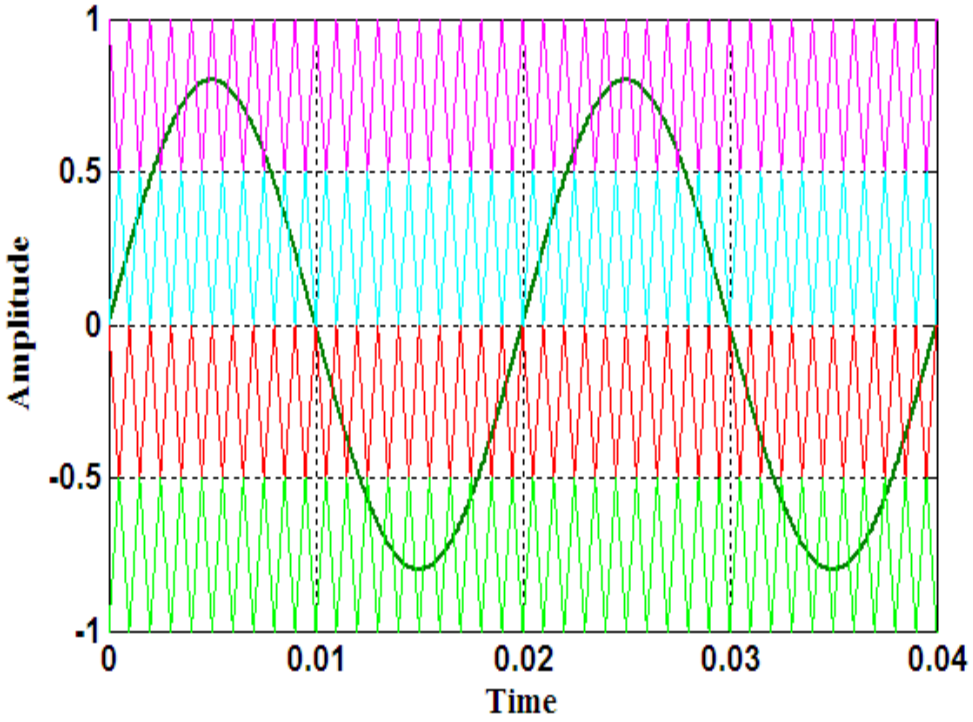


Figure: 4.1. Alternate Phase Disposition

4.2: OPPOSITE PHASE DISPOSITION (OPD)

As can be seen in the figure for a five level inverter a total of four carrier waves are used.

1) They are arranged in such a manner that all carrier waveforms above zero are in phase and are 180 degrees out of phase with those below zero.
2) The converter switches to + V_{dc} / 2 when the sine wave is higher than all carrier waveforms
3) The converter switches to V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers
4) The converter switches to 0 when the sine wave is lower than the two uppermost carrier waveform and greater than two lowermost carriers
5) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

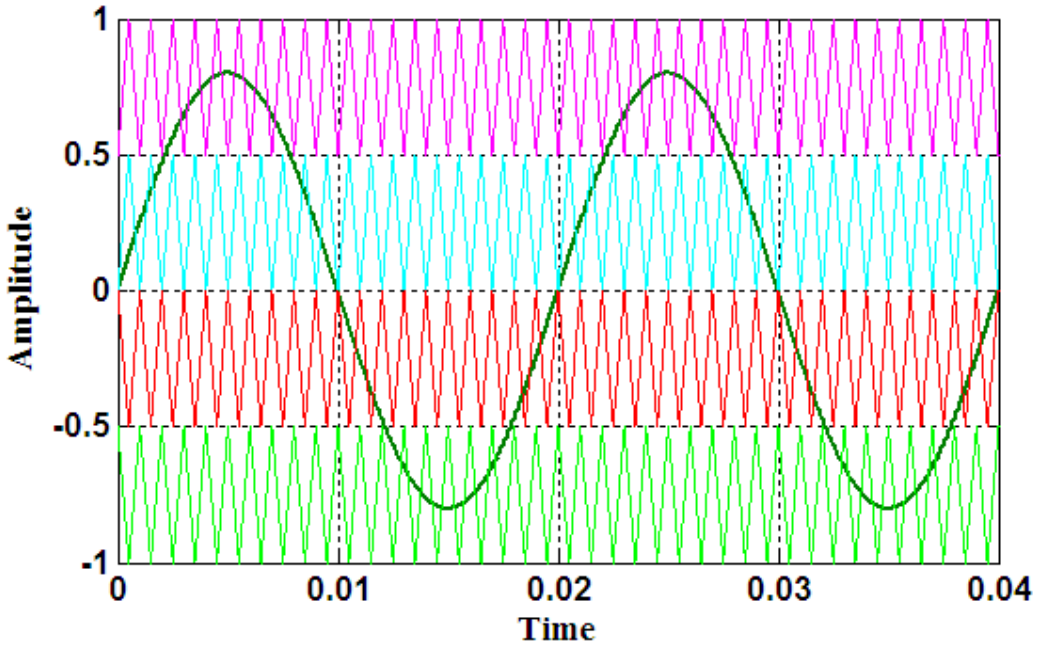


Figure 4.2: Opposite Phase Disposition

4.3: PHASE DISPOSITION (PD)

As can be seen in the figure for a five level inverter a total of four carrier waves are used.

1) They are arranged in such a manner that all carrier waveforms above zero and below zero are in phase.
2) The converter switches to + V_{dc} / 2 when the sine wave is higher than all carrier waveforms
3) The converter switches to V_{dc} / 4 when the sine wave is lower than the uppermost carrier waveform and greater than all other carriers
4) The converter switches to 0 when the sine wave is lower than the two uppermost carrier waveform and greater than two lowermost carriers
5) The converter switches to - V_{dc} / 4 when the sine wave is higher than the lowermost carrier waveform and lesser than all other carriers.

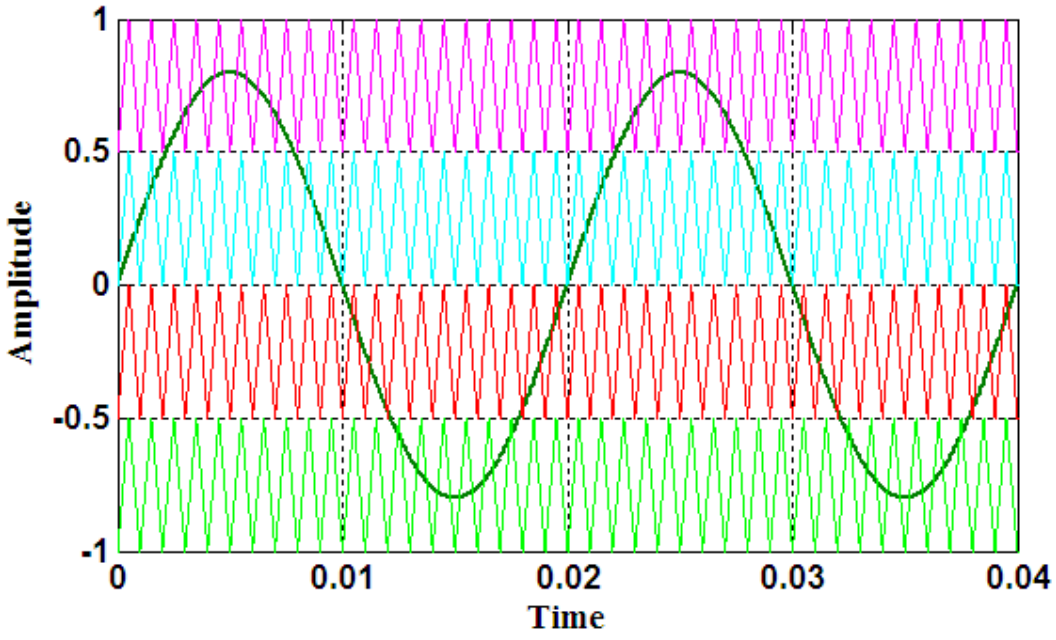


Figure 4.3:Phase Disposition

CHAPTER 5

SIMULATION RESULTS

Chapter 5

SIMULATION RESULTS

In this chapter, we are considering the simulation of all the three topologies of multilevel inverter. Simulation parameters for three level inverter are given below:

DC Bus Voltage	100 V
Carrier frequency	1 kHz
Fundamental frequency	50Hz
Load	R=1Ω,L=100 H

Simulation model of three level Neutral Point Clamped Topology

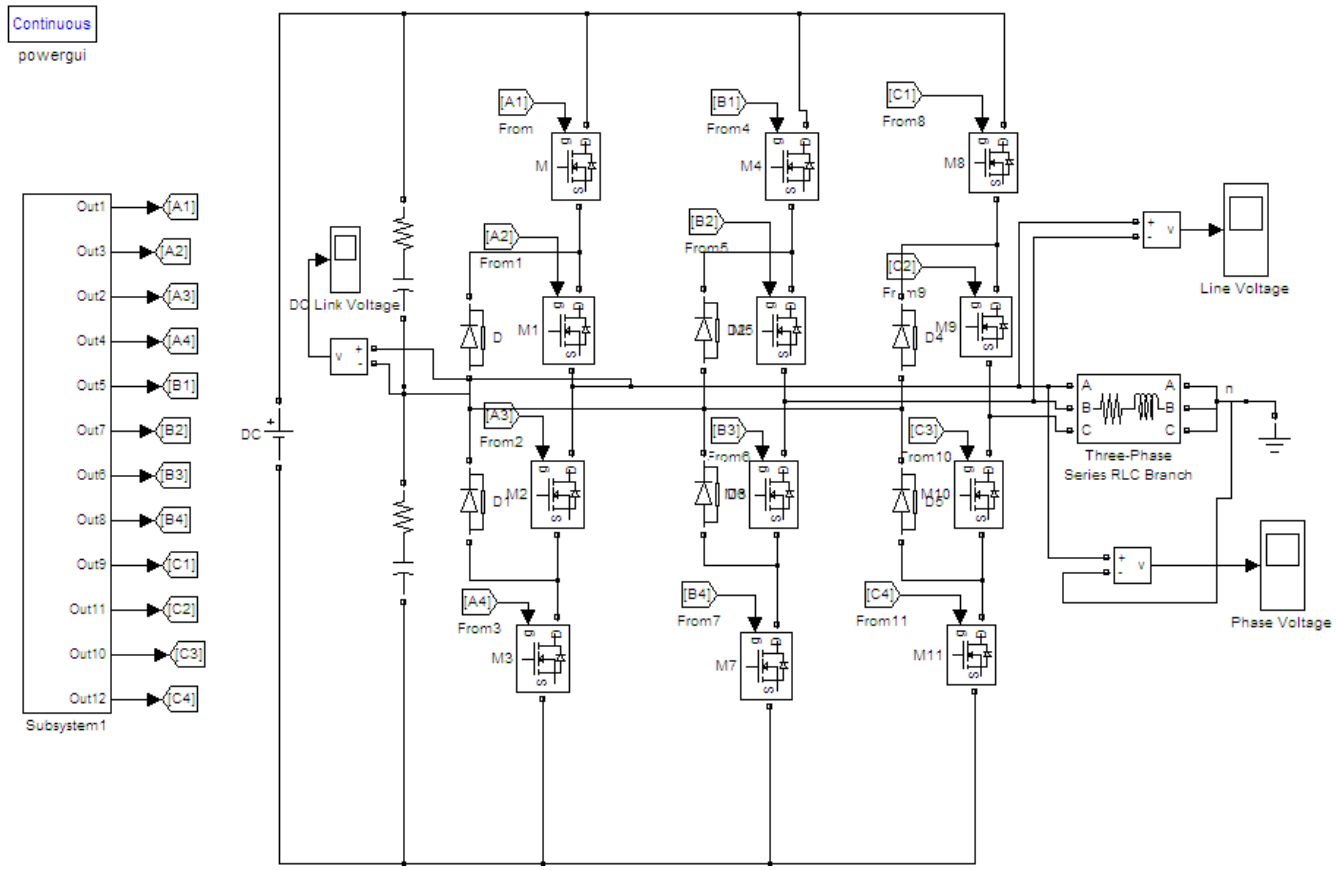


Figure 5.1: Simulation Model of Three Phase Three Level Neutral Point Clamped Inverter

Phase voltage for neutral point clamped topology

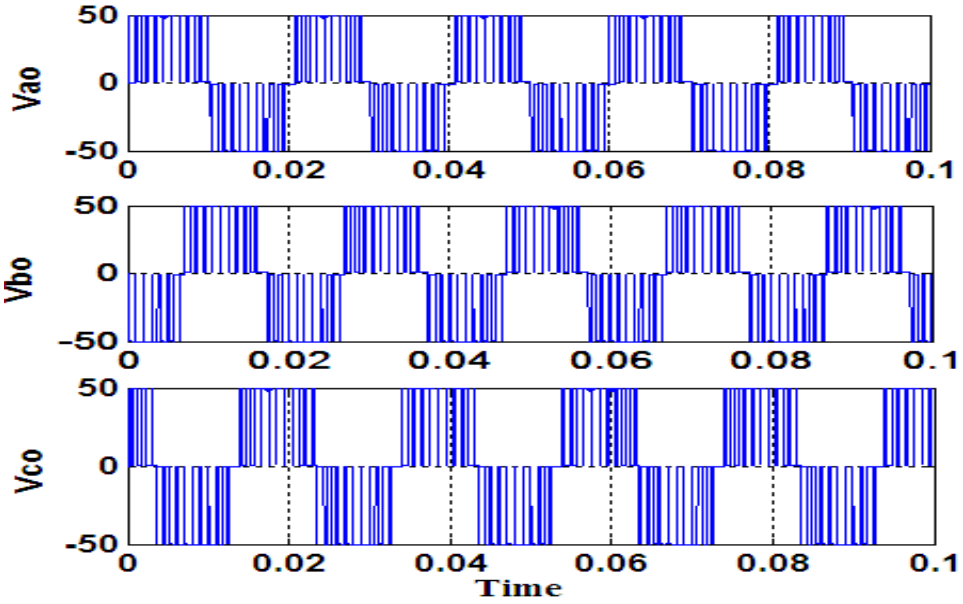


Figure 5.2: Phase Voltage of Three LevelInverter for neutral point clamped topology

Line voltage for neutral point clamped topology

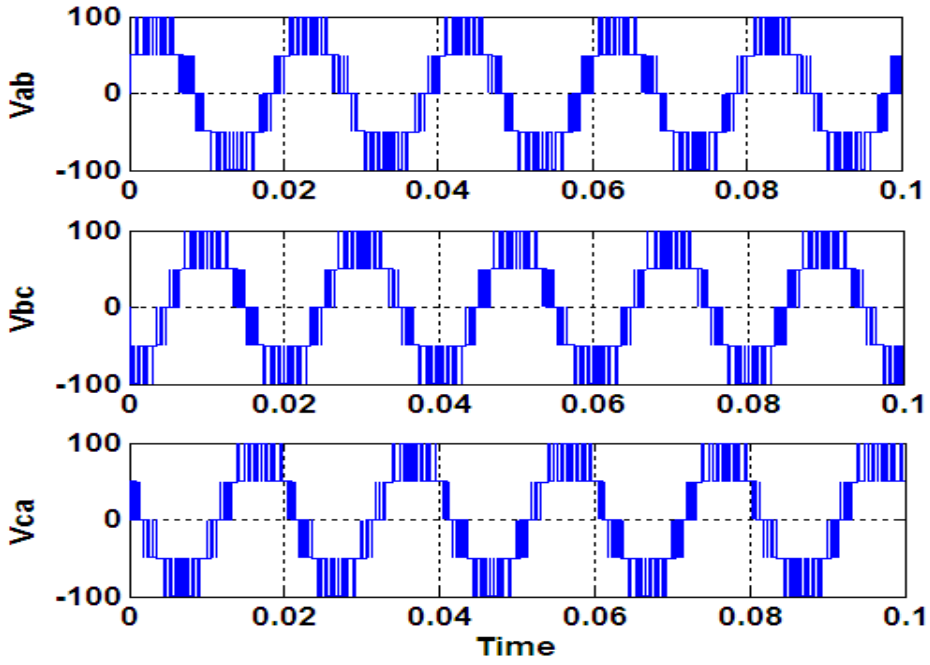


Figure 5.3: Line Voltage of Three LevelInverter for neutral point clamped topology

Simulation model of Capacitor Clamped Topology

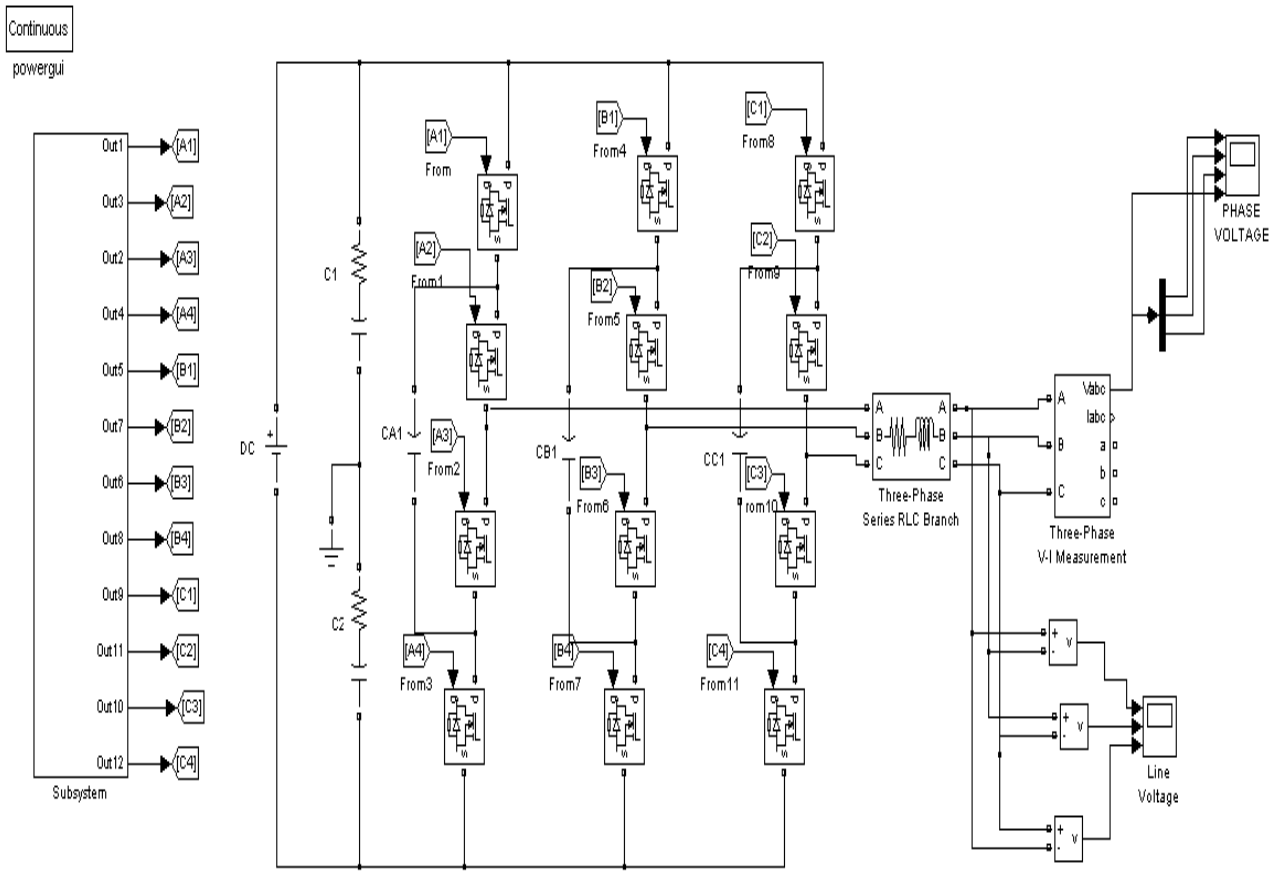


Figure 5.4: Simulation Model of Three Phase Three Level Capacitor Clamped Inverter

Phase voltage for Capacitor Clamped Topology

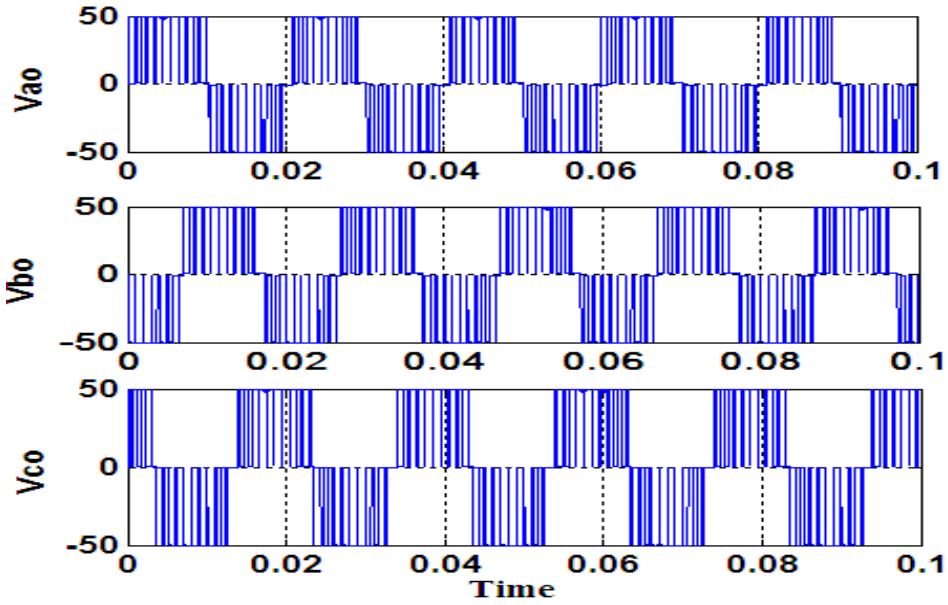


Figure 5.5: Phase Voltage of Three LevelInverter for Capacitor Clamped Topology

Line voltage for Capacitor Clamped Topology

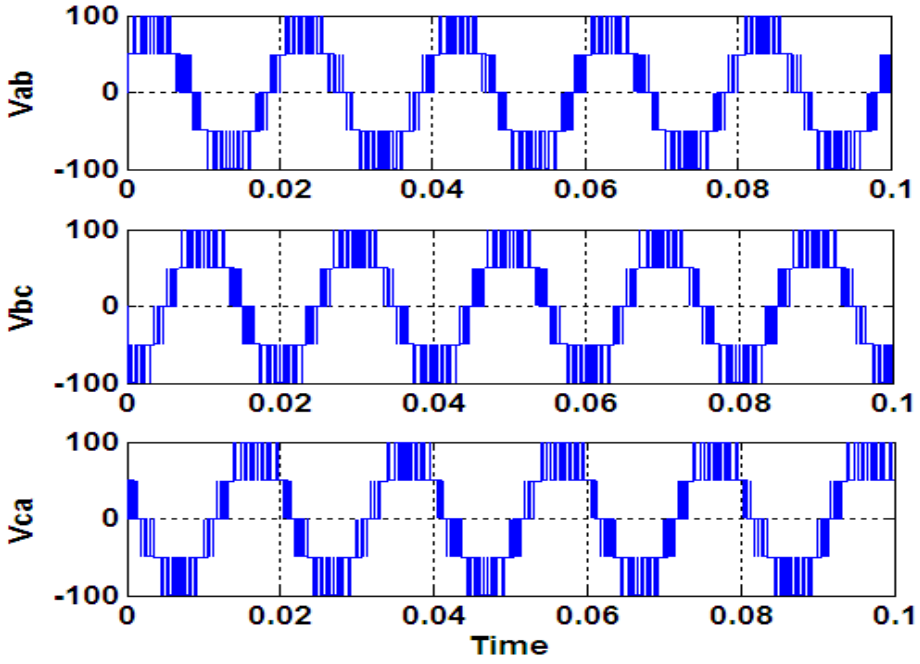


Figure 5.6: Line Voltage of Three LevelInverter for Capacitor Clamped Topology

Simulation model of three level H-bridge inverter

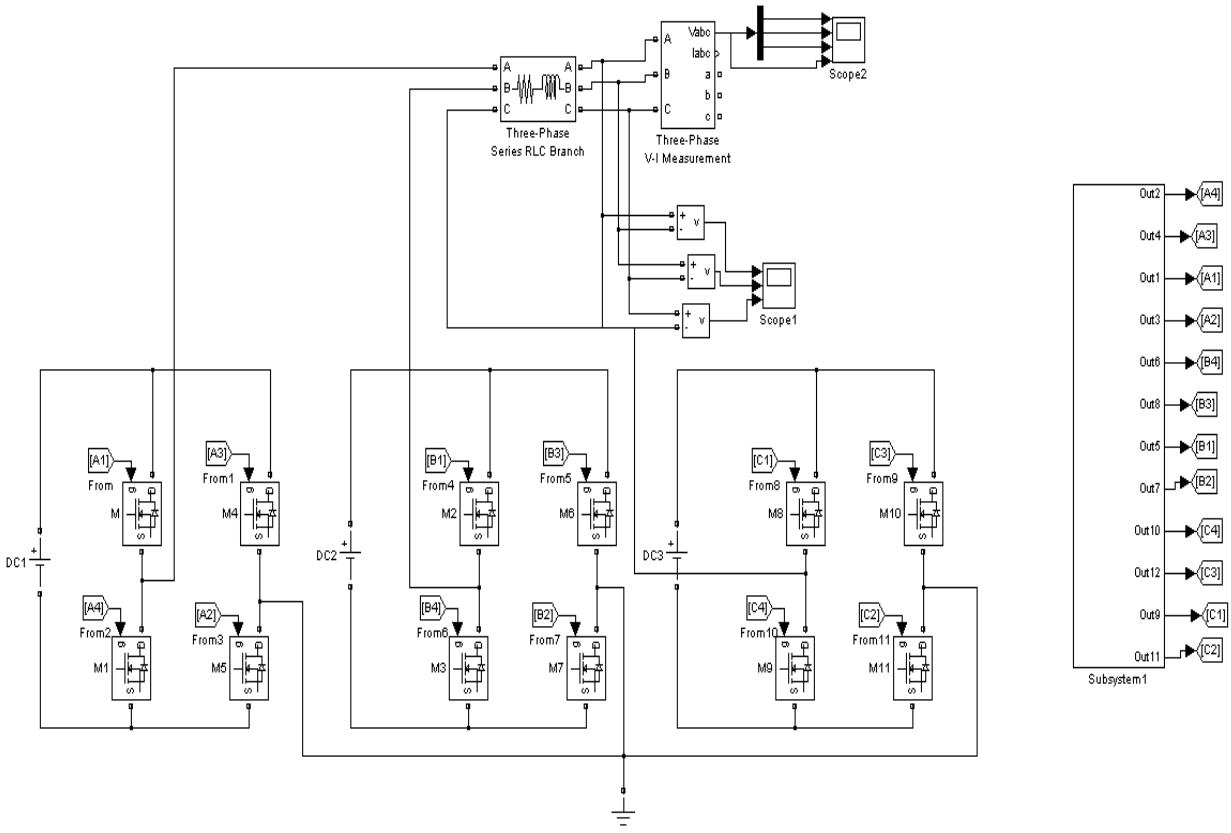


Figure 5.7: Simulation Model of Three Phase Three Level Cascaded H-Bridge Inverter

Phase voltage for H-Bridge inverter

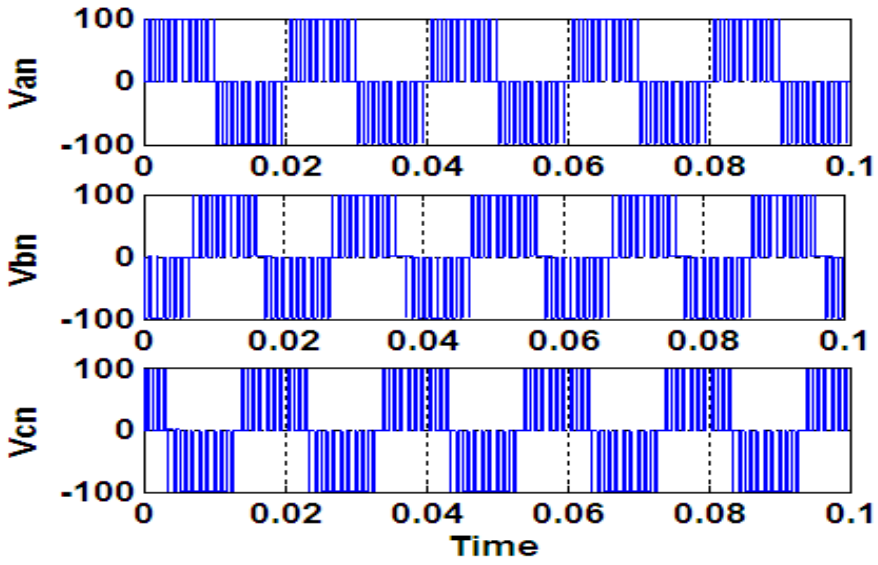


Figure 5.8: Phase Voltage of Three LevelH-Bridge Inverter

Line voltage for H-Bridge inverter

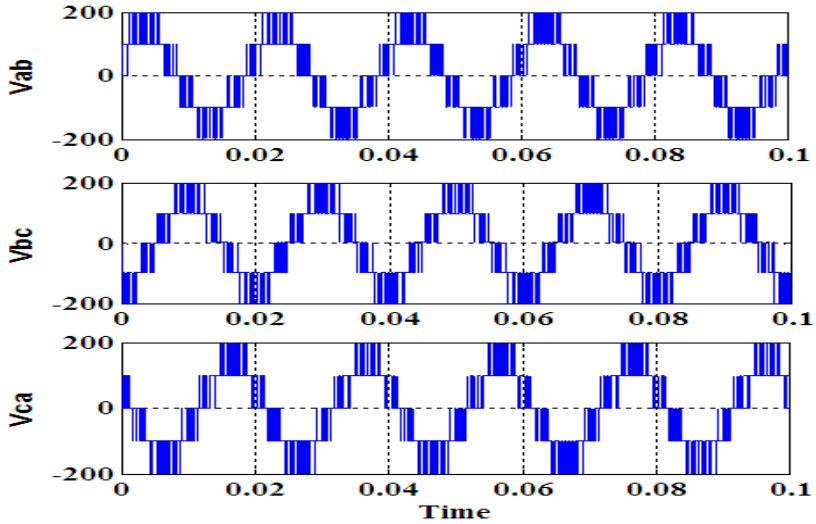


Figure 5.9: Line Voltage of Three LevelH-Bridge Inverter

From the above results it is observed that, the neutral point and capacitor clamped topologies have the same output voltage value but in case of H-bridge topology the output voltage have get more value than the two topologies (neutral point and capacitor clamped).

CHAPTER 6

ANALYSIS OF H-BRIDGE MULTILEVEL INVERTER

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Cascaded H-bridge multilevel inverter is one of thepopular converter topologies used in high-power Medium-Voltage (MV) drives As the name suggests, thecascaded H-bridge multilevel inverter has been usedmultiple units of H-bridge power cells connected in a seriesto achieve medium-voltage operation and low harmonicdistortion

The concept of this inverter is based on connecting H-bridge inverters in series to get a sinusoidal voltage output. The output voltage is the sum of the voltage that is generated by each cell. The number of output voltage levels are 2n+1, where n is the number of cells.One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the Diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two former types. There are some of the advantages of H-bridge inverter over diode clamped inverter and flying capacitor inverter are given as below

6.1 ADVANTAGES OF H-BRIDGE MULTILEVEL INVERTER

1. Compared with diode clamped inverter and flying capacitor inverter , H-bridge inverters requires the least number of components to achieve the same number of voltage levels and H-bridge inverters does not require any extra clamping diodes or voltage balancing capacitors.
2. Optimized circuit layout and packaging are possible in H-bridge multi-level inverter because each level has the same structure.
3. As the number of levels are increased, the synthesize output waveform has more steps which produce a staircase wave that approaches the desired waveform. Also as the steps are added to the waveform the harmonic distortion of the output wave decreases.
4. Due to the isolated DC-links, this topology does not have the DC-link unbalancing problem due to neutral point current as in NPC topology.

6.2 ANALYSIS OF H-BRIDGE MULTILEVEL INVERTER

One of the biggest problems in power quality aspects is the harmonic contents in the electrical system. Generally, harmonics may be divided into two types:

1) Voltage harmonics and
2) Current harmonics

Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives.

Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. There are several methods to indicate of the quantity of harmonics contents. The most widely used measure in North America is the total harmonics distortion (THD) which is defined in terms of the amplitudes of the harmonics, H_n.

Where, n is integer and H_1 is amplitude of the fundamental component The THD is mathematically given by

$$\text{THD}=\frac{\sqrt{\sum_{n=2}^{\infty} H_{(n)}^2}}{H_1}$$

6.3 SIMULATION OF THREE LEVEL H-BRIDGE MLI:

DC Bus Voltage	100 V
Fundamental frequency	50Hz
Load	R=10Ω

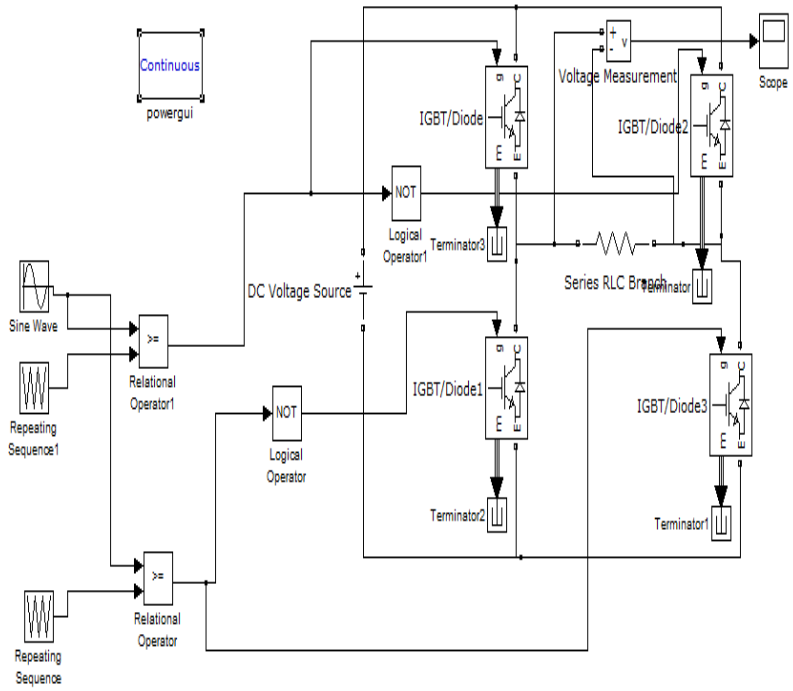
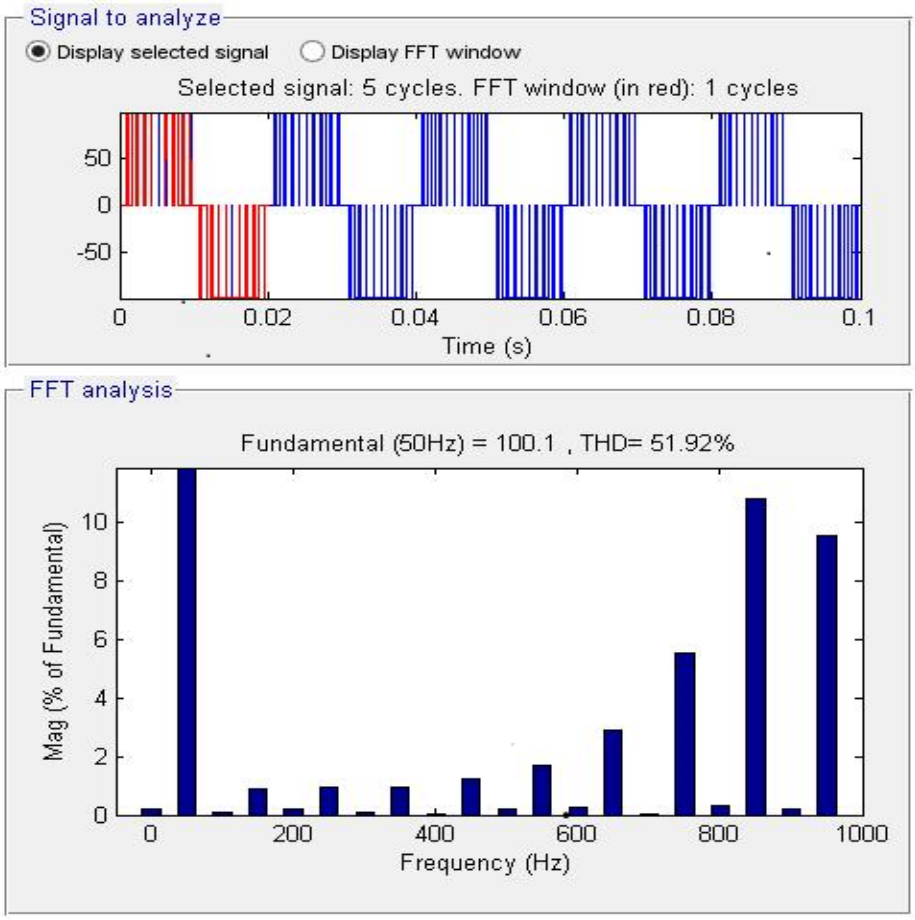
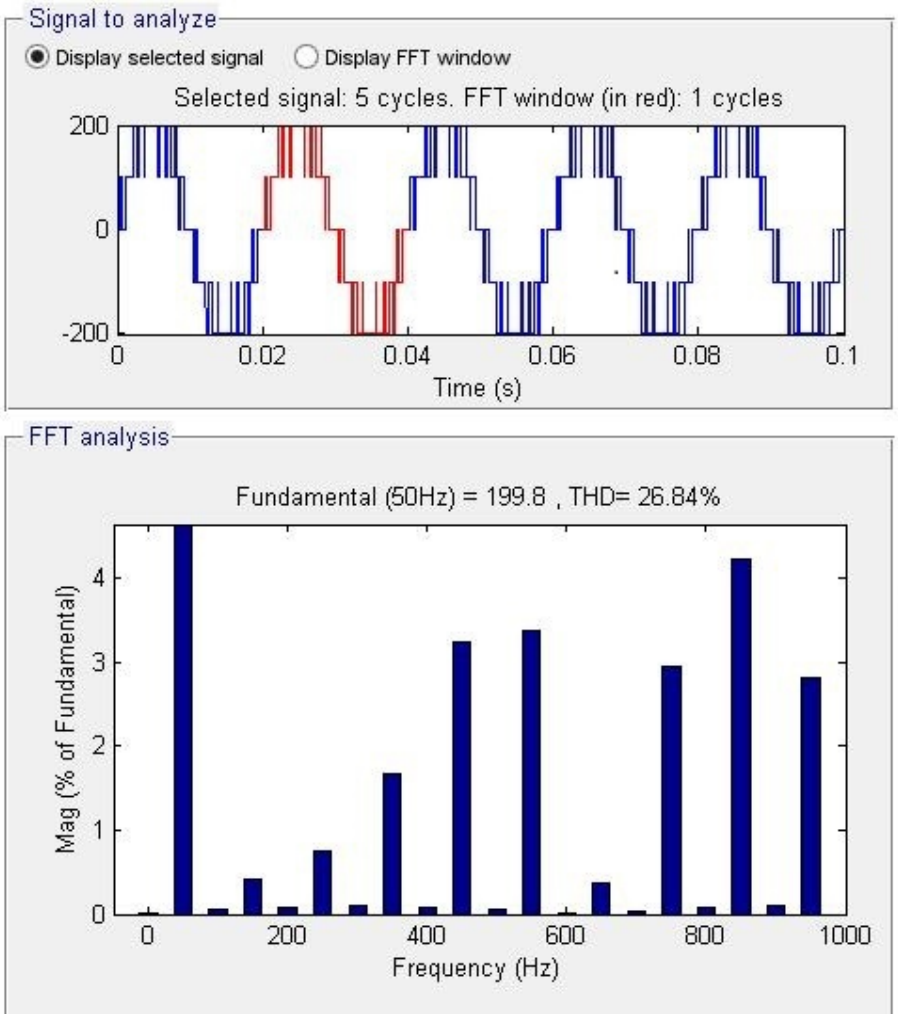


Fig. 5.1 Simulink Model of Three level Single Phase MLI.



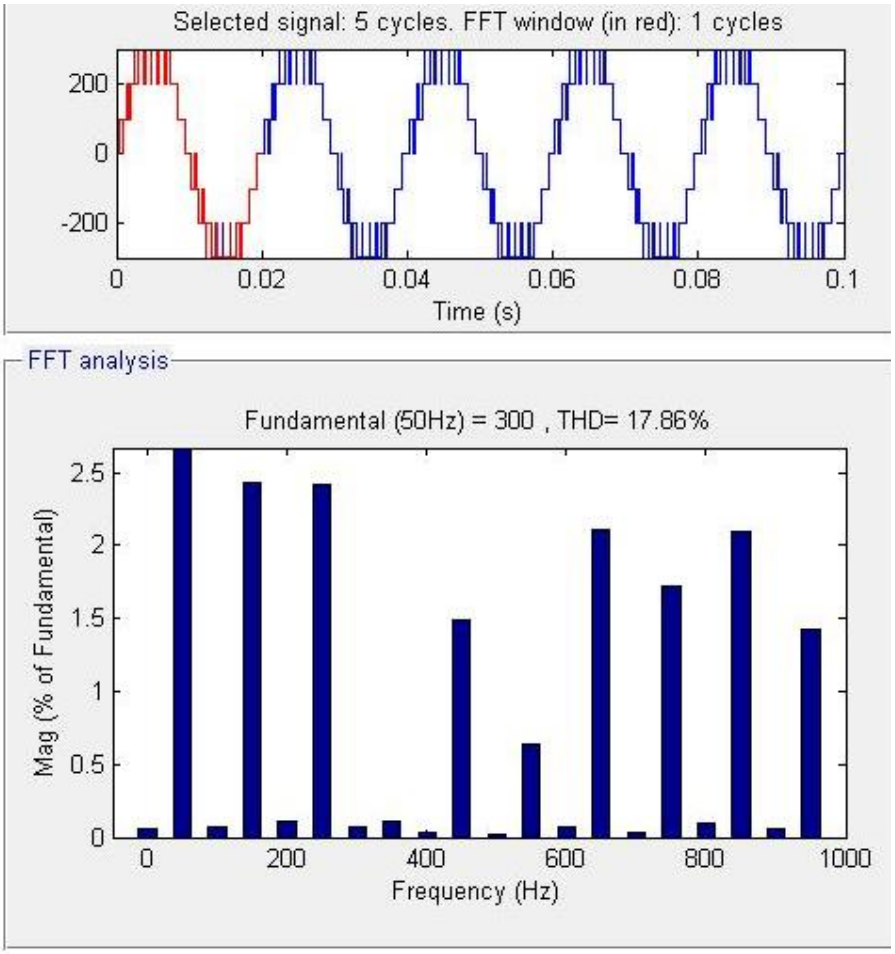
Simulation of Three level Inverter

Above simulation result shows the total harmonics distortion of three level inverter. As we can see that THD for three level inverter is 51.92% by using phase disposition modulation techniques.



Simulation of five level Inverter

Above simulation result shows the total harmonics distortion of five level inverter. As we can see that THD for five level inverter is 26.84% by using phase disposition modulation techniques.



Simulation of seven level Inverter

Above simulation result shows the total harmonics distortion of seven level inverter. As we can see that THD for seven level inverter is 17.86% by using phase disposition modulation techniques.

CHAPTER 7

CONCLUSION AND FUTURE SCOPE

Chapter 7

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

We hereby conclude that Multi-level inverter is a very promising technology in the power industry. In this project, the advantages of Multi-Level Inverters are mentioned and a detailed description of different multi-level inverter topologies is presented.

Three Phase three level and five level H-Bridge Inverters functioning is realized virtually using MATLAB SIMULINK. A detailed Multi-Level Inverter is presented from which we concluded that the harmonic content is greatly reduced in Multi-Level Inverter.

A single phase three level MOSFET based Cascade H-Bridge Inverter is designed and implemented practically and is tested with non-inductive resistive load. The components used in the practical implementation of H-Bridge Inverter are described in detail.

7.2 FUTURE SCOPE OF PROJECT

This project can be extended further by increasing the number of levels in multi-level inverter.Here PWM are generated by using analog circuit butthere are some disadvantages associated with analog modulation scheme which are listedbelow:

1) They are prone to environmental noise and temperature changes. Hence they are notsuitable where these factors are prominent.

(2) They also suffer variation due to component variation .e.g. for a variation in comparatorthere is variation in PWM output.

To overcome these various problems Digital techniques can be used or by microcontroller programming can be used to generate gating pulses directly rather than designing them by using comparators.Another future for multilevel inverters is using DSP controllers an intelligent control approach is possible to reduce the overall system cost and to improve the reliability of the system performance.

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