RF PROTECTION INTERLOCK SYSTEM FOR LEHIPA

Submitted in partial fulfilment of

requirement in degree of

Bachelor in Engineering

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Project Report Approval for B.E

This project report entitled ***RF PROTECTION INTERLOCK SYSTEM FOR LEHIPA project initiative by BARC (BHABHA ATOMIC RESEARCH CENTRE)***

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Declaration

We declare that this written submission represents the project initiative by **BARC (BHABHA ATOMIC RESEARCH CENTRE)** and where other sides or words have been included; we have adequately cited and referenced the original sources. We also declare that we have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my opinion. We understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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We appreciate the beauty of a rainbow, but never do we think that we need both the sun and the rain to make its colours appear. Similarly, this project work is the fruit of many such unseen hands.
It's those small inputs from different people that have lent a helping to our project.

I take this opportunity to express my profound gratitude and deep regards to my guide at BARC **Mrs Sujo C.l. ,** for her exemplary guidance, monitoring and constant encouragement throughout the course of this project work.

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ABSTRACT

Nuclear Power appears to be an inevitable option as future energy source; but disposal of nuclear waste is an important issue of concern in harnessing nuclear energy through “critical reactors”, which needs to be addressed satisfactorily. In India, economic exploitation of nuclear power is considerably dependent on Uranium &Thorium.

Accelerator-Driven System (ADS) has the potential to provide an additional route to an efficient use of the available uranium and thorium resources, besides offering a way towards nuclear waste incineration. o The most challenging part of this CW proton accelerator is development of the low-energy injector, typically up to 20 MeV, because the space charge effects are maximal here. Therefore, BARC has initiated a programme for the development of a Low Energy (20 MeV) High Intensity Proton Accelerator (LEHIPA) as front-end injector of the 1 GeV accelerator for the ADS programme.

RF Protection Interlock (RFPI) system has been developed for the protection of high power RF components in LEHIPA. The system consists of six VME64X based modules which processes output of different sensors. The system is designed based on a mezzanine card approach with a common base board. All the function specific boards are mounted as mezzanine boards. After detecting any fault, time required for RFPI system to switch off RF power to the cavities is less than 1us.

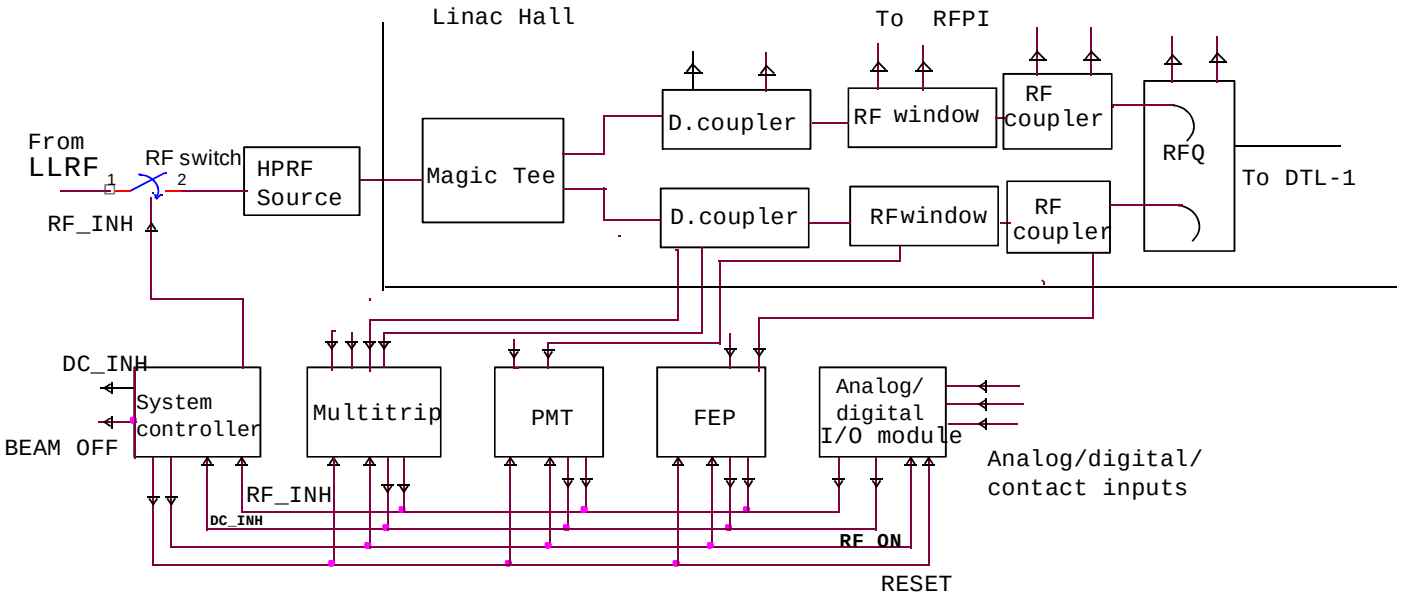
The system consists of the following modules.

1. Multi trip module- processes the pickup RF signals from directional couplers.
2. Photo Multiplier Tube (PMT) module- processes output signals from PMTs
3. Field Emission Probe (FEP) module- processes output of field emission probes
4. Photo diode module- processes optical signal or arc signals from the system
5. Photo transistor module- processes output of photo transistor which is mounted on RF window
6. System control module-which processes RF leakage signals from wave guide joints and also generates RESET and Video Pulse signals to other modules of the system.

There are many fault conditions which are detrimental to the accelerator operation; some of them are listed below.

1) Waveguide arcs
2) Plasma generation in the coupler
3) RF leakage from waveguides
4) Forward Power overdrive due to absence of beam loading in the cavity
5) Reflected Power due to load mismatch at the klystron and the cavity
6) Cavity Vacuum degradation
7) Coupler Window Temperature rise

Functional Block Diagram of RFPI



We have tested and worked on various faults and modules of RFPI i.e.

i. Detection of Coupler Window Temperature rise

ii. Module on photodiode

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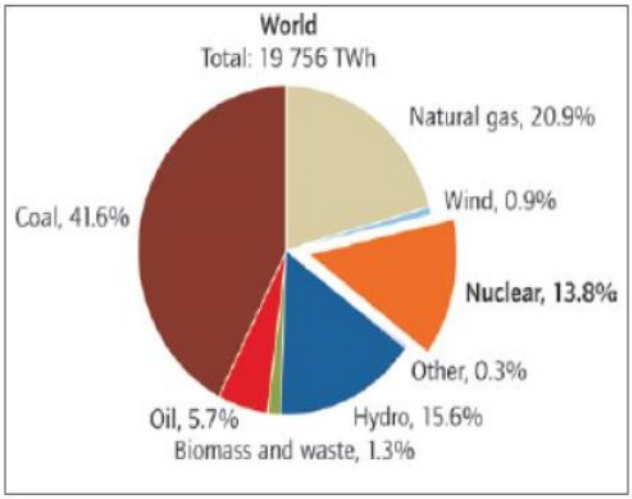
NUCLEAR POWER



Electricity generation worldwide (OECD, 2007)

Fig.NO.1.

- Nuclear Power appears to be an inevitable option as future energy source; but disposal of nuclear waste is an important issue of concern in harnessing nuclear energy through "critical reactors", which needs to be addressed satisfactorily
- In India, economic exploitation of nuclear power is considerably dependent on
  - Uranium
  - Thorium
- At the present consumption level, known reserves for coal, oil and gas correspond to a duration:
- Coal: 230 yrs Oil: 45 yrs Gas: 65 yrs

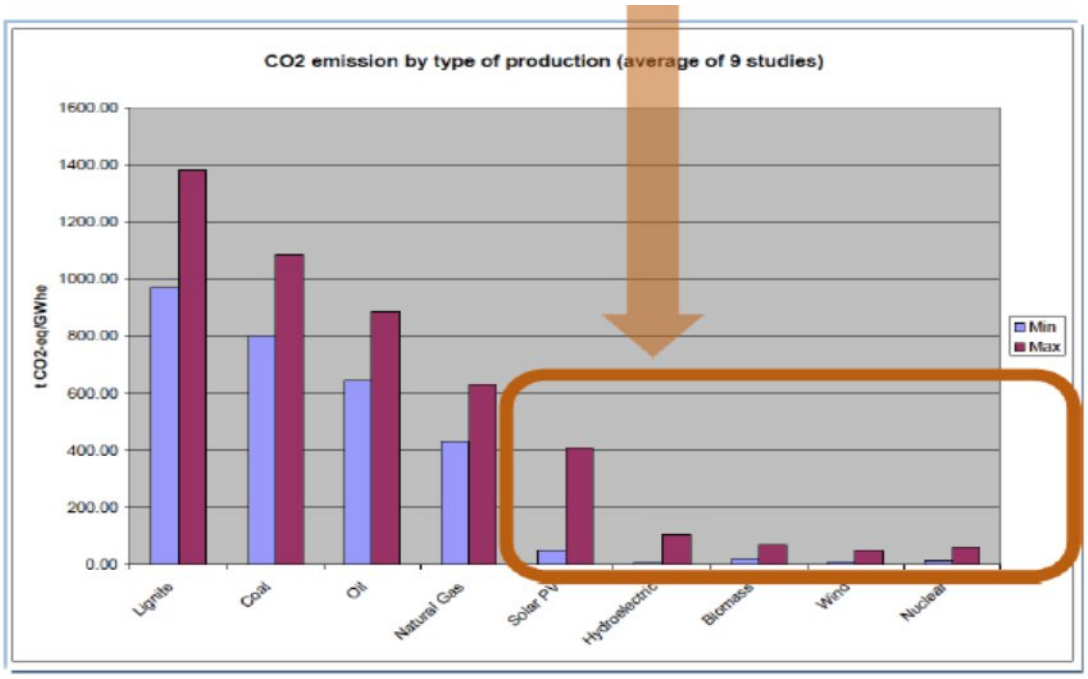


FIG.NO.2

- Attractive Features of Thorium / Thoria
  - High Abundance
  - Uniformly distributed in earth crust
  - 3 to 4 times abundant than uranium
  - Better Fuel Performance Characteristics
  - Higher melting point
  - Better thermal conductivity
  - Lower fission gas release
  - Good radiation resistance and dimensional stability
  - Reduced fuel deterioration in the event of failure
  - Relative ease in Waste Management
  - No oxidation -Superior behaviour and suitable for direct disposal in repository as it is monovalent.
  - Generates less plutonium and minor actinides

- India needs a system which can…
  - Produce energy
  - Efficient use of thorium resources
  - Transmutation of high level long-lived radioactive waste
  - Incineration of minor actinides

ADS (ACCELERATOR DRIVEN SYSTEM)

- A new type of fission reactor, where nuclear power (say, 500-1000 MWe) can be generated in a neutron multiplying core (keff < 1.000) without the need of criticality.
- But, ADS has to be driven by an external neutron source and hence it is inherently safe system.
- In India, long-term economic exploitation of nuclear power is considerably dependent on an efficient utilization of the thorium through the reactor based Th-U_{233} fuel cycle.
- Accelerator-Driven System (ADS) [1] has the potential to provide an additional route to an efficient use of the available uranium and thorium resources, besides offering a way towards nuclear waste incineration.
- Consequently, it has evoked considerable interest in the nuclear community the world over as well as in India.
- Our effort naturally is directed towards devising ADS relevant to the $_{233}$U-Th cycle.
- Accelerator Driven System (ADS) mainly consists of a sub-critical reactor coupled to a high power proton accelerator through high Z spallation target.

Country	ADS Projects
JAPAN	Under its OMEGA (Option Making Extra Gains of Actinides and FP), that is extension of its earlier Actinides Burner Reactor (ABR).
KOREA	Under its HYPER (Hybrid Power Extraction Reactor) programme.
ITALY	Under its TRASCO (TRAnsmutation SCOrie) Programme and, Industrial project undertaken by ANSALDO for EC
CHINA	Proposed as CIAE+IHEP project but under an un-named ADS programme of Sino-Italian collaboration.
BELGIUM	Under MYRRHA project as extension of ADONIS (Accelerator-Driven Operated New Irradiation System) programme for radioisotope production.
FRANCE	Its CNRS/IN2P3 institutes are spearheading waste incineration R&D with spinoff of its TRISPAL activities for accelerator to ADS.
GERMANY	Activities under FZK in the yet un-named programme.
RUSSIA	Undertaken several study projects in ITEP/ISTC against the EC/US funding.
USA	Earlier as ATW. Now AAA (Advanced Accelerator Applications) aiming for having ADTF in 10 years from 2001. Full technological Demo in next 10 years.

Table no.1

- Role of ADS in Indian nuclear power systems
  - For sustainable thorium-based fuel cycle by introducing non-fission neutrons in the neutron inventory.
  - For cleaner nuclear power from thorium that generates reduced minor actinides waste in the spent fuel.
  - A safer way to incinerate minor actinides from spent U-Pu fuel system of stages-1 & 2 of the 3-stage nuclear power programme.

- Challenges in ADS accelerator design Accelerators for ADS applications
  - Require proton beam energy in the ~GeV range and operating with 10's of mA beam current
  - Beam loss has to be limited to < 1 watt/m
  - Require careful beam dynamics optimization to minimize the formation of beam halos for a high current beam that could lead to beam loss and activation of the structure.

- Are required to operate in the CW mode making the thermal management of normal conducting cavities difficult.

- Are required to be very reliable since they will be used for power production.

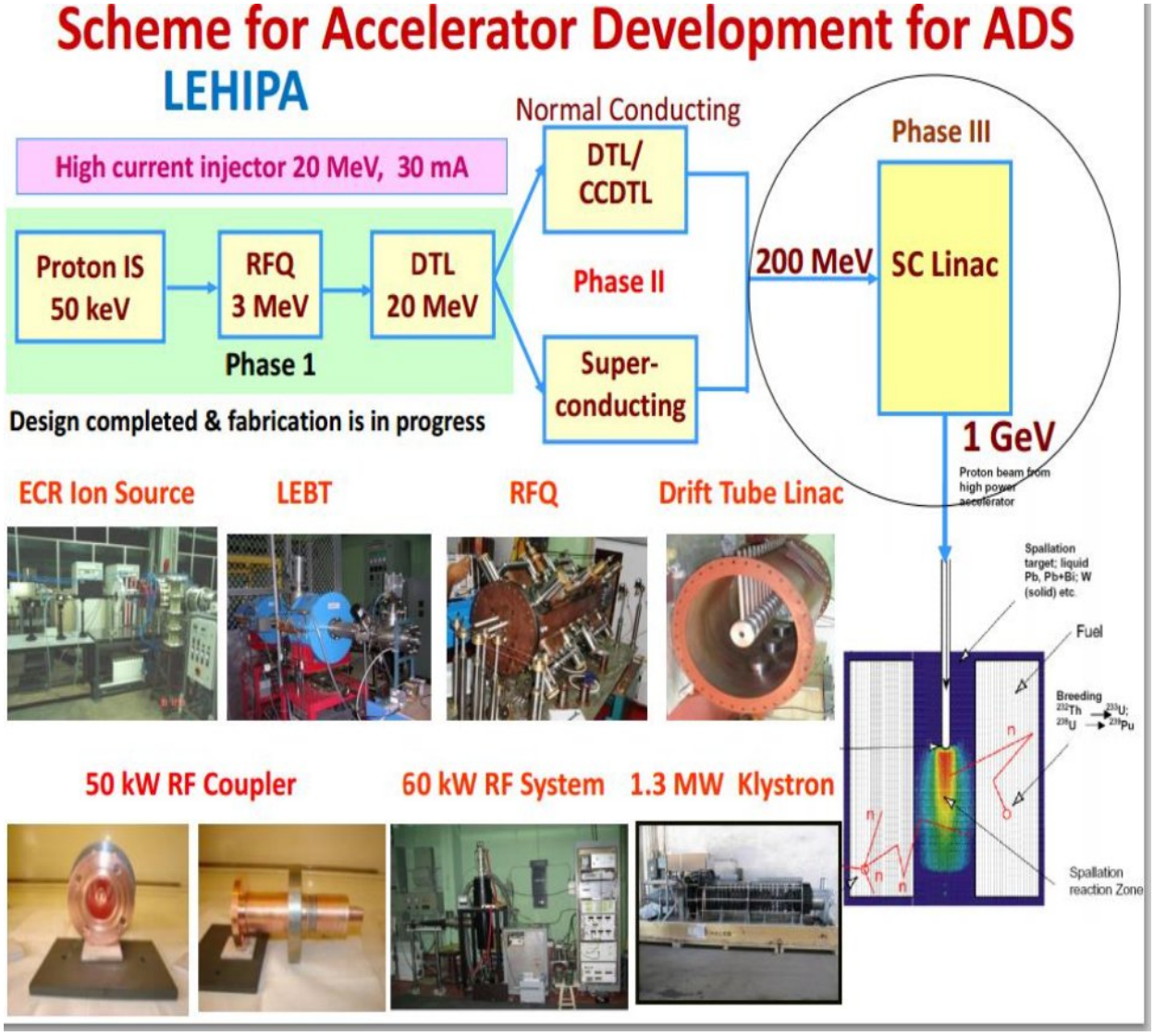
At present there is no such accelerator operating in the world!!

- It is planned that the development of the 1 GeV accelerator for ADS will be pursued in three phases, namely, 20 MeV, 100 MeV and 1 GeV.
- The most challenging part of this CW proton accelerator is development of the low-energy injector, typically up to 20 MeV, because the space charge effects are maximal here.
- Therefore, BARC has initiated a program for the development of a Low Energy (20 MeV) High Intensity Proton Accelerator (LEHIPA) as front-end injector of the 1 GeV accelerator for the ADS program.

LEHIPA

Energy (20 MeV) High Intensity Proton Accelerator (LEHIPA)

(FIG.3)



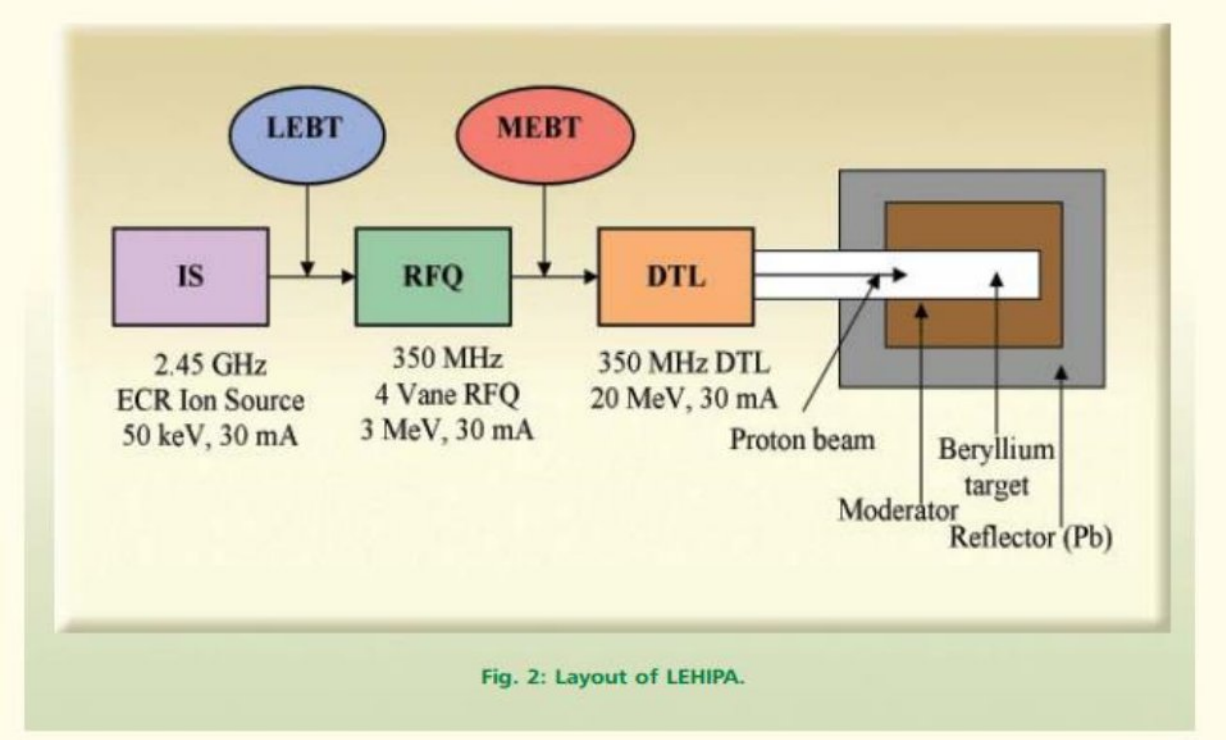


FIG.4

- The major components of LEHIPA are
  - a 50 keV ECR ion source
  - a 3 MeV Radio-Frequency Quadrupole (RFQ)
  - a 20 MeV Drift Tube Linac (DTL) [5].
  - The Low Energy Beam Transport (LEBT) and Medium Energy Beam Transport (MEBT) lines match the beam from the ion source to RFQ and from RFQ to DTL respectively. The main criterion for the design of the linac is to have minimum beam loss. The layout of the 20 MeV accelerator is shown in figure above.

- The design of various components of LEHIPA is discussed below.
  - Ion Source
    A 50 keV, 60 mA ECR ion source for LEHIPA is being developed by APPD, BARC [3]. In order to optimize the beam emittance, a five electrode extraction geometry has been used.
  - Low Energy Beam Transport line (LEBT)
    The dc proton beam from the ECR ion source is matched to the RFQ using LEBT. The main criterion for the design of the LEBT was to minimize the emittance growth with minimum beam loss. Two solenoids were used to focus and match the beam into the RFQ. Effects on the transmission through the RFQ if either solenoid strength changes from the designed value have also been studied It can be seen that if magnetic field strength of either solenoid changes by ±20 Gauss then the transmission at the end of the RFQ drops below 95%. At low energies space charge forces are very dominant and mainly responsible for increase in beam size and emittance.

In order to reduce these effects, space charge compensation technique, in which electrons produced by ionization of a residual gas neutralize the space charge of the beam, is used in the LEBT. Simulation studies show that there is no emittance growth in the LEBT when the beam is more than 95% space charge compensated [7]. Also the maximum beam radius reduces from 6.5 cm to 3.4 cm with compensation.

- Radio-Frequency Quadrupole (RFQ)

The RFQ is a low-velocity, high-current linear accelerator with high capture efficiency. It focuses, bunches and accelerates the beam simultaneously. The physics design of the 350 MHz, 3 MeV, four vane RFQs has been done. Proton beam extracted from the ECR ion source is injected into RFQ through a Low Energy Beam Transport System (LEBT). The parameters of the RFQ are shown in Table 2.The RFQ design has been done using the equi-partitioning [7] scheme, where the longitudinal and transverse temperatures of the beam should be equal. By using this technique the emittance growth was observed to be less than 2%. In this design the vane voltage has been kept constant, keeping the peak surface field less than 1.8 times the Kilpatrick limit. The total length of the RFQ is 4 m and it will be built in 4 segments, which will be coupled with coupling cells. The total RF power requirement is 500 kW which includes 88.5 kW of beam power. The LEHIPA project involves handling of very large RF power at 352.21 MHz and fabrication of long complex structures like the RFQ. In order to understand these accelerator technologies it is planned to build first a 400 keV D+ RFQ which will replace an existing 400 kV dc accelerator at PURNIMA facility in BARC. So, this system consisting of a 50 keV, 1 mA dc deuteron source, a LEBT line and a 400 keV CW RFQ has been designed. A 1.2 m long prototype of the 400 keV RFQ has been fabricated and its characterization is in progress at BARC.

Parameters	**Value**
Frequency	352.21 MHz
Input energy	50 keV
Output energy	3 MeV
Input current	30 mA
Transverse emittance	0.02/0.0204 π cm-mrad
Synchronous phase	-30^0
Vane voltage	80 kV
Peak surface field	32.8 MV/m
Length	4 m
Total RF power	500 kW
Transmission	98 %

TABLE NO.2

An indigenous power coupler development program has been initiated at the Nuclear Physics Division, BARC. Two 50 kW CW coaxial couplers are presently under fabrication. The design incorporates disc type alumina windows with double barrier for better mechanical stability and reliability of the coupler. A shorted stub will provide RF matching along with providing support for central conductor and cooling channels. A 250 kW iris type coupler for the 3 MeV RFQ, with tapered transition to WR 2300 half height wave-guide, is presently in RF design stage. The thermal loss estimation and mechanical tolerance level requirements are being worked out.

- Medium Energy Beam Transport line (MEBT)

  The MEBT has been used to match the beam from RFQ to DTL. It consists of 4 quadruples and two RF gaps for matching the beam in transverse and longitudinal planes. The total length of the MEBT is 1.04m.

- Drift Tube Linac (DTL)

  The DTL can focus and accelerate a high intensity proton beam very effectively at low energies–typically from 3 to 50 MeV, where the space charge forces are considerable. In LEHIPA, an Alvarez-type DTL is used to accelerate the beam from 3-20 MeV because of its higher effective shunt impedance as compared to Coupled Cavity Drift Tube Linac (CCDTL) Beyond 20 MeV, the bore radius has been increased from 1.1 cm to 1.4 cm which results in decrease of effective shunt impedance.

TABLE NO.3 PARAMETERS OF THE DTL:

Parameter	Value
Resonant frequency	352.21 MHz
Input energy	3 MeV
Output energy	20 MeV
Beam current	30 mA
Diameter of cavity	52 cm
Diameter of drift tube	12 cm
Bore radius	1.2 cm
Axial electric field	2.14 MV/m
Total length	12.86 m
Beam transmission	100%
Type of lattice	FFDD
Effective length of quad.	4.72 cm
Quadrupole gradient	46.5-43.6 T/m
Total power (dissipated+beam)	1.34 MW
Maximum surface field	0.53 Kilp.

- Beam Dump

  A beam dump has been designed to dissipate 600 kW (20 MeV, 30 mA) proton beam power. The beam will be stopped on a beam dump during commissioning and on a suitable neutron converter target to produce neutrons during utilization stage for which a Beryllium target will be used. In addition to neutron yield, the designed target should also have good heat removal capability. To reduce the peak power density one needs to extend the operational area of the target. Hence a conical shape of the target has been chosen. A target for beam dump of 600 kW proton beam from LEHIPA has been designed covering thermal and structural requirements. Thermal and mechanical stresses were examined both analytically and numerically in order to develop a procedure where the target dimensions could be optimized to allow the maximum amount of power to be placed on a target for a given set of conditions. Optimizing a target generally involves the balancing of stresses on the hot and cold faces so that the target will not fail for the given set of conditions. A conical shape and nickel bulk was chosen for preliminary analyses of this target and design of the water-cooling system has been finalized.

FIG NO.5 BEAM DUMP FOR 20MeV LEHIPA

RFPI

RF PROTECTION INTERLOCK SYSTEM FOR LEHIPA

Introduction

The RF Protection Interlock (RFPI) system being developed in Electronics Division, BARC for LEHIPA has three main functional objectives. The primary objective of the RFPI system is to provide a high level TTL signal to the Low Level RF (LLRF) system, permitting it to energize the High Power RF system during normal course of operation. The RFPI system continues to monitor various accelerator subsystems during the entire power 'ON' period and protects the system by issuing a RF-INH signal which will switch off the RF switch connected at the output of LLRF system within two microseconds of detection of any fault condition.

The second objective is to provide an interlock signal to the High power RF source, in case of repetitive faults. The RFPI system will issue a signal requesting to switch off the DC power supplies of High power RF source in case the same type of fault is observed on three consecutive reference RF pulses, indicating some kind of system related problem, which requires operator intervention.
The third objective is to facilitate remote monitoring and control. The operator can set trip limits remotely and receive trip alarms on the remote system. This is achieved via the Ethernet connected cPCI bus and digitization of all the analog signals being monitored by the RFPI system. The RFPI also has a provision of setting the trip limit locally for testing and debugging purpose. The RFPI can be configured to "Normal" mode of operation as well as "System Conditioning" mode depending on the system requirements.

RF Protection Interlock (RFPI) system has been developed for the protection of high power RF components in LEHIPA. The system consists of six VME64X based modules which processes output of different sensors. The system is designed based on a mezzanine card approach with a common base board. All the function specific boards are mounted as mezzanine boards. After detecting any fault, time required for RFPI system to switch off RF power to the cavities is less than 1us.

Electronics Division, BARC has developed RF Protection Interlock System to protect the high power RF components of LEHIPA. The system processes sensor outputs of directional couplers, Photo Multiplier Tubes (PMT), Field Emission Probes (FEP), photo diodes, photo transistors and RF antenna. It accepts digital /contact inputs and analog inputs from different sub systems of LEHIPA. The RFPI system can provide digital and analog outputs which can be used for the control of other sub systems. If a fault condition is detected, by any of the sensors, RF power to the cavities is switched OFF by operating a RF switch at the output of LLRF [2] system.

DIFFERENT SENSORS IN LEHIPA

In order to protect the RF components against high RF power, RF pick up signals are taken from directional couplers installed at the input of a magic Tee and RF windows. A logarithmic RF sensor having a bandwidth of 8 GHz has been selected to find the dc equivalent of RF signal. The sensor has a dynamic range of 55dB with a rise time of 10ns. Sensitivity of the sensor has been designed to be 30mV/dB.
To protect the RF couplers against arcs, photo diode sensor having a spectral response from 350nm-900nm has been selected. Response time of photo diodes is in nS. Photo transistor with response time of micro-seconds have been provided by manufactures with RF windows for arc detection .Photo Multiplier Tubes (PMT) can also be used as arc detectors. Electronics to process photodiode outputs, photo transistor outputs and PMTs has been developed.
For measuring the rapid build-up of excessive ionization in the system, Field Emission Probes (FEP) also known as Langmuir probes are mounted in the coupler. Biasing voltage required to detect the plasma formation is adjustable locally or remotely. To detect RF leakage from waveguide joints, electronics has been developed which generates DC equivalent of the RF signal. Pt100 is used for measurement of temperature of RF coupler and cavity. Analog and digital /contact signals can also be processed by RFPI system.

ARCHITECTURE OF RFPI SYSTEM

RFPI system is built around six VME64X modules each processing sensor outputs installed in LEHIPA. Each module has a carrier board on which mezzanine boards are mounted. The analog/RF signals from sensors are connected to the mezzanine boards and the detected DC signals can be viewed from the front panel. The carrier board is common to all the modules of the system on which two FPGAs are placed.
The system consists of the following modules.

1. Multi trip module- processes the pickup RF signals from directional couplers.
2. Photo Multiplier Tube (PMT) module- processes output signals from PMTs
3. Field Emission Probe (FEP) module- processes output of field emission probes
4. Photo diode module- processes optical signal or arc signals from the system
5. Photo transistor module_-processes output of photo transistor which is mounted on RF window
6. System control module-which processes RF leakage signals from wave guide joints and also generates RESET and Video Pulse signals to other modules of the system.

Each mezzanine card can process four sensor outputs and has a 14 bits quad ADC to digitize the signals being monitored. The digitized signals are stored in DDR3 on the base board and can be viewed by the user at the control room. DDR3 is a circular buffer and 1s data is available with the memory always. The data will be transferred to GUI through VME controller after fault detection. The sensor outputs can also be viewed on the front panel on SMB connectors. An EPROM has been placed on each mezzanine card in which any card related data can be stored. The detected signals are compared with trip limits set and a trip signal is generated by FPGA.

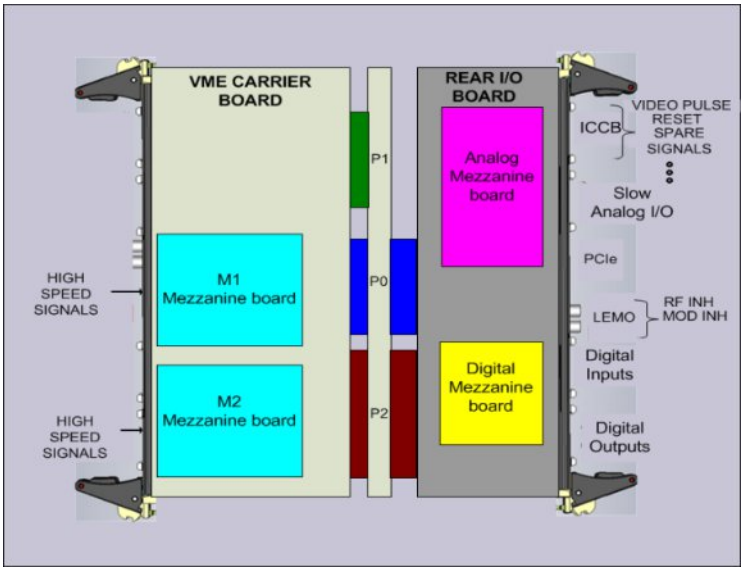


Figure 6: Arrangement of different boards in a RFPI module

This signal is communicated to System control board through VME P2 connector and Inter Card Communication Bus (ICCB) on the rear carrier card. The output signal to switch off the RF power is issued by the system control module FPGA, by OR'ing the fault signals of all the modules.

Figure 7: VME64X module with mezzanine cards

The system control module holds the analog and digital boards also on the rear carrier board. Analog I/O module processes voltage/ current inputs from the field and generates trip signals if the parameter exceeds set value. It also generates analog outputs which can be used for any control applications. Eight analog channels are available with this card. Digital card can process sixteen digital/ contact signals from the field and the trip signals are interfaced with FPGA. The digital board can generate sixteen output signals with 50 ohm cable driver which can be used for any control action in the field. At present, temperature and vacuum signals will be interfaced with analog module in LEHIPA. Water flow status signals will be interfaced with digital modules.

Each module is connected to a rear carrier board on the back plane of VME crate through which the modules are inter-connected. Digital input and output signals are connected to FPGA

through a CPLD placed on the rear carrier board and VME P2 connector. Similarly the trip signals and output signals generated by DACs on the analog board are interfaced through P2 connector and CPLD to FPGA on the VME carrier board.

DESCRIPTION OF RFPI

The measurement of sensor outputs is done during video pulse ON time, during which RF power is applied to the RF cavities. Video pulse is generated by a Programmable Timing Control Unit (PTC) which synchronizes different sub systems of LEHIPA. This signal is transmitted to all the modules through ICCB. When any sensor output exceeds the set value, a trip signal is generated and is transmitted to system control board. The trip limit can be set either by trim pots on the front panel or by DACs from control room. RF switch placed at the output of LLRF will be made OFF during the remaining period of video pulse when a trip is detected by any module.

If three trip signals are encountered in three consecutive video pulses a fault signal is generated by FPGA of that module and the fault signal is transmitted to FPGA of system control module through ICCB. The system control module generates the control signal to RF switch which inhibits the RF power to the RF cavity permanently within 1us. Fig.8 shows the timing between the detection of sensor output and generation of fault signal by FPGA in multi-trip module. The time is measured as 180 ns. Once a fault signal is detected, RESET signal is to be given to all the modules from system control board to restart the electronics. RESET signal is also propagated to other modules of the system through ICCB.

Figure 8: Measurement of time between sensor output and generation of fault signal

Requirement of RFPI System

There are many fault conditions which are detrimental to the accelerator operation; some of them are listed below.

1) Waveguide arcs
2) Plasma generation in the coupler
3) RF leakage from waveguides
4) Forward Power overdrive due to absence of beam loading in the cavity

5) Reflected Power due to load mismatch at the klystron and the cavity
6) Cavity Vacuum degradation
7) Coupler Window Temperature rise

Many more condition do exists and could be added by the user, based on the operating experience. This necessitates the RFPI to be flexible and scalable. The proposed RF Protection Interlock system has been designed as a modular system based on cPCI architecture. Each subsystem module has multiple channels, and multiple boards can be added to support the required no of channels for a particular type.
The RFPI system functional block diagram is shown below in fig.1 which indicates the signals and locations from which they can be monitored. This is just an indicative block diagram and by no means indicates all the signals that are required to be monitored.

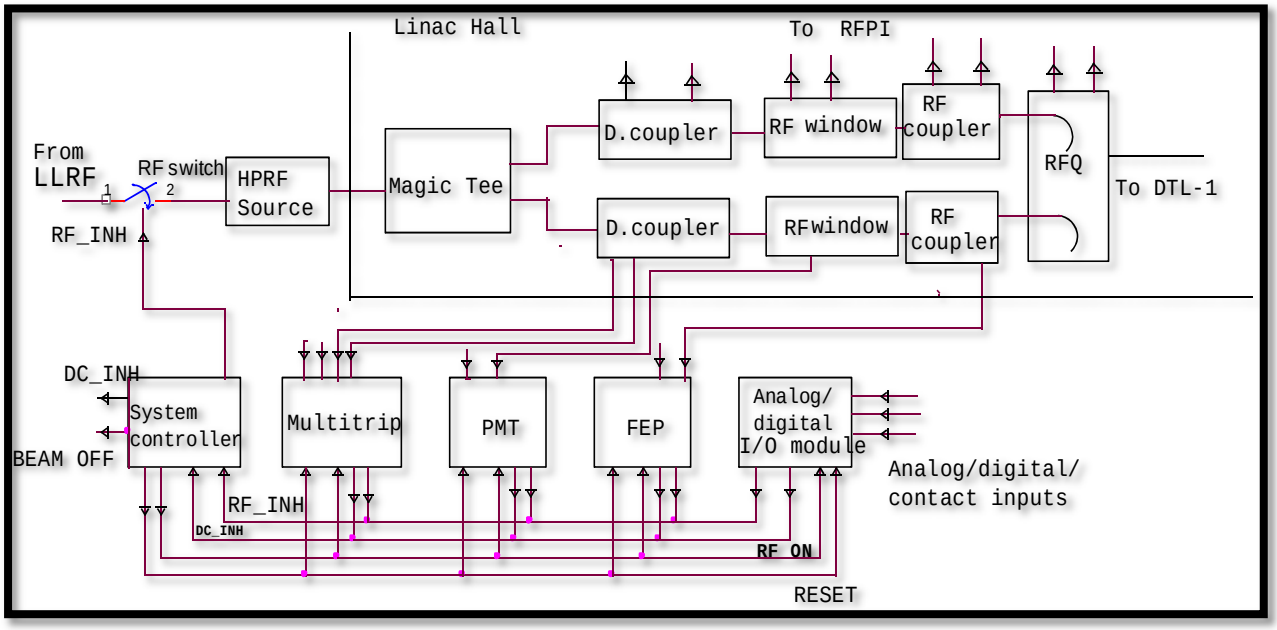


Fig.9. Functional Block diagram of RFPI System

Presently the RF protection interlock system monitors signals from the following components. Signals can be added or removed from it depending on the availability of the signals and the space to mount the sensors:

1) Klystron: Forward and Reflected power
2) Coupler: arc detection, field emission detection, ceramic window temperature, water flow status
3) Cavity: arc detection, cavity vacuum, water flow status, temperature
4) RF Wave guide: arc detection, field emission detection, ceramic window temperature
5) RF Windows: arc detection, vacuum, water flow status, temperature

RF Protection Interlock System Functional Overview

The timing signals in order to synchronize the various sub systems in LEHIPA such as ion source, LLRF,RFPI and integrated control system (ICS) etc. will be issued by a programmable timing control unit (PTC) developed in Electronics division, BARC.
After receiving a trigger signal from ICS through Ethernet, PTC will issue RF ON signal to LLRF and RFPI system. RFPI system will use this signal as a reference input signal. The RF ON signal to individual modules will initiate the individual state machine for the corresponding channels. The interlock system protects the monitored components by issuing 'RF_INH' signal temporarily, for switching off the GaAs switch connected at the output of LLRF within two microseconds of detection of any fault condition. The state machine for each channel, also count the fault occurrence. If three consecutive faults are observed on a particular channel, the state machine for that channel generates a permanent RF-INH signal and also a DC_INH signal which will be used to switch off DC power supply of high power RF source. RFPI system will issue a signal to switch off beam input to RF cavity also.

The system now enters 'trip state' and can only be re-armed by operator intervention. The operator can analyse the reasons for the trip and can re-arm the system after taking the necessary corrective action.

The interlock functions are independent of cPCI bus and the cPCI controller. The RFPI can continue to functions even if the cPCI backplane has locked up or the cPCI controller is non-functional. The soft trip limit references stored in the FPGA continue to update the DAC. The trip processing logic is built on to the FPGA and is independent of cPCI bus.

The RFPI modules are designed on a mezzanine card topology. The 3D model of the RFPI is shown in fig.2 below. The section that are common to all RFPI modules are kept on the base board and the section that are unique to each board are kept on the mezzanine board. The function separation is arrived by keeping analog sections as well as ADC and comparator sections on the mezzanine board. The digital sections as well as the digitizer memory are kept on the base board.

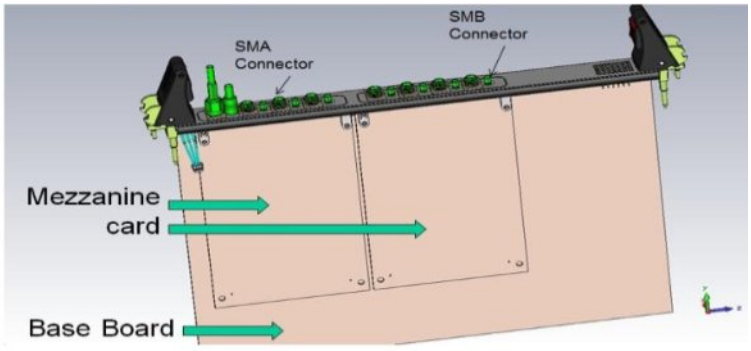


Fig.10. model of the RFPI module with Mezzanine card and base board

Each module has 128Mb of shared DDR2 memory on the base board and a four channel 14 bit 125MsPS ADC on each of the mezzanine card for digitizing the analog signals being monitored via SMA connectors. The 128 Mb Memories is configured as 8 Mega word ring buffer which can record 1 sec of signal information while operating at 8MsPS nominal sampling rate.

RF Protection Interlock System Functional Overview

The RFPI system for LEHIPA consists of following functional modules

a) multi-trip module
b) Photo Multiplier Module
c) Field Emission Module
d) Analog I/O module
e) Digital I/O module
f) RF leakage module
g) System Control Module

The trip signals from all channels on the module are OR'ed on the FPGA and a common 'RF_INH' signal is issued to the system control module. In case multiple cards of the same species are used, the common OR'ed signal from previous module is also OR'ed by next module. The same methodology is also followed for 'DC_INH' signal

a) Multi-trip Protection Module: The forward and reflected RF power from the directional couplers at the input of RF cavity is monitored by this module. The RF signal is converted to a proportional logarithmic DC voltage. The DC signal is compared with the trip limits and generates a trip signal if the signal exceeds the trip limit set by the user.

b) Photomultiplier Tube protection Module: The Photomultiplier tubes are mounted at strategic locations in the RF system for capturing a light discharge in the system. The most suitable locations are the quartz windows and bends in the RF plumbing, which gives a wide viewing angle to the PMT sensor. The PMT protection module processes this signal and generates a trip signal after comparing it with the trip limit set by the user The PMT dark current is also monitored for PMT health and reliable cable contact.

c) Field Emission Probe protection Module: The Field Emission Probes (FEP) also known as Langmuir probes are mounted at strategic locations all along the RF system for measuring the rapid build-up of excessive ionization in the system. The FEP protection card processes this signal and generates a trip signal after comparing it with the trip limit set by the user

d) RF Leakage Detection Module: The RF leakage detection module monitors leakage of RF energy from the RF system to ambient. The antennas mounted at various locations in the accelerator bay pick up the RF leakage from the systems. RF leakage detection module converts the RF signal to a proportional logarithmic DC voltage and generates a trip signal after comparing it with the trip limit set by the user.

e) Analog and Digital I/O Module: The Analog I/O module and the Digital I/O module monitor the status of various field parameters like temperature, flow rate, pressure, contact status, alarm status. The modules also interface to various status signals from PLC's that are used by many stand alone systems, for proper health monitoring of those system. The trip logic is dependent on nature of the signal and is implemented in FPGA. If an abnormal condition is detected, it blocks the RF signal to High power RF system till the fault is analyzed and corrected.

f) System Control Module: The system control module is the heart of the RFPI system. It generates all the timing signals for starting and synchronizing various state machines that are running on individual protection modules. It monitors the trip request from various modules and blocks the LLRF or issues a signal for switching off of the DC power supplies of the high power RF source.

Trip Logic in FPGA: The state machines based trip logic is implemented in FPGA on every module. The state machine starts on each 'RF ON' trigger Pulse and monitors the trip signal from the signal processing channels and generates a trip request only during this valid RF ON period.

Some signals like forward and reflected power are valid only after cavity fill period and hence state machines on these cards waits for the appropriate cavity fill duration before it acknowledges a trip signal from the corresponding signal processing channels. The trip signals from all the modules are monitored by system control board and it responds by generating 'RF_INH' signal which blocks the LLRF signal temporarily and will be made on again. The RFPI will issue a Beam off signal also which will be used to stop the ion source output. If the fault is observed for three consecutive cycles, the LLRF output will be blocked and the channel state machine generates 'DC-INH' signal from system control board, which will be used to switch off DC power supplies of High power RF source till the fault is analyzed and repaired.

Each channel in the modules has two comparators, which compare the input signal to the reference value and issues a trip if the input crosses the trip limit. The "Soft limit" is set via the operator console into the FPGA, which in turn loads it to the DAC in real time. The second limit i.e. "Hard Limit" is settable locally and is usually kept higher than the soft limit. The local control is required to facilitate ease of testing and troubleshooting during the conditioning modes.

Advantages of Mezzanine card approach

A conceptually new design wherein the common cPCI carrier board which accommodates 128MB DDR2 Memory, cPCI interface and digital glue logic and the mezzanine board which accommodates the ADC, comparator section and the analog and RF sections that are unique to each module has been designed.

The mezzanine card approach has following advantages

1) It allows rapid development of new hardware as well as up-gradation of existing hardware, as only the mezzanine card needs to be designed.
2) It reduces the development cost and the design cycle by re-using field proven older base boards.
3) It facilitates easy migration to newer platforms, as only the new base board needs to be designed.
4) Quick and easy repairs as well as lower inventory cost because of module level repairs.

The mezzanine card connector supports high speed differential signals; low speed digital signals, single ended analog signals, and differential analog signals in addition to various busses like I2C, SMBUS, SPI, and JTAG used by ADC, DAC and CPLD on the mezzanine board.

The mezzanine card is 76 mm height (along the fascia) and 120 mm depth as shown in fig.11. The mezzanine card bezel is flushed with main fascia for EMI shielding integrity. The board to board air gap of 5 mm (as shown in fig 12) offers better signal integrity for the connector.

Fig.11.Rear view of the Mezzanine card

Fig.12. Side view of the mezzanine card assembly

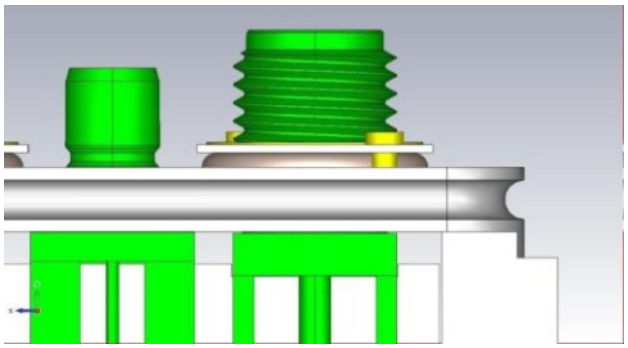


Fig.13. close-up cut section view of SMA connector

Cable sense detection

The reliability of the RFPI is very much dependent on the quality of cable contacts as poor cable contacts, especially on the ground side could lead to false triggering of the corresponding channel.

Cable sense assembly shown in fig.13.has been designed and incorporated in the RFPI for electrically detecting proper tightening of the SMA plug on to the SMA connector
The cable sense assembly consists of a PCB having a circular copper area which mates with the bottom contact of the SMA plug. Under normal condition, the cable sense PCB floats at VCC (3.3V) via a pull up resistor. When the SMA plug (which is at ground potential) connects with the cable sense PCB, it pulls the PCB potential to ground. This change in the cable sense PCB is detected by the cable sense electronics. A size 10 silicon rubber O-ring provides the counter pressure to the PCB against tightening and ensures that the PCB contact is always under positive pressure

Software Features of the RF Protection Interlock System

The RFPI has the following features to assist the user on the operator console
During Normal Operation

1) Display the status of each channel on each board by name and system it monitors
2) Upon power up or on user request sends a reset command to the system control board which propagates the signal to the rest of the boards.
3) LOCAL/REMOTE mode of operation of the RFPI which decides whether the comparator trip point is set by the DAC or by the front panel pot is selected for each channel on each board
4) Set the trip level of each comparator in each channel when operating in REMOTE mode.
5) Compare the MANUAL and REMOTE thresholds and indicate to the user in via alarm or warning that his setting is out of tolerance with respect to the MANUAL mode.
6) Allow the user to change the comparator threshold when in REMOTE mode during operation.
7) The control system should be able to read the process status word from the system control and display this status on a parameter page.
8) It should read the process status word from each of the boards in the interlock system at the request of a user.
9) It should read the digitized analog signal from memory and display the data for the user for the fault analysis.

During Trip condition
The RFPI should support the following functions during a trip operation

1) Read the process status word from the system control board to determine which board originated the trip, and then display it on the parameter page.
2) Read the process status word from the board where the trip originated to find out which channel originated the trip and then display it on the parameter page.
3) Read out the post-mortem memory corresponding to the trip channel and other channels associated with the trip.
4) Set an alarm once the trip has occurred.
5) Change the trip level for that channel as dictated by the system state machine.
6) Display if the LLRF is being inhibited. This occurs when the RF is held off but not permanently inhibited.

The VME64X based RF Protection Interlock (RFPI) system consists of 6U form factor system having multiple modules. The RFPI system consists of following functional modules a) multi-trip module, b) Photo Multiplier Module (PMT), c) Field Emission Module (FEP), d) System Control Module and e) photo diode module.
Each module consists of the following types of cards. Two types of carrier boards i.e. VME carrier board and rear I/O carrier board and four mezzanine cards. Rear analog I/O mezzanine card and rear digital I/O mezzanine card are mounted on rear I/O carrier board. Two function specific mezzanine cards are mounted on VME carrier board. Detail component breakup of each module is given in annexure III.

All the modules in the RFPI system are 6U, VME64X form factor modules having a rear I/O card. The modules have analog sections which are unique to each card and digital sections that are common to all the modules. The digital section like interlock logic, FPGA, DDR3 Memory and the VME interface are on the base board (VME carrier board), which is common to all the RFPI modules. It also has provisions for various power supplies and filters that are required by the carrier board as well as mezzanine boards. The unique functionality of each module is migrated on to the mezzanine board which are populated on VME base board. The VME base board has two such mezzanine cards (M1 and M2). The module also has a rear I/O card for interfacing the field and control signals. This rear I/O has 2 Mezzanine card for interfacing to slow speed analog and digital signals. One rear mezzanine card (M3) has 16 Digital Inputs and 16 Digital Outputs which are isolated. The second rear Mezzanine module (M4) has eight analog input and eight analog output channels. Architecture of the module is as shown below in fig.14.

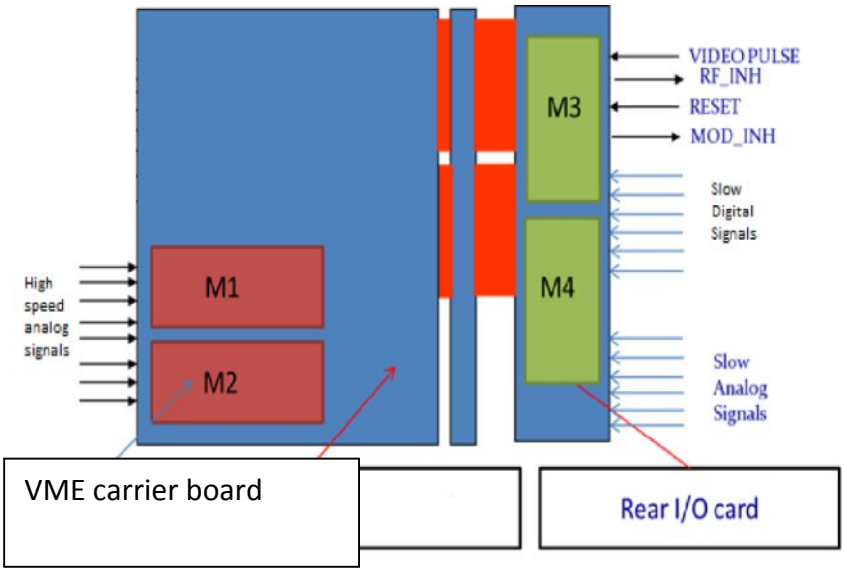


Fig.14. Architecture of VME module with mezzanine card and rear I/O card.

Each mezzanine card on VME64 carrier board has four independent channels and one ADC having four inputs of 80MSPS. Each carrier board has an FPGA for implementing the trip logic and 256MB DDR3 memory interfaced to FPGA. Three sets of following modules are required to be developed, fabricated and delivered as part of the RFPI system.

Different modules of The RFPI system

1) Multi Trip module: - This module monitors the forward and reflected RF power at various points in the system. The RF signal is fed to a log amplifier for processing and its output is then compared against a local set point as well as DAC controlled set point. The multi-trip module consist of

a) Common VME carrier board: - This board has VME interface, glue logic, 256MB DDR3 Memory, Altera FPGAs for implementing trip logic and VME interface. This board also has a rocket IO connector which utilises the PCIe (1x, 4x, 8x) hard IP core available in Aria2 FPGA. The bus interface glue logic is required for 5V to 3.3V logic conversion.

The front panel fascia has LEDs for displaying status of some events and monitoring terminals. The carrier board also has provisions for various power supplies and filters that are required by the carrier board as well as mezzanine boards. This board is common to all RFPI modules.

b) Rear I/O carrier card: - This board handles all the cabling connections which enter the system from the rear side. It also has provisions for two mezzanine cards, one mezzanine slot (M3) is populated with rear digital mezzanine card and the other one (M4) is populated with rear analog mezzanine card. This board is common to all RFPI modules.

c) Rear Digital Mezzanine card: - The rear digital mezzanine card is mounted on M3 Slot only. The input and output signal grounds are isolated from VME ground. It has sixteen digital inputs and sixteen digital outputs. This board monitors the status of various field parameters like potential free contact signals as well as active status signals. This board also generates command and actuation signals for various field signals. The trip logic is dependent on nature of the signal and is implemented in FPGA. This board is common to all RFPI modules.

d) Rear Analog Mezzanine card: - The rear analog mezzanine card is mounted on M4 slot only. Provisions to isolate the input and output signal grounds from VME ground is to be provided using DC to DC converters. It has eight low speed analog inputs and eight low speed analog outputs. This board monitors the status of various analog field parameters like temperature, flow rate, pressure, analog voltages and currents. This board can also generate analog set points for various systems. The ADC and DAC used are low speed 1MSPS devices. The trip logic is dependent on nature of the signal and is implemented in FPGA. This board is common to all RFPI modules.

e) Multi-trip Mezzanine card: - Two nos. of multi-trip mezzanine cards are populated on VME carrier boards. Each multi-trip mezzanine card has four channels of analog processing electronics specific to multi-trip card. All the channels are digitised using a four channel 80MSPS 14bit ADC. It also has two comparators per channels for trip setting. The trip limit of one comparator is controlled by a local trim pot, whereas the other one has its reference controlled by a 16 bit DAC. The card also has two additional comparators for monitoring the cable connection and fault identification.

2) Photomultiplier Tube (PMT) protection module: -

The PMT module consists of

a) Common VME carrier board: - Identical to the one described in multi trip module section.

b) Rear I/O carrier card: - Identical to the one described in multi trip module section.

c) Rear Analog Mezzanine card: - Identical to the one described in multi trip module section.

d) Rear Digital Mezzanine card: - Identical to the one described in multi trip module section.

e) PMT Mezzanine card: - Two nos. of PMT mezzanine cards are populated on VME carrier boards. Each PMT mezzanine card has four channels of analog processing electronics of the PMT output current. All the channel outputs are digitised using a four channel 80MSPS 14bit ADC. It also has two comparators per channels for trip setting. The trip limit of the comparators is controlled by a local trim pot.

3) Field Emission Probe (FEP) protection module: -. The FEP module consist of

a) Common FEP carrier board: - identical to the one described in multi trip module section.

b) Rear I/O carrier card: - identical to the one described in multi trip module section.

c) Rear Analog Mezzanine card: - identical to the one described in multi trip module section.

d) Rear Digital Mezzanine card: - identical to the one described in multi trip module section.
e) FEP Mezzanine card: - Two nos. of FEP mezzanine cards are populated on VME carrier boards. Each FEP mezzanine card has four channels of analog processing electronics specific to FEP card. All the channels are digitised using a four channel 80MSPS 14bit ADC. It also has two comparators per channels for trip setting. The trip limit of one comparator is controlled by a local trim pot, whereas the other one has its reference controlled by a 16 bit DAC.

4) System Control (SC) Module: - The SC module generates all the timing signals for starting and synchronizing various state machines running on protection cards. The SC module consist of
a) Common VME carrier board: - identical to the one described in multi trip module section.
b) Rear I/O carrier card: - identical to the one described in multi trip module section.
c) Rear Analog Mezzanine card: - identical to the one described in multi trip module section.
d) Rear Digital Mezzanine card: - identical to the one described in multi trip module section.
e) SC Mezzanine card: - Two SC mezzanine cards are populated on VME carrier boards. Each SC mezzanine card has electronics specific to System control card.

5) Photo diode Module: - The photo diode module processes the output of a photo diode for arc detection. The output voltage after suitable amplification is compared with a ref voltage which is set by trim-pots or a 16 bit DAC. The card also has two additional comparators for monitoring the cable connection and fault identification.
a) Common VME carrier board: - identical to the one described in multi trip module section.
b) Rear I/O carrier card: - identical to the one described in multi trip module section.
c) Rear Analog Mezzanine card: - identical to the one described in multi trip module section.
d) Rear Digital Mezzanine card: - identical to the one described in multi trip module section.
e) Photo diode Mezzanine card: - Two photo diode cards are populated on VME carrier boards. Each mezzanine card has electronics specific to photo diode module

Mechanical Design details
The mezzanine cards are connected to the host board through Samtec connectors. Samtec make connector QTH-90-01-L-D-A will be used as mezzanine card Header. The VME carrier card PCB is on the lower side. The mezzanine card is the upper PCB. The green connector between Mezzanine card and VME card is the Samtec connector (HSMC connector in fig.15.) which separates the boards by 5mm.
Mechanical Dimensions of Mezzanine card on the VME carrier board: - The mezzanine card is 76 mm height (along the facia) and 120 mm depth. The mezzanine card bezel is flushed with main facia for EMI shielding integrity. The rear side view of the Mezzanine card is shown in fig. 11. The mounting holes are provided on the mezzanine cards and the host board for better mechanical support to the mezzanine card. The board to board air gap of 5 mm (as shown in fig.15) offers better signal integrity for the connector.

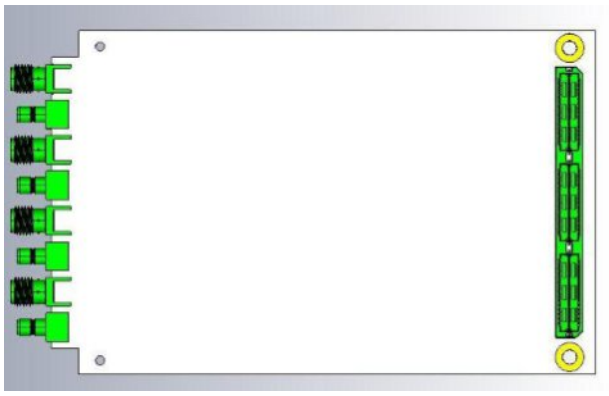


Fig.15.Rear view of the Mezzanine card

VME Host Board Layout: - The Samtec connectors on the mezzanine card is to be located on the edge of the PCB to minimize the keep-out area required on both, the host boards and the mezzanine card. The components are mounted on top side of the mezzanine card and the QTH header is mounted on the bottom surface of the card. The connectors are placed sufficiently away from the board's edge to allow for two mounting holes. This ensures a rigid connection between the host board and mezzanine card.

Mezzanine card mounting arrangement: - The mezzanine card is mounted on the host board via three pairs of screws. Two pairs of M 2.5 screws are mounted at the rear end of the card (one pair each next to Samtec connector). The card top side is fixed on to a standard PMC bezel (as shown in fig.16) using two nos. of M 2.5 mounting screws. The bezel is fixed in the fascia using a silicon rubber O-ring, which also provides EMI shielding. The O-ring grove on bezel is visible in the Fig. 16. The SMA and SMB connectors are flush mounted to the bezel.

Fig.16. Mezzanine card mounting at bezel end

Facia mechanical arrangement: - The front view of facia is shown in fig.17. The cutaway sections houses mezzanine card bezel. The 5X7 LED connector is visible on left hand side. The space between bezel and LED will house card specific connectors and potentiometers and test points for setting up the trip limit.

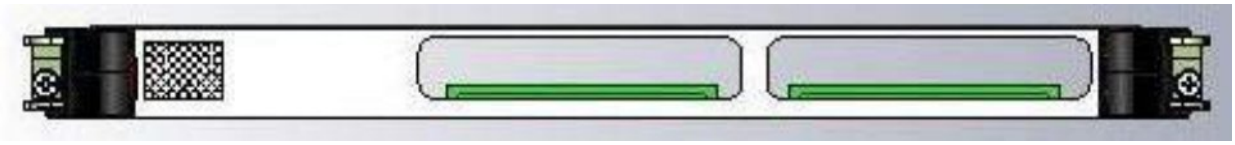


Fig.17. Front view of Facia

Cable Sense assembly: - The cable sense assembly detects proper tightening of the SMA plug on to the SMA connector and generates an electrical signal accordingly. Each SMA connector should have a cable sense assembly.

Functional Block Diagrams of different Modules

The part numbers given in the block diagrams below are indicative only. Any functionally compatible parts can be used with the consent of the indenter, if required.

1. Description of one RF channel of multi trip module: - Four identical RF channels are to be incorporated on each mezzanine card. Each channel is to be shielded separately so as to avoid EMI problems. The RF channel includes log amplifier for RF to DC conversion, buffers and comparators as per the block diagram shown in fig.18.

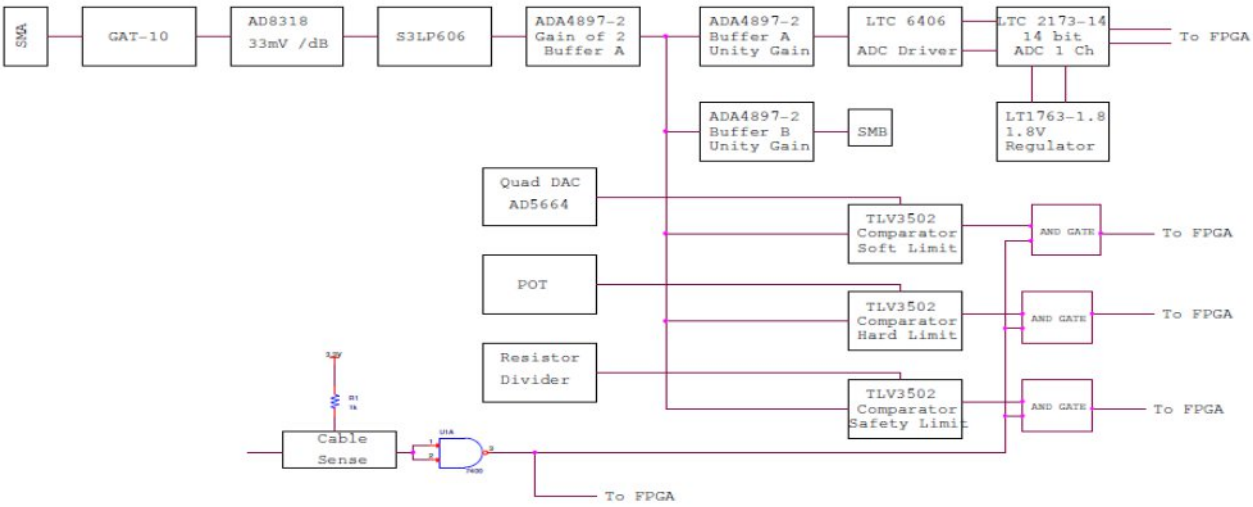


Fig.18. Block Diagram of one multi trip Channel

The signal from forward as well as reflected power detectors is fed to attenuators before processing by log amplifier section. The RF envelop is digitised by LTC 2173-14, a Quad Channel, 80MSPS, 14 bit ADC from Linear Technology. The envelop amplitude is also compared against 3 references; when the input exceeds the set limit, a trip signal is generated. The cable sense circuit is used for detecting whether a cable is connected to the SMA input. The signals going to FPGA are terminated on Samtec connector.

2. Description of one PMT processing channel: Four identical PMT processing channels are to be incorporated on each mezzanine card. Each channel is to be shielded separately so as to avoid EMI problems.

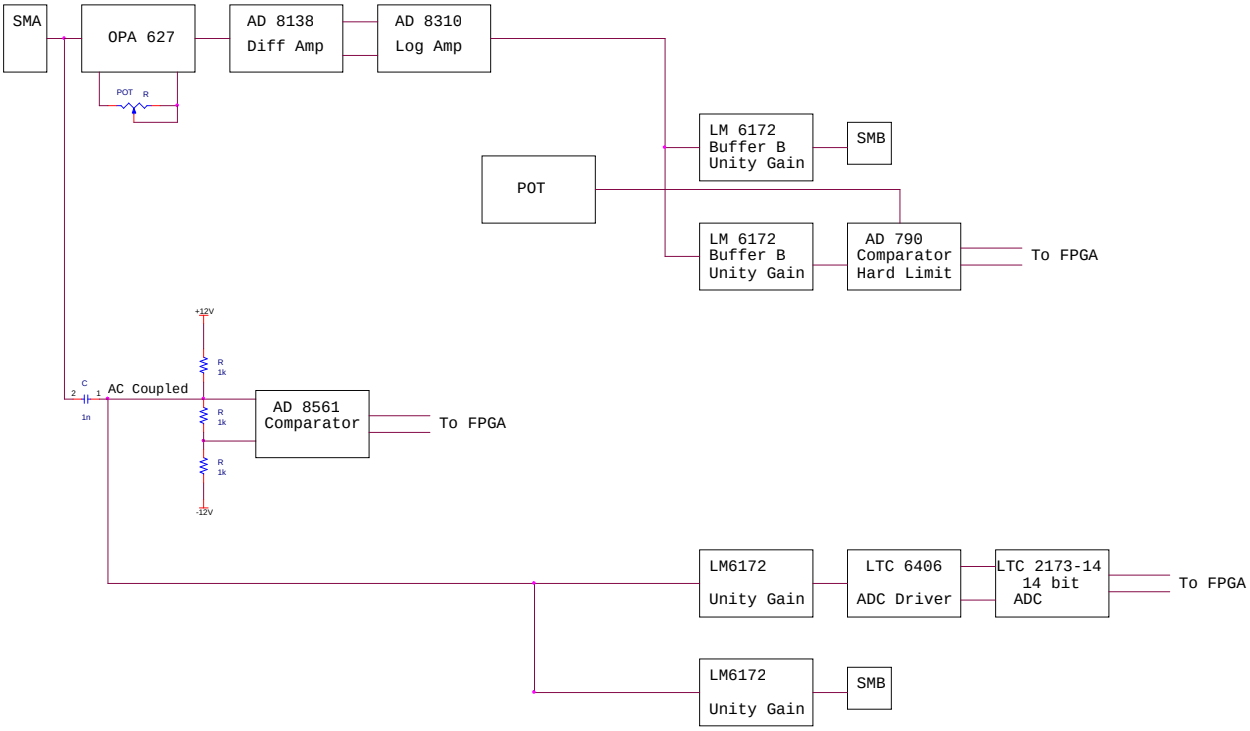


Fig.19. Block Diagram of PMT processing Channel

The signal from PMT detectors is processed by this channel and is shown in fig.20. It has a differential log amplifier and comparator section which monitors the amplitude of PMT leakage current and generates a trip when the limit is crossed. The second section of this PMT channel is monitoring the PMT pulses and generates a trip when pulse amplitude exceeds the set limit. The RF envelop is digitised by LTC 2173-14, a Quad Channel, 80MSPS 14 bit ADC from Linear Technology. When the input exceeds the set limit, a trip signal is generated. The cable sense circuit is used for detecting whether a cable is connected to the SMA input. The signals going to FPGA are terminated on Samtec connector.

30. Description of one FEP channel: Four identical FEP channels are to be incorporated on each mezzanine card. Each channel is to be shielded separately so as to avoid EMI problems. The FEP channel produces the bias voltage (approx. 30V, adjustable) for the probe. As field emission takes place, a voltage gets developed at the output of LM6171. This voltage is processed using buffers and comparators as per the block diagram shown in fig.20.

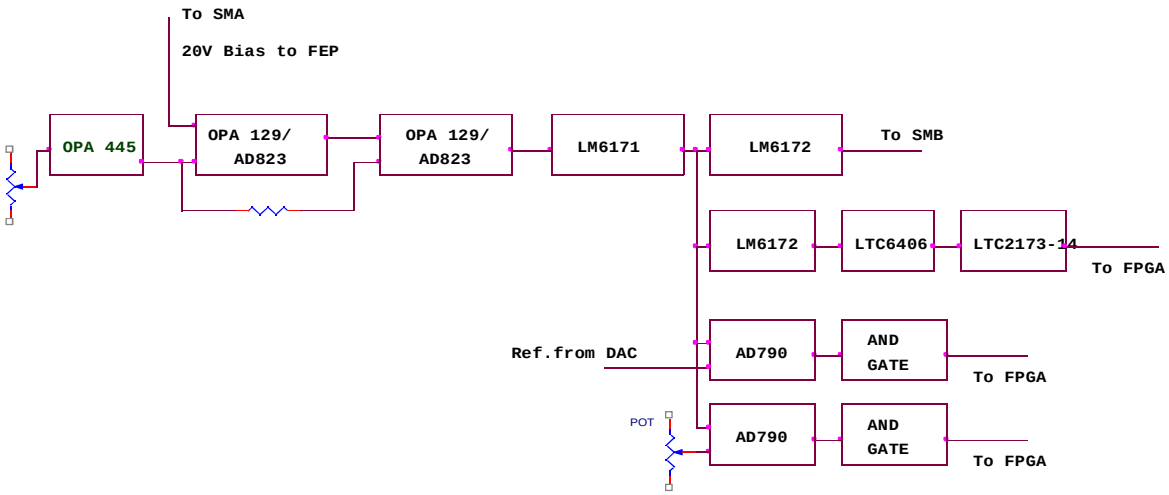


Fig.20. Block Diagram of one FEP output processing Channel

The FEP signal is digitised by LTC 2173-14, a Quad Channel, 80MSPS 14 bit ADC from Linear Technology. The amplitude is also compared against 2 references; when the input exceeds the set limit, a trip signal is generated. The cable sense circuit is used for detecting whether a cable is connected to the SMA input. The signals going to FPGA are terminated on Samtec connector.

Description of System control module: The SC module process the trip signals from various modules. The base board of system control module accommodates two mezzanine cards. One section of the system control board is same as one channel of multi trip board. The other sections on the card includes a video channel section which has a comparator stage which converts digital pulses coming externally to LTTL signal. The card also accommodates buffers and comparators for processing external signals.

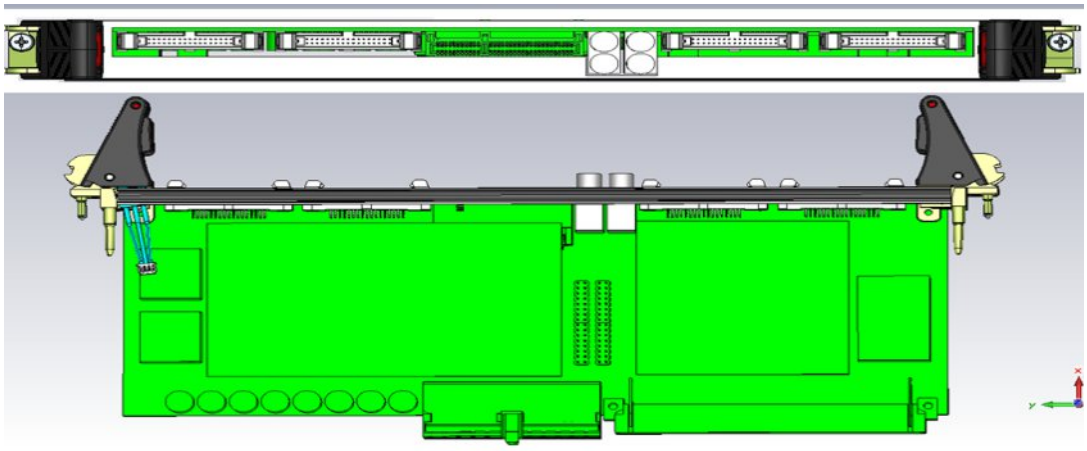


Fig.no.21. Rear carrier board with back panel

The back panel of the rear I/O carrier board will accommodate four nos. of 32 pin FRC connectors as given in the BOM so as to accommodate the field signals

MODULE 1

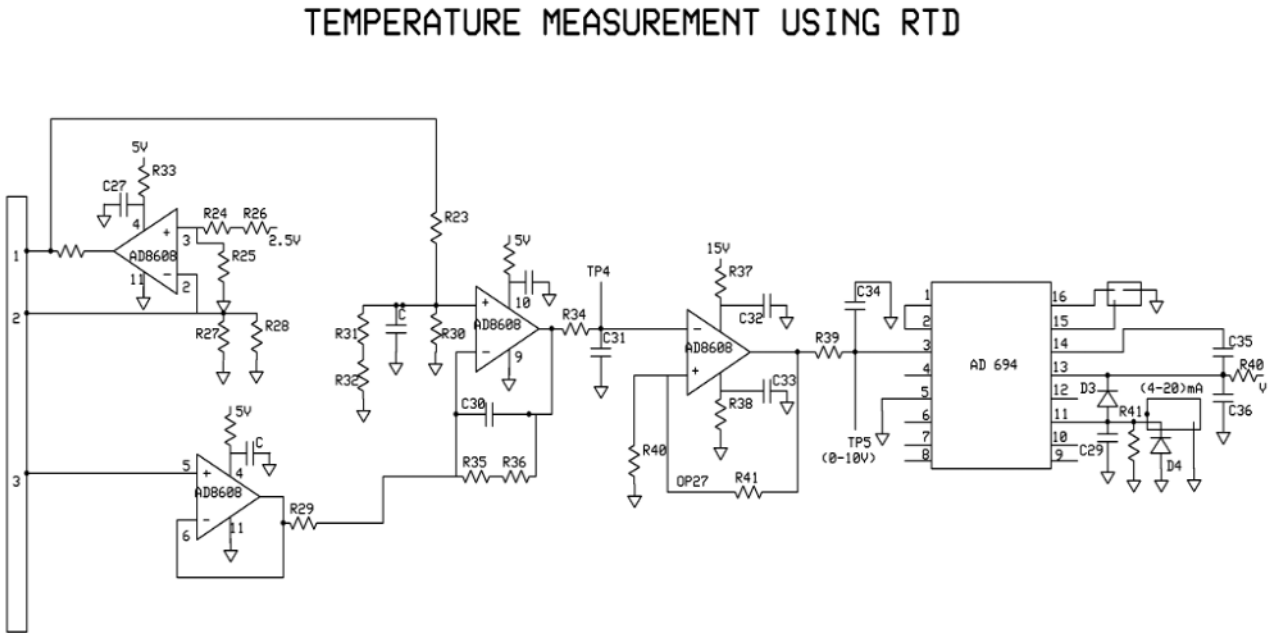


FIG.NO. 22

CIRCUIT DESCRIPTION

The input stage of the circuit is an RTD signal conditioning circuit using a compensated 3-wire connection to the RTD. The circuit translates the RTD input resistance range (100 Ω to 212.05 Ω for a 0°C to 300°C temperature range) into voltage levels compatible with the input range of the ADC (0 V to 2.5 V). The excitation current for the RTD is supplied by op amp U1C that is one-fourth of the quad AD8608. A reference voltage, VR, of 100 mV is developed by the R8/R9 divider driven by the 2.5 V ADC reference. This in turn produces an RTD excitation current of VR/(R1||R2), approximately 1.05 mA. The excitation current produces a voltage change of approximately 117.6 mV (105 mV to 222.6 mV) across the RTD for a temperature change of 0°C to 300°C.

The U1A op amp amplifies this voltage change by 19.6, producing an output span of 2.3 V. Resistor R2 added in parallel with Resistor R1 shifts the output range so that the U1A op amp output is 0.1 V to 2.4 V, which matches the input range of the ADC (0 V to 2.5 V) with 100 mV headroom to maintain linearity. The resistor values can be modified to accommodate other popular temperature ranges as described later in this circuit note. The circuit design allows single supply operation. The minimum output voltage specification for the AD8608 is 50 mV for a 2.7 V power supply and 290 mV for a 5 V power supply with 10 mA load current, over the temperature range of −40°C to +125°C.

A minimum output voltage of 45 mV to 60 mV is a conservative estimate for a 3.3 V power supply, a load current of less than 1 mA, and a narrower temperature range. Considering the tolerances of the parts, the minimum output voltage (low limit of the range) is set to 100 mV to allow for a safety margin. The upper limit of the output range is set to 2.4 V in order to give 100 mV headroom for the positive swing at the ADC input. Therefore, the nominal output voltage range of the op amp is 0.1 V to 2.4 V.

The op amp U1B is used to buffer the internal 2.5 V voltage reference of the AD7091R (U3) ADC. The quad AD8608 op amp is chosen for this application because of its low offset voltage (75 µV maximum), low bias current (1 pA maximum), and low noise (12 nV/√Hz maximum). Power dissipation is only 18.5 mW on a 3.3 V supply. The U1D op amp provides the 3-wire correction signal that compensates for the errors produced by the lead resistances r1 and r2. The gain from Point A to TP1 is +19.6, and the gain from Point B to TP1 is −39.2. The voltage at Point A includes a positive error term that is equal to the voltage dropped across r1 and r2. The voltage at Point B contains a positive error term equal to the voltage dropped across r2, neglecting the small drop across r3.

Because the gain from Point B to TP1 is negative and twice the gain from Point A to TP1, the errors due to the voltages dropped across r1 and r2 are cancelled, assuming that r1 = r2. A single-pole RC filter (R11/C9) follows the op amp output stage to reduce the out-of-band noise. The cut-off frequency of the RC filter is set to 664 kHz. Additional second order filters (adding capacitors C10 and C11) are used for reducing the filter cut-off frequency in case of low frequency industrial noise. In this case, AD7091R is not operating at maximum throughput rate. To increase the conversion speed C10 and C11 should be left unpopulated. The AD7091R 12-bit 1 MSPS SAR ADC is chosen because of its ultralow power 349 µA at 3.3 V (1.2 mW) which is significantly lower than any competitive ADC currently available in the market. The AD7091R also contains an internal 2.5 V reference with ±4.5 ppm/o C typical drift.

The input bandwidth is 7.5 MHz, and the high speed serial interface is SPI compatible. The AD7091R is available in a small footprint 10-lead MSOP. The total power dissipation of the circuit (excluding the ADuM5401 isolator) is approximately 20 mW when operating on a 3.3 V supply. Galvanic isolation is provided by the ADuM5401 (C Grade) quad channel digital isolator. In addition to the isolated output data, the ADuM5401 also provides isolated +3.3 V for the circuit. The ADuM5401 is not required for normal circuit operation unless isolation is needed. The ADuM5401 quad-channel, 2.5 kV isolators with integrated dc-to-dc converter, is available in a small 16-lead SOIC. Power dissipation of the ADuM5401 with a 7 MHz clock is approximately 140 mW. The AD7091R requires a 50 MHz serial clock (SCLK) to achieve a 1 MSPS sampling rate. However, the ADuM5401 (C-grade) isolator has a maximum data rate of 25 Mbps that corresponds to a maximum serial clock frequency of 12.5 MHz.

In addition, the SPI port requires that the trailing edge of the SCLK clock the output data into the processor, therefore the total round-trip propagation delay through the ADuM5401 (120 ns maximum) limits the upper clock frequency to 1/120 ns = 8.3 MHz. Even though the AD7091R is a 12-bit ADC, the serial data is formatted into a 16-bit word to be compatible with the processor serial port requirements.

The sampling period, TS, therefore consists of the AD7091R 650 ns conversion time plus 58 ns (extra time required from data sheet, t1 delay + tQUIET delay) plus 16 clock cycles for the SPI interface data transfer. TS = 650 ns + 58 ns + 16 × 120 ns = 2628 ns fS = 1/TS = 1/2628 ns = 380 kSPS. In order to provide a safety margin, a maximum SCLK of 7 MHz and a maximum sampling rate of 300 kSPS is recommended. The digital SPI interface can be connected to the microprocessor evaluation board using the 12-pin Pmod compatible connector (Digilent Pmod Specifications).

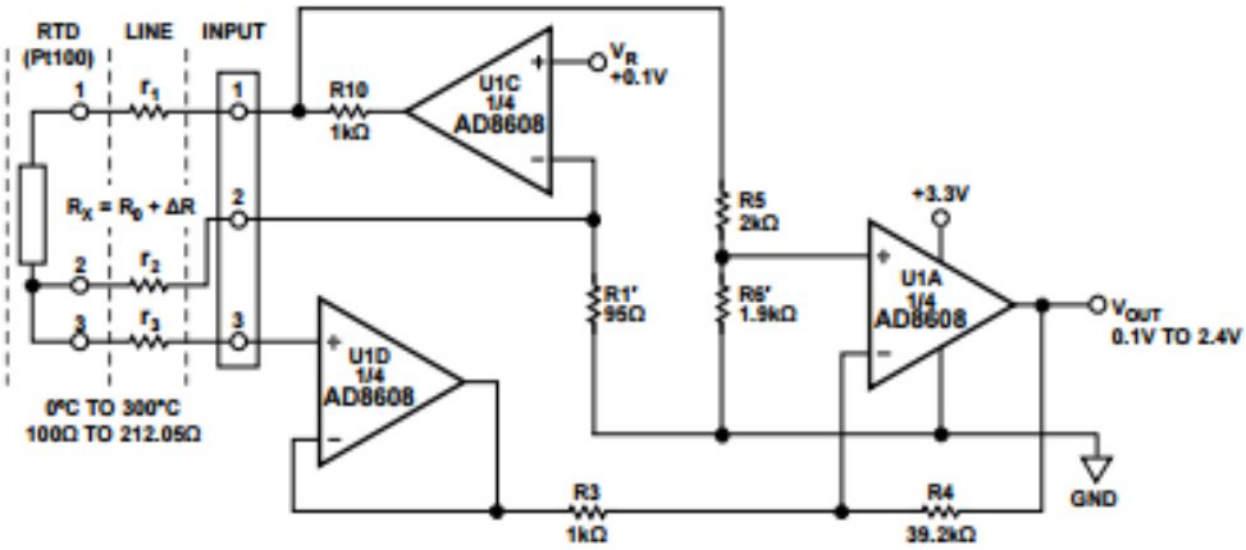


FIG.NO.23. RTD SIGNAL CONDITIONING USING A 3-WIRE CONNECTION

Circuit Design

The circuit shown in Figure 2 converts the RTD resistance change from 100 Ω to 212.05 Ω to an output voltage change of 0.1 V to 2.4 V, which is compatible with the ADC input range. In addition, the circuit removes the errors associated with the wiring resistances r1 and r2. The transfer function of the circuit in Figure 2 is obtained using the superposition principle:

$$V_{OUT} = \frac{V_R}{R1'}(r_1 + R_X + r_2 + R1')\frac{R6'}{R5 + R6'}\left(1 + \frac{R4}{R3}\right) - \frac{V_R}{R1'}(r_2 + R1')\frac{R4}{R3} \quad (1)$$

Where,

$R_X = R_0 + \Delta R$

$R1' = R1||R2 = R_0$, $R6' = R6||R12$

$r_1 = r_2$, and neglects the voltage drop across r_3.

Expand Equation 1, set the term containing r1 to zero, and solve for R6':

$$R6' = R5\frac{R4/R3}{2+R4/R3} \qquad (2)$$

Meeting the criteria in Equation 2 removes the error due to the lead resistances, r1 = r2, (r3 is not taken into account because it is connected to the high impedance input of U1D). Substituting Equation 2 into Equation 1, obtain the transfer function:

$$V_{OUT} = \frac{V_R}{2R_0}\times\frac{R4}{R3}\Delta R \qquad (3)$$

Equation 3 shows that the lead wire resistance is fully compensated provided Equation 2 is met. The gain is set to the desired value by adjusting the ratio of R4/R3.

Calculation of the Gain, Output Offset, and Resistor Values and Tolerances:

For temperature range of 0°C to 300o C, the RTD Pt100 resistance range is 100 Ω to 212.05 Ω, and the input resistance change, ΔR, for the circuit in Figure 2 is 0 Ω to 112.05 Ω. Therefore, the gain of the circuit from Equation 3 is:

$$Gain = \frac{V_R}{2R_0}\times\frac{R4}{R3} = \frac{V_{OUT}}{\Delta R} = \frac{2.4\,\text{V}-0.1\,\text{V}}{112.05\,\Omega-0\,\Omega} = 20.53\,\text{mA} \qquad (4)$$

Assuming that the current through the sensor is equal to 1 mA and R0 = 100 Ω, the required reference voltage V_R is:

$$V_R = 100\,\Omega\times 1\,\text{mA} = 0.1\,\text{V}.$$

Then, Equation 4 is solved for R4/R3:

$$\frac{R4}{R3} = 2\times\frac{100\,\Omega}{0.1\,\text{V}}\times 20.53\,\text{mA} = 41.06$$

Choose R3 = 1 kΩ, then R4 = 41 kΩ.

Choosing a standard value of 2 kΩ for Resistor R5, Resistor R6' can be calculated from Equation 2.

$$R6' = R5\frac{R4/R3}{2+R4/R3} = 2\,\text{k}\Omega\times\frac{41.06}{2+41.06} = 1.907\,\text{k}\Omega$$

An easy way to ensure Equation 2 is met is to use the following relationships:

R5 = 2R3, R6′ = R5||R4, as shown in Figure 1.

If this condition is met, R1′ = R_0 = 100 Ω at 0°C, and V_{OUT} = 0 V.

The output offset of the circuit must now be set to 0.1 V. An easy way to shift the output is to make the resistor R1′ slightly less than R0. Note that this affects the gain proportionally. The output offset of 0.1 V is approximately 4.35% of the total span of 2.3 V, therefore the ratio R1′/R0 must be less than 0.9565.

To keep the high output level equal to 2.4 V, the ratio R4/R3 can be proportionally corrected. For example, R4 = 0.9565 × 41.06 × R3 = 39.27 kΩ. Using standard resistors values as shown in Figure 1, the circuit gives a good approximation to the required gain and the output offset. Resistor R1′ is formed by connecting Resistor R2 = 1.91 kΩ in parallel with resistor R1 = 100 Ω.
Equation 1 shows that all resistors influence the total error. If these values are chosen carefully, the overall error due to substituting standard value resistors can be made less than a few percent. However, use Equation 1 to recalculate the U1A op amp output for 100 Ω and 212.05 Ω inputs to ensure that the required headroom is preserved. In the actual circuit the nearest available standard resistors values were chosen. The Resistors Rl, R2, R8, and R9 are 0.1%, 25 ppm/°C. The other resistors in the circuit are 1%, 100 ppm/°C: R3, R4, R5, R6, and R12.
The absolute accuracy in this type of circuit is primarily determined by the resistors, and therefore gain and offset calibration is required to remove the error due to standard value substitution and resistor tolerances. Effect of Resistor Temperature Coefficients on Overall Error Equation 1 shows that the output voltage is a function of nine resistors: R1, R2, R3, R4, R5, R6, R8, R9, and R12. The sensitivity of the full-scale output voltage at TP1 to small changes in each of the nine resistors was calculated using a simulation program. The input RTD resistance to the circuit was 212 Ω. The individual sensitivities calculated were SR1 = 1.83, SR2 = 0.09, SR3 = 0.94, SR4 = 0.94, SR5 = 1.35, SR6 = 1.28. SR8 = 0.97, SR9 = 0.96, and SR12 = 0.07. Assuming that the individual temperature coefficients combine in a root-sum-square (rss) manner, then the overall full-scale drift 25 ppm/°C resistors for R1, R2, R8, R9, and 100 ppm/°C resistors for R3, R4, R5, R6, R12 is approximately:

Full scale drift

$$= 25\ \text{ppm/°C}\sqrt{[(S_{R1})^2 + (S_{R2})^2 + (4S_{R3})^2 + (4S_{R4})^2 + (4S_{R5})^2 + (4S_{R6})^2 + (S_{R8})^2 + (S_{R9})^2 + (4S_{R12})^2)]}$$

$$= 25\ \text{ppm/°C}\sqrt{(1.83^2 + 0.09^2 + 3.76^2 + 3.76^2 + 5.4^2 + 5.12^2 + 0.97^2 + 0.96^2 + 0.28^2)}$$

$$= 236\ \text{ppm/°C}$$

The full-scale drift of 236 ppm/°C corresponds to 0.024% FSR/°C. For a ±10°C change in temperature, the error is ±0.24% FSR. Using 25 ppm/°C resistors for all nine resistors reduces the full scale drift to approximately 80 ppm/°C, or 0.008% FSR/°C. The error caused by the tolerances of the resistors, the offset of the AD8608 op amps (75 µV), and the ADC AD7091R is

eliminated after the calibration procedure. It is still necessary to calculate and verify that the op amp output is within the required range.
Effect of Active Component Temperature Coefficients on Overall Error The dc offsets of the AD8608 op amps (75 µV) and the AD7091R ADC are eliminated by the calibration procedure. The offset drift of the ADC AD7091R internal reference is 4.5 ppm/°C typical and 25 ppm/°C maximum.
The offset drift of the AD8608 op op-amp is 1 µV/°C typical and 4.5 µV/°C maximum. Note that resistor drift is the largest contributor to total drift if 50 ppm /° C or 100 ppm /° C resistors are used and the drift due to active components can be neglected. Lead Wire Resistance Compensation The circuit in Figure 1 realizes full compensation for the lead wire resistances (r1, r2, and r3). However, if there is any mismatch in Equation 3, the lead wires r1 and r2 add errors to the measurement. The third lead wire r3 does not have any effect on the circuit because it is connected to the high impedance input of U1D. The linearity of the circuit is not affected by the lead wires r1 and r2, even if there is mismatch in Equation 3. RTD Linearization The circuit is linear with respect to the resistance change of the RTD.
However, the transfer function of the RTD (resistance vs. temperature) is nonlinear.
Therefore, linearization is needed to eliminate the nonlinearity error of the RTD. For systems in which a microcontroller is involved, this linearization is typically done in the software. The AN-709 Application Note discusses some linearization techniques for Pt100 RTD sensor. The same techniques are used in the CN0337 evaluation software to eliminate the nonlinearity error of the Pt100 sensor.
PCB Layout Considerations In any circuit where accuracy is crucial, it is important to consider the power supply and ground return layout on the board. The PCB should isolate the digital and analog sections as much as possible. The PCB for this system was constructed in a simple 2-layer stack up, but 4-layer stack up gives better EMS. See the MT-031 Tutorial for more discussion on layout and grounding and the MT-101 Tutorial for information on decoupling techniques. Decouple the power supply to AD8608 with 10 µF and 0.1 µF capacitors to properly suppress noise and reduce ripple. Place the capacitors as close to the device as possible, with the 0.1 µF capacitor having a low ESR value.
Ceramic capacitors are advised for all high frequency decoupling. Power supply lines should have as large trace width as possible to provide low impedance path and reduce glitch effects on the supply line. The ADuM5401 isoPower integrated dc-to-dc converter requires power supply bypassing at the input and output supply pins. Note that low ESR bypass capacitors are required between Pin 1 and Pin 2 and between Pin 15 and Pin 16, as close to the chip pads as possible. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for VDD1 and VISO. The smaller capacitor must have a low ESR, for example, use of a ceramic capacitor is advised. The total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. Consider bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 unless both common ground pins are connected together close to the package.
For more information, see ADuM5401 datasheet.

A complete documentation package including schematics, board layout, and bill of materials (BOM) can be found at www.analog.com/CN0337-DesignSupport. High Voltage Capability This PCB is designed in adherence with 2500 V basic insulation practices.

High voltage testing beyond 2500 V is not recommended. Appropriate care must be taken when using this evaluation board at high voltages, and the PCB should not be relied on for safety functions because it has not been high potential tested (also known as hipot tested or dielectric withstanding voltage tested) or certified for safety.

COMMON VARIATIONS

The circuit is proven to work with good stability and accuracy with component values shown. Other precision op-amps and other ADCs can be used in this configuration to convert resistance deviation input range to digital output and for other various applications of the circuit. The circuit in Figure 1 can be redesigned for other than 0°C to 300o C input temperature ranges, following the recommendations given in Circuit Design section. Table 1 shows calculations for some standard temperature ranges when using Pt100 RTD sensors

Temperature Range	R1	R2	R4, R12
–50°C to 50°C	79.4 Ω	7.82 kΩ	93.1 kΩ
0°C to 50°C	100 Ω	11.7 kΩ	237 kΩ
0°C to 100°C	100 Ω	5.83 kΩ	118 kΩ
0°C to 200°C	100 Ω	2.91kΩ	59 kΩ
0°C to 300°C	100 Ω	1.91 kΩ	39.2 kΩ
0°C to 400°C	100 Ω	1.45 kΩ	29.4 kΩ
0°C to 500°C	100 Ω	1.17 kΩ	23.7 kΩ
0°C to 600°C	100 Ω	976 Ω	19.6 kΩ
0°C to 700°C	100 Ω	837 Ω	16.9 kΩ
0°C to 800°C	100 Ω	723 Ω	14.7 kΩ

TABLE.NO.4. RESISTOR VALUES FOR COMMON TEMPERATURE RANGES

The AD7091 is similar to the AD7091R, but without the voltage reference output, and the input range is equal to the power supply voltage. The AD7091 can be used with a 2.5 V ADR391 reference. The ADR391 does not require buffering. The ADR391 is a precision 2.5 V band gap voltage reference, featuring low power and high precision (9 ppm/°C of temperature drift) in a tiny TSOT package. The AD8605 and AD8606 are single and dual versions of the quad AD8608 and can be used as a substitute for the AD8608, if different configurations are needed. The AD8601, AD8602, and AD8604 are single, dual, and quad rail-to-rail, input and output, single-supply amplifiers featuring very low offset voltage and wide signal bandwidth that can be used in place of AD8605, AD8606, and AD8608.

The AD7457 is a 12-bit, 100 kSPS, low power, SAR ADC, and can be used in combination with the ADR391 voltage reference in place of AD7091R, when a 300 kSPS throughput rate is not needed. CIRCUIT EVALUATION AND TEST This circuit uses the EVAL-CN0337-PMDZ circuit board, the SDP-PMD-IB1Z, and the EVAL-SDP-CB1Z system demonstration platform (SDP) evaluation board.

The SDPPMD-IB1Z interposer board and the EVAL-SDP-CB1Z SDP board have 120-pin mating connectors. The interposer board and the EVAL-CN0337-PMDZ board have 12-pin Pmod matching connectors, allowing quick setup and evaluation of the circuit's performance. The EVAL-CN0337-PMDZ board contains the circuit to be evaluated, as described in this note and the SDP evaluation board is used with the CN0337 evaluation software to capture the data from the EVALCN0337-PMDZ circuit board.

- Equipment Needed
  - PC with a USB port, Windows® XP, Windows Vista® (32- bit), or Windows® 7/8 (64- or 32-bit)
  - EVAL-CN0337-PMDZ circuit evaluation board
  - EVAL-SDP-CB1Z SDP evaluation board
  - SDP-PMD-IB1Z interposer board
  - CN0337 evaluation software
  - Precision Resistance Decade Box or Pt100 sensor (the calibration procedure can be performed if a resistance box is not available)

Getting Started

Load the evaluation software by placing the CN0337 evaluation software disc in the CD drive of the PC. You also can download the most up to date copy of the evaluation software from CN0337 evaluation software. Using the My Computer icon, locate the drive that contains the evaluation software disc and open the setup.exe file. Follow the on-screen prompts to finish the installation. It is recommended to install all software components to the default locations.

Functional Block Diagram

A functional block diagram of the test setup is shown in Figure.

Setup

1. Connect the EVAL-CFTL-6V-PWRZ (+6 V dc power supply) to SDP-PMD-IB1Z interposer board via the de barrel jack.
2. Connect the SDP-PMD-IB1Z (interposer board) to EVALSDP-CB1Z (SDP board) via the 120-pin Connector A.
3. Connect the EVAL-SDP-CB1Z (SDP board) to the PC via the USB cable.
4. Connect the EVAL-CN0337-PMDZ evaluation board to the SDP-PMD-IB1Z interposer board via the 12 header Pmod connector.
5. Connect the resistance decade box (Pt100 sensor) to the EVAL-CN0337-PMDZ evaluation board via the terminal block J2.

Test

Launch the evaluation software. The software can communicate to the SDP board if the Analog Devices System Development Platform drivers are listed in the Device Manager. After USB communications are established, the SDP board can be used to send, receive, and capture serial data from the EVAL-CN0337- PMDZ board. Data can be saved in the computer for various values of the input temperature (resistance).

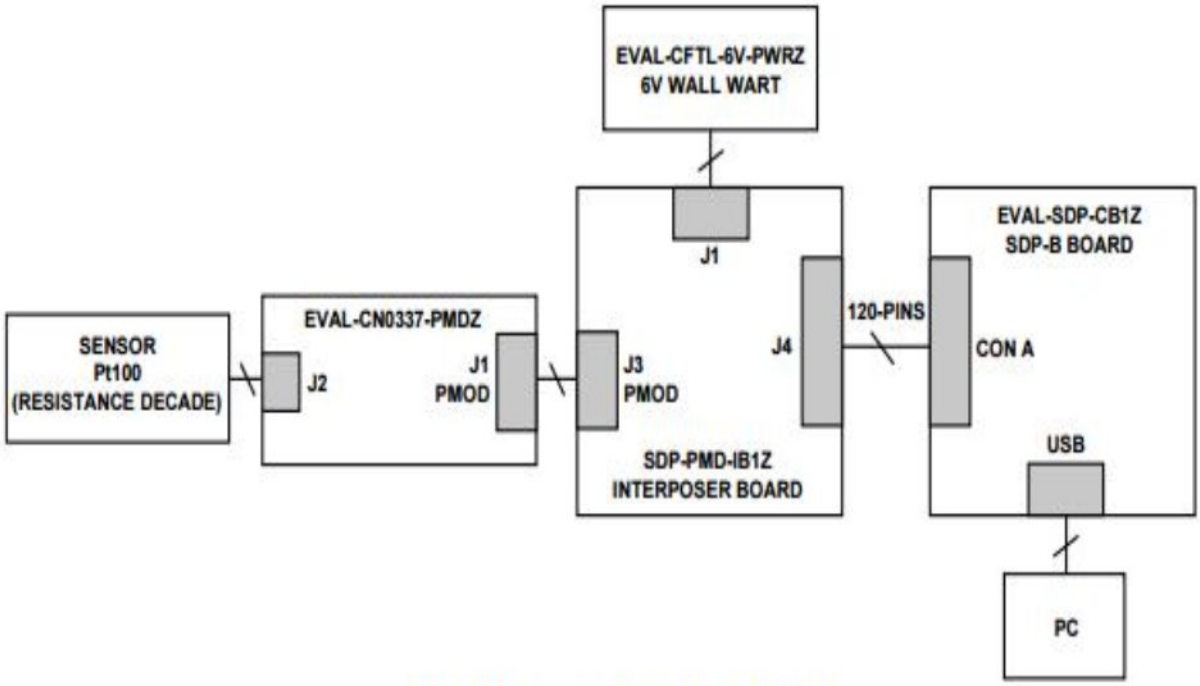


Figure 4. Functional Test Setup Block Diagram

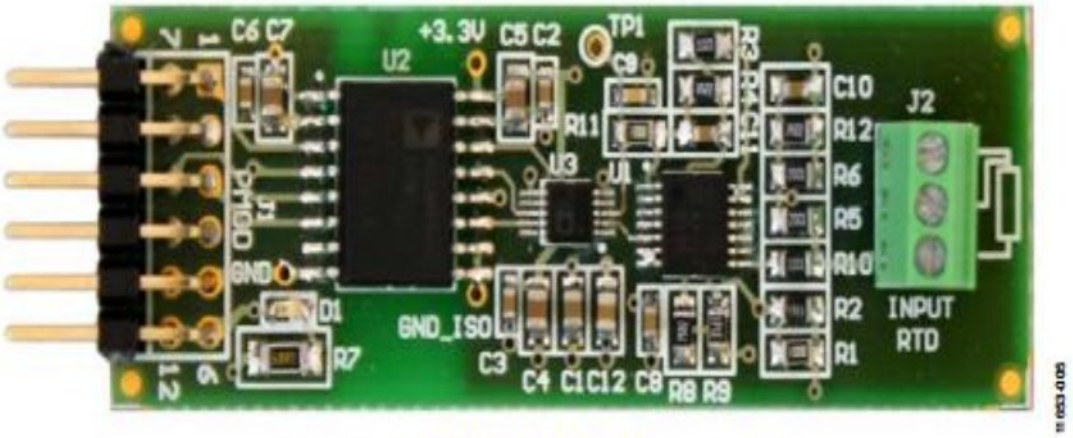


Figure 5. Photo of EVAL-CN0337-PMDZ Evaluation Board

MODULE 2

Description of photo diode:

Each mezzanine card has four identical channels each processing output from a photo diode. Block diagram of the one channel is given in fig.25. The photo diode signal is digitised by LTC 2173-14, a Quad Channel, 80MSPS 14 bit ADC from Linear Technology. The amplitude is also compared against 2 references; when the input exceeds the set limit, a trip signal is generated. The cable sense circuit is used for detecting whether a cable is connected to the SMA input. The signals going to FPGA are terminated on Samtec connector.

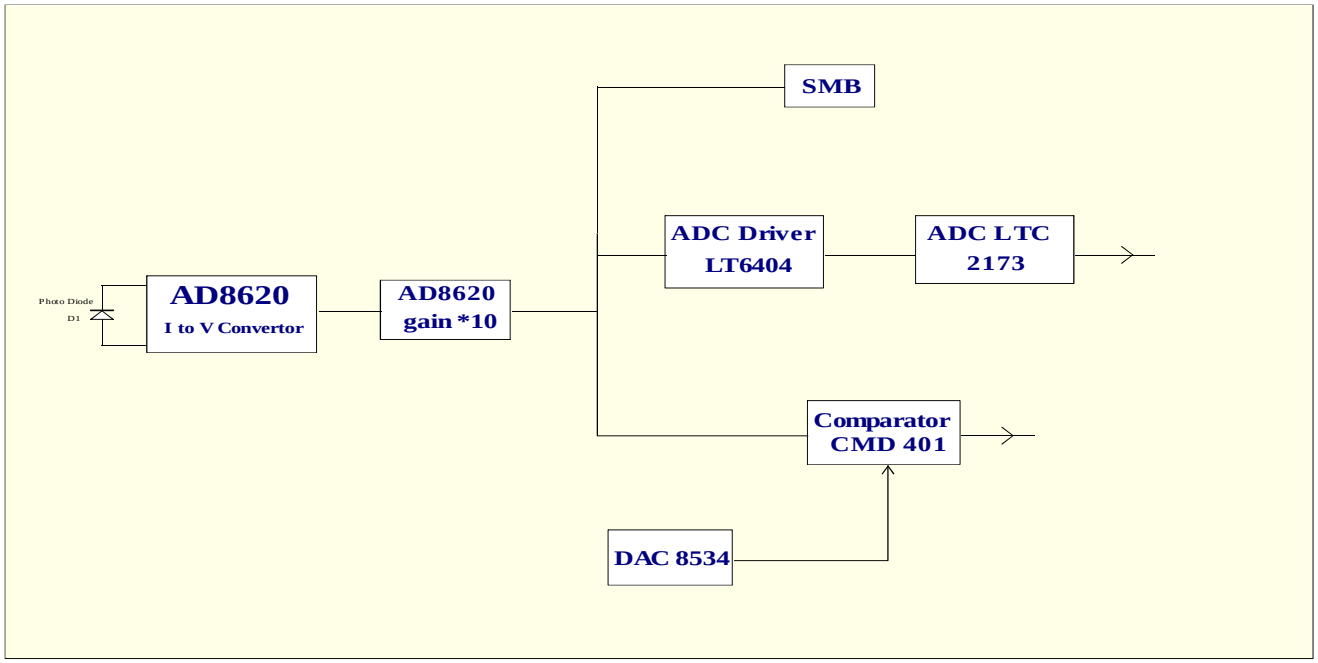


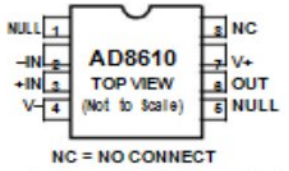
Fig.25. Block Diagram of one photo diode output processing Channel

AD8620

GENERAL DESCRIPTION

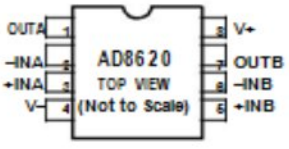
The AD8610/AD8620 are very high precision JFET input amplifiers featuring ultralow offset voltage and drift, very low input voltage and current noise, very low input bias current, and wide bandwidth. Unlike many JFET amplifiers, the AD8610/AD8620 input bias current is low over the entire operating temperature range.

PIN CONFIGURATIONS



NC = NO CONNECT

Figure 1. 8-Lead MSOP and 8-Lead SOIC_N



The AD8610/AD8620 are stable with capacitive loads of over 1000 pF in non-inverting unity gain; much larger capacitive loads can be driven easily at higher noise gains. The AD8610/ AD8620 swing to within 1.2 V of the supplies even with a 1 kΩ load, maximizing dynamic range even with limited supply voltages. Outputs slew at 50 V/µs in either inverting or non-inverting gain configurations, and settle to 0.01% accuracy in less than 600 ns. Combined with high input impedance, great precision, and very high output drive, the AD8610/AD8620 are ideal amplifiers for driving high performance ADC inputs and buffering DAC converter outputs.
Applications for the AD8610/AD8620 include electronic instruments; ATE amplification, buffering, and integrator circuits; CAT/MRI/ultrasound medical instrumentation; instrumentation quality photodiode amplification; fast precision filters (including PLL filters); and high quality audio.
The AD8610/AD8620 is fully specified over the extended industrial temperature range (−40°C to +125°C). The AD8610 is available in the narrow 8-lead SOIC and the tiny 8-lead MSOP surface-mount packages. The AD8620 is available in the narrow 8-lead SOIC package. The 8-lead MSOP packaged devices are avail-able only in tape and reel.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (AD8610B)	VOS			45	100	µV
		−40°C < TA < +125°C		80	200	µV
Offset Voltage (AD8620B)	VOS			45	150	µV
		−40°C < TA < +125°C		80	300	µV
Offset Voltage (AD8610A/AD8620A)	VOS			85	250	µV
		25°C < TA < 125°C		90	350	µV
		−40°C < TA < +125°C		150	850	µV
Input Bias Current	IB		−10	+2	+10	pA
		−40°C < TA < +85°C	-250	+130	+250	pA
		−40°C < TA < +125°C	−2.5	+1.5	+2.5	nA
Input Offset Current	IOS		−10	+1	+10	pA
		−40°C < TA < +85°C	−75	+20	+75	pA
		−40°C < TA < +125°C	-150	+40	+150	pA
Input Voltage Range			−2		+3	V
Common-Mode Rejection Ratio	CMRR	VCM = −1.5 V to +2.5 V	90	95		dB
Large Signal Voltage Gain	AVO	RL = 1 kΩ, VO = −3 V to +3 V	100	180		V/mV
Offset Voltage Drift (AD8610B)	ΔVOS/ΔT	−40°C < TA < +125°C		0.5	1	µV/°C
Offset Voltage Drift (AD8620B)	ΔVOS/ΔT	−40°C < TA < +125°C		0.5	1.5	µV/°C
Offset Voltage Drift (AD8610A/AD8620A)	ΔVOS/ΔT	−40°C < TA < +125°C		0.8	3.5	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	VOH	RL = 1 kΩ, −40°C < TA < +125°C	3.8	4		V
Output Voltage Low	VOL	RL = 1 kΩ, −40°C < TA < +125°C		−4	−3.8	V
Output Current	IOUT	VOUT > ±2 V		±30		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	VS = ±5 V to ±13 V	100	110		dB
Supply Current per Amplifier	ISY	VO = 0 V		2.5	3.0	mA
		−40°C < TA < +125°C		3.0	3.5	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	RL = 2 kΩ	40	50		V/µs
Gain Bandwidth Product	GBP			25		MHz
Settling Time	tS	AV = +1, 4 V step, to 0.01%		350		ns
NOISE PERFORMANCE						
Voltage Noise	en p-p	0.1 Hz to 10 Hz		1.8		µV p-p
Voltage Noise Density	en	f = 1 kHz		6		nV/√Hz
Current Noise Density	in	f = 1 kHz		5		fA/√Hz
Input Capacitance	CIN					
Differential Mode				8		pF
Common Mode				15		pF
Channel Separation	CS					
f = 10 kHz				137		dB
f = 300 kHz				120		dB

TABLE.NO.5. SPECIFICATIONS

THEORY OF OPERATION

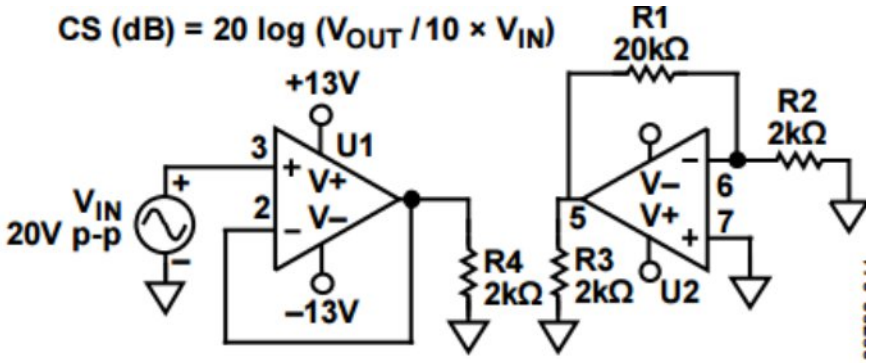


FIG.NO.26. CHANNEL SEPARATION TEST CIRCUIT

FUNCTIONAL DESCRIPTION

The AD8610/AD8620 are manufactured on the Analog Devices, Inc., XFCB (extra fast complementary bipolar) process. XFCB is fully dielectrically isolated (DI) and used in conjunction with N-channel JFET technology and thin film resistors (that can be trimmed) to create the JFET input amplifier. Dielectrically isolated NPN and PNP transistors fabricated on XFCB have an fτ > 3 GHz. Low TC thin film resistors enable very accurate offset voltage and offset voltage temperature coefficient trimming. These process breakthroughs allow Analog Devices IC designers to create an amplifier with faster slew rate and more than 50% higher bandwidth at half of the current consumed by its closest competition.

The AD8610/AD8620 are unconditionally stable in all gains, even with capacitive loads well in excess of 1 nF. The AD8610B grade achieves less than 100 µV of offset and 1 µV/°C of offset drift, numbers usually associated with very high precision bipolar input amplifiers. The AD8610 is offered in the tiny 8-lead MSOP as well as narrow 8-lead SOIC surface-mount packages and is fully specified with supply voltages from ±5.0 V to ±13 V.

The very wide specified temperature range, up to 125°C, guarantees superior operation in systems with little or no active cooling. The unique input architecture of the AD8610/AD8620 features extremely low input bias currents and very low input offset voltage. Low power consumption minimizes the die temperature and maintains the very low input bias current. Unlike many competitive JFET amplifiers, the AD8610/AD8620 input bias currents are low even at elevated temperatures. Typical bias currents are less than 200 pA at 85°C. The gate current of a JFET doubles every 10°C, resulting in a similar increase in input bias current over temperature. Give special care to the PC board layout to minimize leakage currents between PCB traces. Improper layout and board handling generates a leakage current that exceeds the bias current of the AD8610/AD8620.

LT6404

Features

- Fully Differential Input and Output
- Low Noise: 1.5nV/√Hz RTI
- Very Low Distortion:
  LTC6404-1 ($2V_{P-P}$, 10MHz): –91dBc
  LTC6404-2 ($2V_{P-P}$, 10MHz): –96dBc
  LTC6404-4 ($2V_{P-P}$, 10MHz): –101dBc
- Closed-Loop –3dB Bandwidth: 600MHz
- Slew Rate: 1200V/µs (LTC64044)

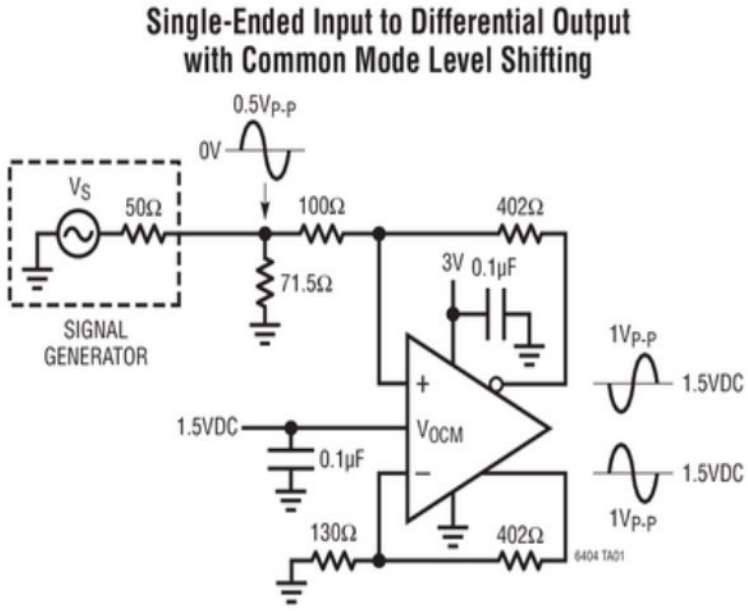


FIG NO.27

- Adjustable Output Common Mode Voltage
- Rail-to-Rail Output Swing
- Input Range Extends to Ground
- Large Output Current: 85mA (Typ)
- DC Voltage Offset < 2mV (Max)
- Low Power Shutdown
- Tiny 3mm × 3mm × 0.75mm 16-Pin QFN Package

Description

The LTC6404 is a family of AC precision, very low noise, low distortion, fully differential input/output amplifiers optimized for 3V, single supply operation. The LTC6404-1 is unity-gain stable. The LTC6404-2 is designed for closed-loop gains greater than or equal to 2V/V. The LTC6404-4 is designed for closed-loop gains greater than or equal to 4V/V. The LTC6404 closed-loop bandwidth extends from DC to 600MHz. In addition to the normal un-filtered outputs (OUT+ and OUT–), the LTC6404 has a built-in 88.5MHz differential single-pole low-pass filter and an additional pair of filtered outputs (OUTF+, OUTF–). An input referred voltage noise of 1.5nV/√Hz make the LTC6404 able to drive state-of-the-art 16-/18-bit ADCs while operating on the same supply voltage, saving system cost and power. The LTC6404 is characterized, and maintains its performance for supplies as low as 2.7V and can operate on supplies up to 5.25V. It draws only 27.3mA, and has a hardware shutdown feature which reduces current consumption to 250µA. The LTC6404 family is available in a compact 3mm × 3mm 16-pin leadless QFN package and operates over a –40°C to 125°C temperature range.

Applications

- Differential Input A/D Converter Driver
- Single-Ended to Differential Conversion/Amplification
- Common Mode Level Translation
- Low Voltage, Low Noise, Signal Processing

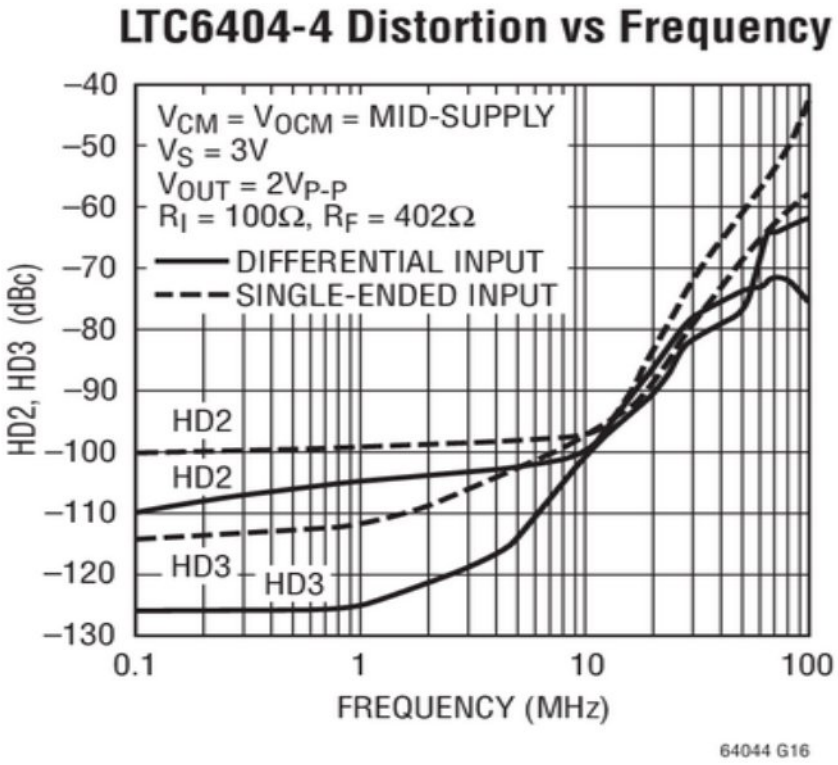


FIG NO.28

LTC2173

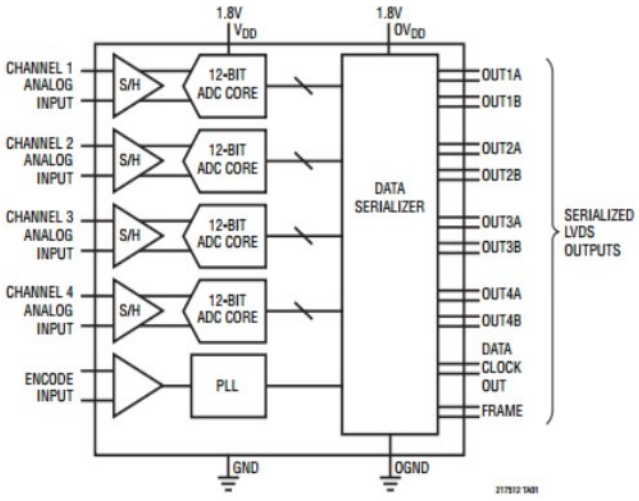
- Features
  - 4-Channel Simultaneous Sampling ADC
  - 70.6dB SNR
  - 88dB SFDR
  - Low Power: 545mW/439mW/369mW Total, 136mW/110mW/92mW per Channel
  - Single 1.8V Supply
  - Serial LVDS Outputs: 1 or 2 Bits per Channel
  - Selectable Input Ranges: 1VP-P to 2VP-P
  - 800MHz Full Power Bandwidth S/H
  - Shutdown and Nap Modes

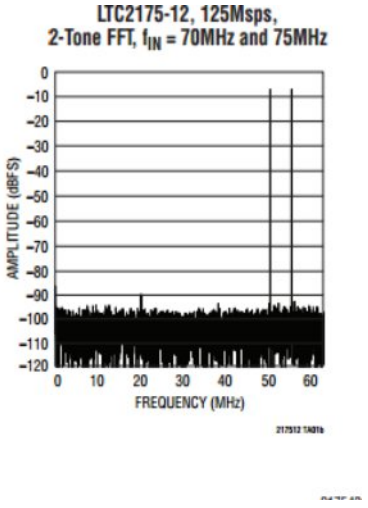
- Serial SPI Port for Configuration
- Pin Compatible 14-Bit and 12-Bit Versions
- 52-Pin (7mm × 8mm) QFN Package

- Applications
  - Communications
  - Cellular Base Stations
  - Software Defined Radios
  - Portable Medical Imaging
  - Multichannel Data Acquisition
  - Non-destructive Testing

Description

LTC2175-12, 125Msps, 2-Tone FFT, fIN = 70MHz and 75MHz The LTC®2175-12/LTC2174-12/LTC2173-12 are 4-channel, simultaneous sampling 12-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 70.6dB SNR and 88dB spurious free dynamic range (SFDR). Ultralow jitter of 0.15psRMS allows under-sampling of IF frequencies with excellent noise performance. DC specs include ±0.3LSB INL (typ), ±0.1LSB DNL (typ) and no missing codes over temperature. The transition noise is a low 0.3LSBRMS. The digital outputs are serial LVDS to minimize the number of data lines. Each channel outputs two bits at a time (2-lane mode). At lower sampling rates there is a one bit per channel option (1-lane mode). The LVDS drivers have optional internal termination and adjustable output levels to ensure clean signal integrity. The ENC+ and ENC– inputs may be driven differentially or single-ended with a sine wave, PECL, LVDS, TTL, or CMOS inputs. An internal clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.





DAC 8534

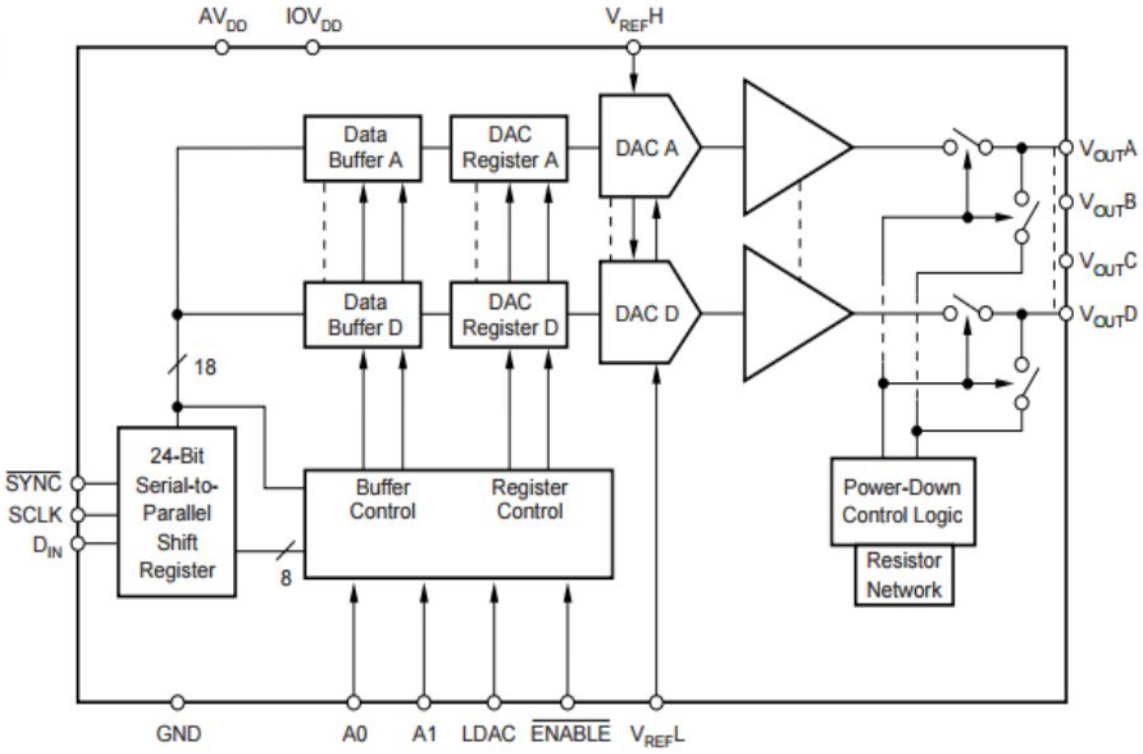


FIG NO.29

FEATURES

- POWER SUPPLY: +2.7V to +5.5V
- micro-POWER OPERATION: 950µA at 5V
- 16-BIT MONOTONIC OVER TEMPERATURE
- SETTLING TIME: 10µs to ±0.003% FSR
- ULTRA-LOW AC CROSSTALK: –100dB typ
- POWER-ON RESET TO ZERO-SCALE
- ON-CHIP OUTPUT BUFFER AMPLIFIER WITH RAIL-TO-RAIL OPERATION
- DOUBLE BUFFERED INPUT ARCHITECTURE
- SIMULTANEOUS OR SEQUENTIAL OUTPUT UPDATE AND POWER-DOWN
- 16 CHANNELS BROADCAST CAPABILITY
- SCHMITT-TRIGGERED INPUTS
- TSSOP-16 PACKAGE

APPLICATIONS

- PORTABLE INSTRUMENTATION
- CLOSED-LOOP SERVO-CONTROL
- PROCESS CONTROL
- DATA ACQUISITION SYSTEMS
- PROGRAMMABLE ATTENUATION
- PC PERIPHERALS

DESCRIPTION

The DAC8534 is a quad channel, 16-bit Digital-to-Analog Converter (DAC) offering low-power operation and a flexible serial host interface. Each on-chip precision output amplifier allows rail-to-rail output swing to be achieved over the supply range of 2.7V to 5.5V. The device supports a standard 3-wire serial interface capable of operating with input data clock frequencies up to 30MHz for IOVDD = 5V. The DAC8534 requires an external reference voltage to set the output range of each DAC channel. Also incorporated into the device is a power-on reset circuit which ensures that the DAC outputs power up at zero-scale and remain there until a valid write takes place.

The DAC8534 provides a per channel power-down feature, accessed over the serial interface, that reduces the current consumption to 200nA per channel at 5V. The low-power consumption of this device in normal operation makes it ideally suited to portable battery-operated equipment and other low-power applications. The power consumption is 5mW at 5V, reducing to 4µW in power-down mode. The DAC8534 is available in a TSSOP-16 package with a specified operating temperature range of –40°C to +105°C.

CONCLUSION

The physics design of LEHIPA, 20MeV, 30mA proton linac has been completed. Various sub-systems of accelerator have been designed and their procurement has been initiated. Development of fabrication techniques of RFQ and DTL structures has also been taken up in-house (with CDM) as well as with industries. The LEHIPA facility will be housed in the basement of Common Facility Building (CFB) at BARC. Construction of the building has commenced and installations of utilities like electrical power, cooling water plant and assembly of accelerator systems in CFB begun in 2008. In order to get hands on experience at relatively high RF power, a 400 keV RFQ for accelerating deuterons has been designed and is being fabricated. Major sub-systems of this device will be assembled and tested in VDG tandem hall. This RFQ will be used for generating 14 MeV neutrons by D-T reaction and will be used for studying neutron multiplication in a sub-critical assembly.

The development for RFPI is progressing steadily with us having completed working on module 1 and 2 which are temperature analysis and detection of arc for LEHIPA.

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S.Krishnagopal- Raja Ramanna Centre for Advanced Technology , Indore

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November 1-4, 2006

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