Introduction

In high performance analog circuit, it is a very challenging task to design a high performance complemtary metal oxide semi-conductor, which is used in either ADC or DAC. As we are dealing with high performance circuit, to meet these requirement both accuracy and fast settling of system is needed, OP-Amp with high DC gain frequency can satisfy both of these requirement. Although a Op-amp with high DC gain satisfy these requirement, but still in many aspects which leads to complementary demands, as the intrinsic gain of many devices are limited.

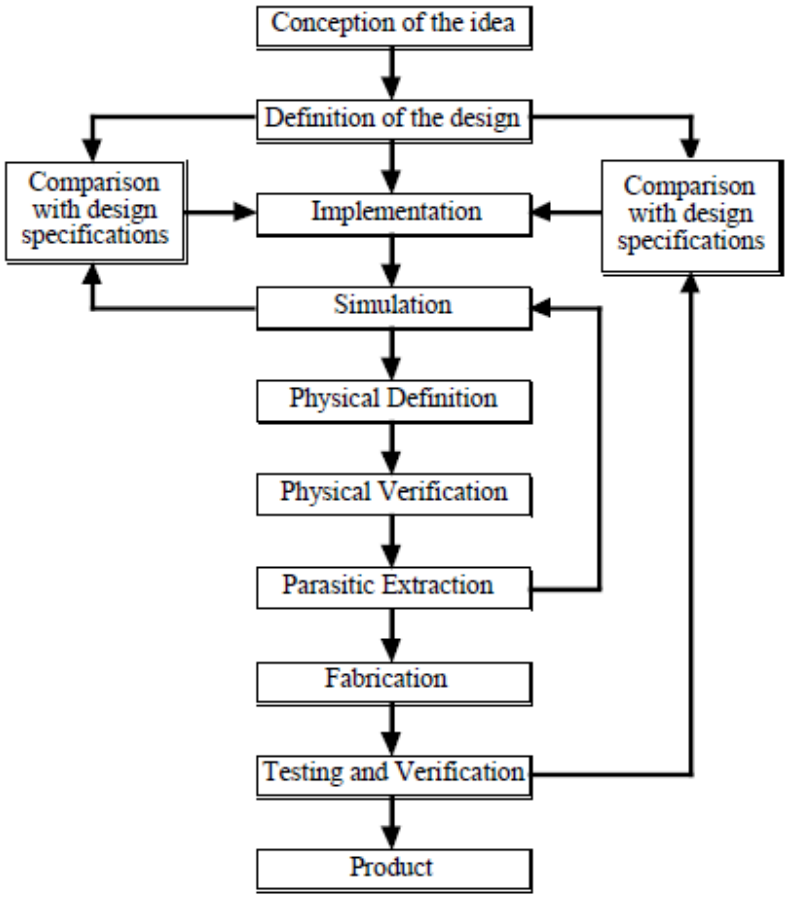
OTA is an Op-amp without an output driver. It is capable of driving small capacitive load. These makes OTA a well suitable for pipeline application.The whole procedure is focused on the development of ultra low power amplifier requiring low silicon area but been able to drive high capacitive load.

BIPOLAR VS. MOS TRANSISTORS

CATEGORY	BIPOLAR	CMOS
Turn-on Voltage	0.5-0.6 V	0.8-1 V
Saturation Voltage	0.2-0.3 V	0.2-0.8 V
g_m at 100µA	4 mS	0.4 mS (W=10L)
Analog Switch Implementation	Offsets, asymmetric	Good
Power Dissipation	Moderate to high	Low but can be large
Speed	Faster	Fast
Compatible Capacitors	Voltage dependent	Good
AC Performance Dependence	DC variables only	DC variables and geometry
Number of Terminals	3	4
Noise (1/f)	Good	Poor
Noise Thermal	OK	OK
Offset Voltage	< 1 mV	5-10 mV

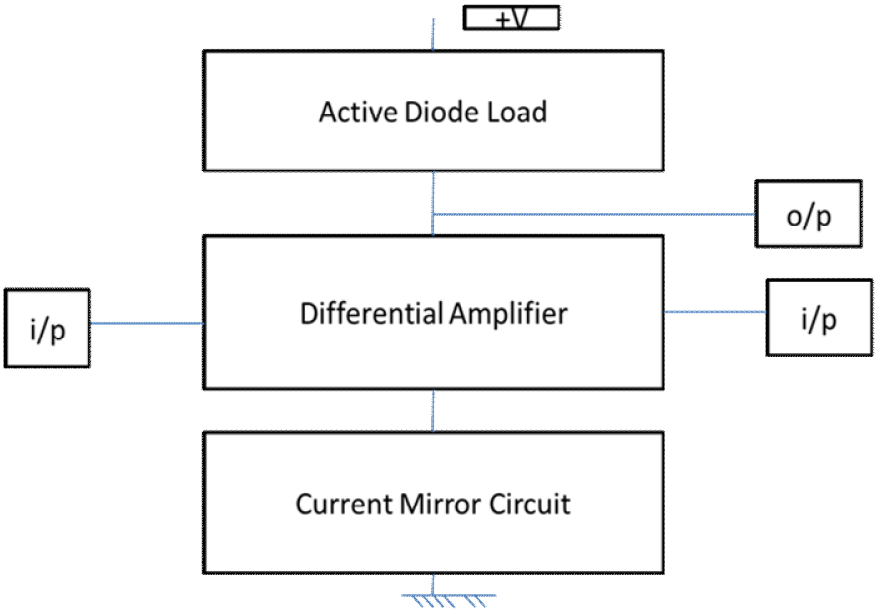
The basic comparison between BJT and CMOS is shown in above table.

THE ANALOG IC DESIGN PROCESS



The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

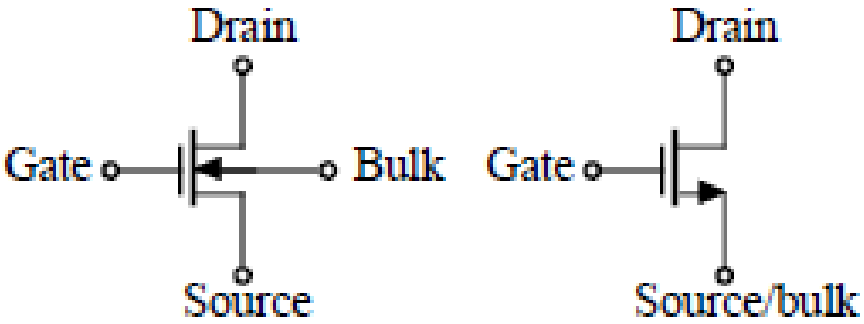
The basic block diagram of operational transconductance amplifier can be given as:-



From the above diagram we can see that it is basically made up of 3 major blocks, viz. load block , diff-amp and current mirror circuit. Now we will see each block in detail.

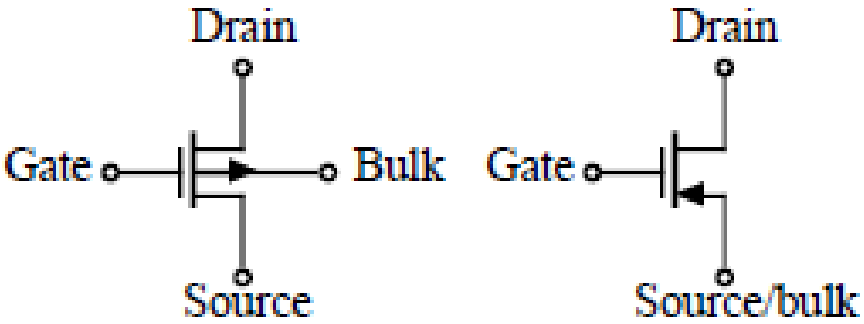
Related Theory:

Symbol representation of transistor



n-channel, enhancement, $V_{BS} \neq 0$

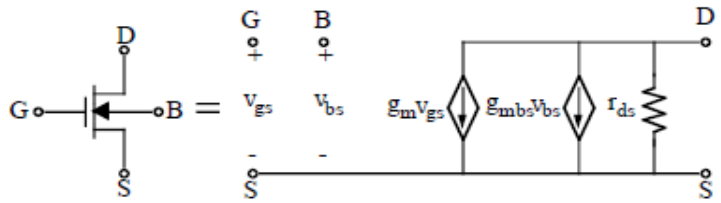
n-channel, enhancement, bulk at most negative supply



p-channel, enhancement, $V_{BS} \neq 0$

p-channel, enhancement, bulk at most positive supply

SMALL SIGNAL MODEL FOR THE MOSFET



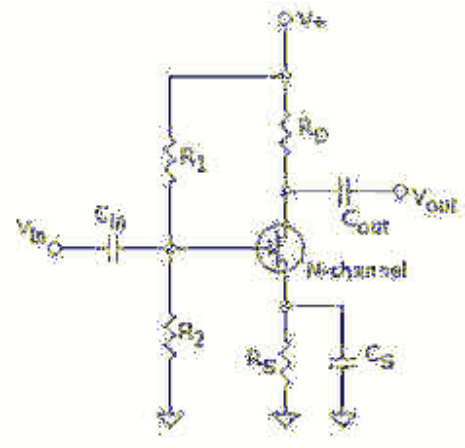
$$g_m = \sqrt{\frac{2K'WI_D}{L}}$$

$$g_{mbs} = \frac{g_m \gamma}{2\sqrt{2\phi_F + |V_{BS}|}}$$

$$r_{ds} \approx \frac{1}{g_{ds}} = \frac{1}{\lambda I_D}$$

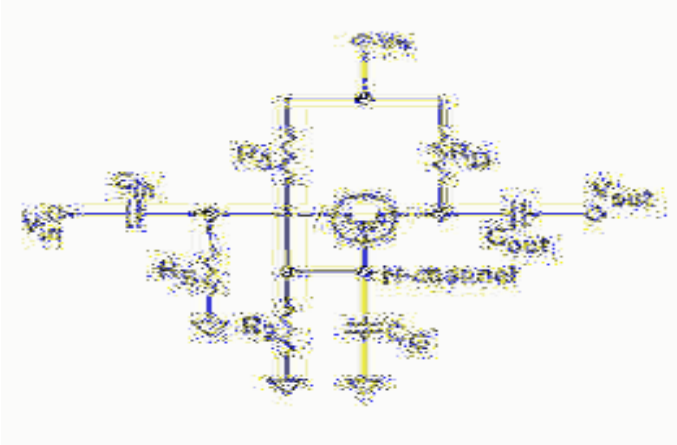
There are three basic configuration of IC MOSFET amplifiers.

(i) COMMON SOURCE:-



Benefits of using CMOS CS Amplifier
1.Large input impedance
2.Low output impedance
3.Large small signal voltage gain.

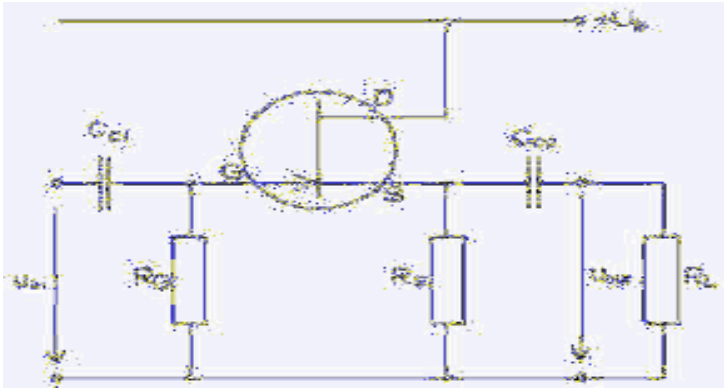
(ii) **COMMON GATE**



Benefits of using CMOS CG Amplifier

1. Input resistance is low
2. Output resistance is high
3. Current gain is unity.

(iii) COMMON DRAIN



Benefits of using CMOS CG Amplifier

1.Unity voltage gain
2.Low output resistance
3.It is also use as voltage buffer

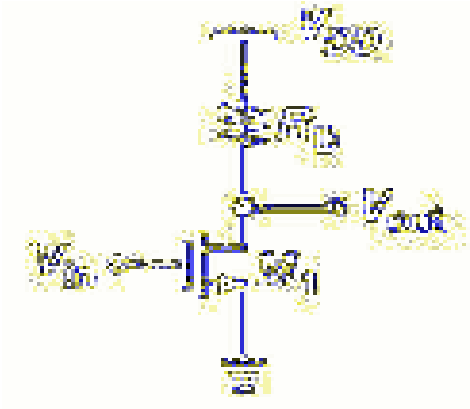
From the above three configuration the configuration which meet our requirement is common source amplifier. Hence, in our project we are going to use common source CMOS configuration in each and every circuit.

Now we will discuss each and every block of OTA in detail.

1. **Active load block:-**

   In this there are basically two types of loads, viz. resistive load and diode load.

   (i) Resistive load



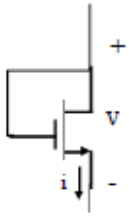
The voltage gain of the above circuit can be given as Av=(-gm x RD)

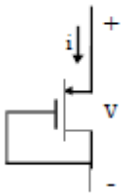
When a circuit makes use of a resistance as a load this is called passive load passive load passive load the resistance which consumes power proportional to R the value of load which we are using, this is a passive load.

(ii) Active load

MOS ACTIVE RESISTORS

Realizations





When the drain is connected to the gate, the transistor is always saturated.

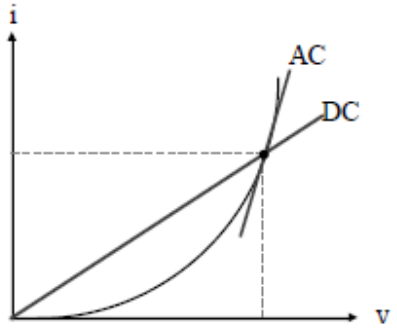
$v_{DS} \geq v_{GS} - V_T$

$v_D - v_S \geq v_G - v_S - V_T$

$\therefore \quad v_{DG} \geq -V_T$ where $V_T > 0$

Large Signal

I-V Characteristics -



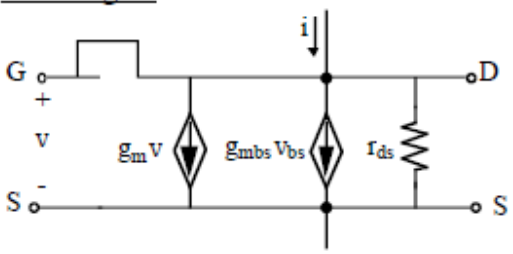
$$i = i_D = \left(\frac{K'W}{2L}\right)[v_{GS} - V_T]^2$$

$$= \frac{\beta}{2}(v_{GS} - V_T)^2, \quad \text{ignore } \lambda$$

or

$$v = v_{DS} = v_{GS} = V_T + \sqrt{\frac{2i_D}{\beta}}$$

Small signal



If $V_{BS} = 0$, then $R_{OUT} = \frac{v}{i} = \frac{1}{g_M + g_{DS}} \approx \frac{1}{g_M}$

The voltage gain can be given as Av = - (gm1 / gm2)

In this we are ignoring bulk transconductance.

Active load:- when resistor is replaced by an active device which acts as a resistor then this is called active load.

Besides power saving there is additional advantage, because today very large number of circuits are actually in integrated circuit form, in integrated circuits remember one thing that creating one for example, in a unit one mosfet and one resistance is more expensive and it will take more

steps for fabrication then two resistors. That means, if we can replace this resistance by a mosfet then the circuit will take two mosfets, but making of two mosfets are in fact, just multiplying in some component is much more economical and convenient in a integrated circuit rather than creating a different element all together resistance and mosfet two are very different elements and two mosfets they are belong to the same category and hence their construction is very simple and more economical.

2. Diff-amp block:-

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It is an analog circuit with two inputs V_{in}^- and V_{in}^+ and one output V_{out} in which the output is ideally proportional to the difference between the two voltages

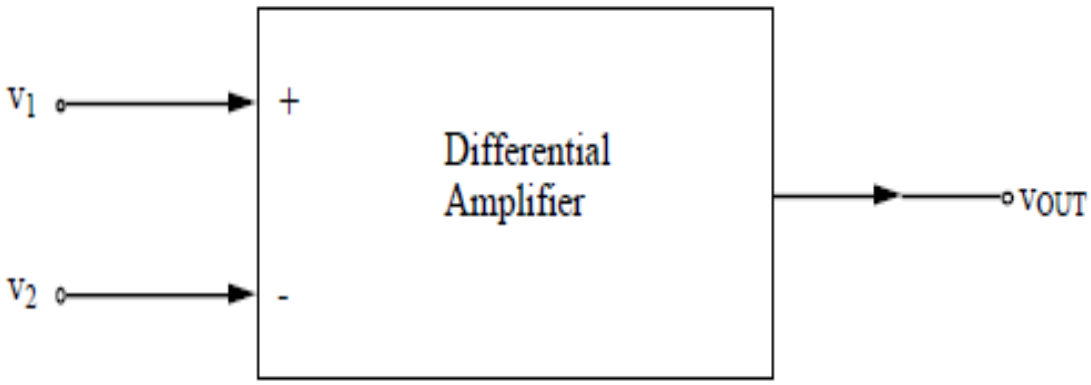
$$V_{out} = A(V_{in}^+ - V_{in}^-)$$

where A is the gain of the amplifier.

The differential pair (differential amplifier) configuration

- Widely used building block in analog integrated circuit design
  - Performance depends critically on the matching of the devices
  - Utilizes more components than single-ended circuits
  - Well suited for IC fabrication
- Advantages of using differential pair
  - Less sensitive to noise and interference than single-ended circuits
  - Bias is provided without the need for bypass and coupling capacitors

Definition of a Differential Amplifier



$$v_{OUT} = A_{VD}(v_1 - v_2) \pm A_{VC}\left(\frac{v_1 + v_2}{2}\right)$$

Differential voltage gain = A_{VD} (100)

Common mode voltage gain = A_{VC} (1)

Common mode rejection ratio = $\frac{A_{VD}}{A_{VC}}$ (1000)

Input offset voltage = $V_{OS}(in) = \frac{V_{OS}(out)}{A_{VD}}$ (2-10mV)

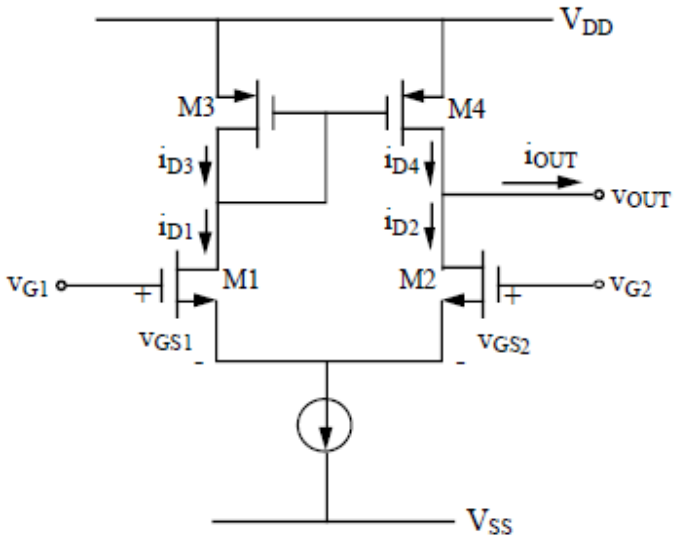
Common mode input range = V_{ICMR} ($V_{SS}+2V<V_{ICMR}<V_{DD}-2V$)

Power supply rejection ratio (PSRR)

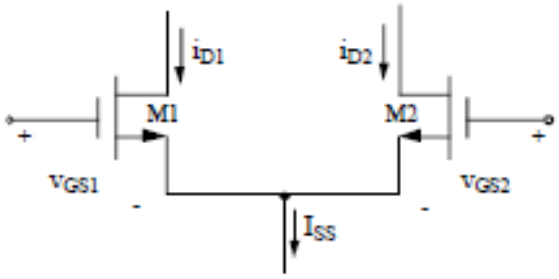
Noise

VI.2-1 - CMOS DIFFERENTIAL AMPLIFIERS

N-Channel Input Pair Differential Amplifier



Large Signal Analysis of CMOS Differential Amplifiers



(1). $v_{ID} = v_{GS1} - v_{GS2} = \sqrt{\frac{2i_{D1}}{\beta}} - \sqrt{\frac{2i_{D2}}{\beta}}$

(2). $I_{SS} = i_{D1} + i_{D2}$

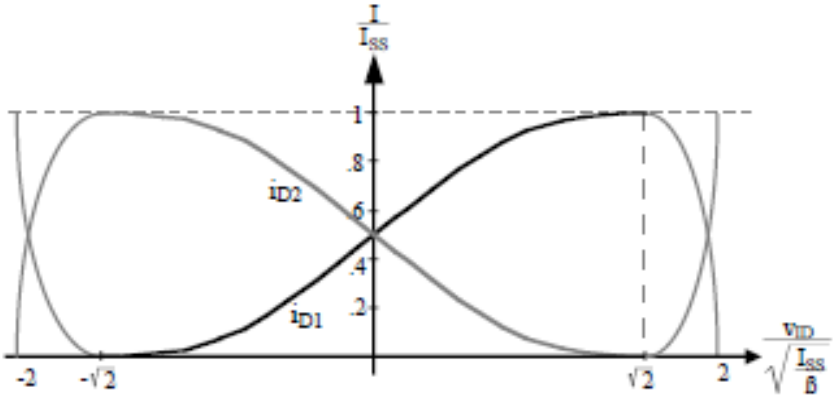
Solving for i_{D1} and i_{D2} gives,

(3). $i_{D1} = \left(\frac{I_{SS}}{2}\right) + \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$

And

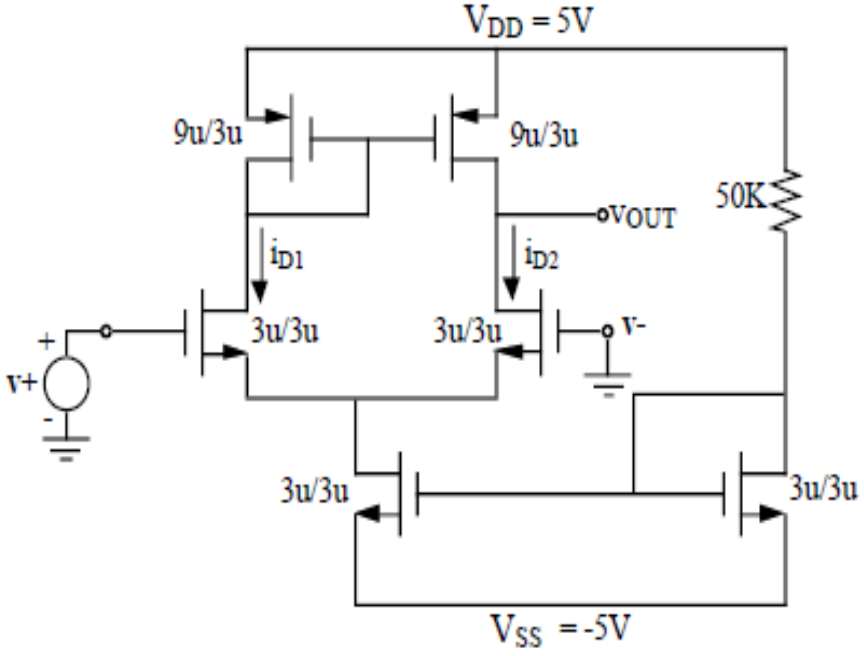
(4). $i_{D2} = \left(\frac{I_{SS}}{2}\right) - \left(\frac{I_{SS}}{2}\right) v_{ID} \sqrt{\frac{\beta}{I_{SS}} - \frac{\beta^2 v_{ID}^2}{4I_{SS}^2}}$

Where $v_{ID} < 2\sqrt{\frac{I_{SS}}{\beta}}$ $\quad g_m = \frac{\partial i_{D1}}{\partial v_{ID}} = \sqrt{\frac{\beta I_{SS}}{4}}$

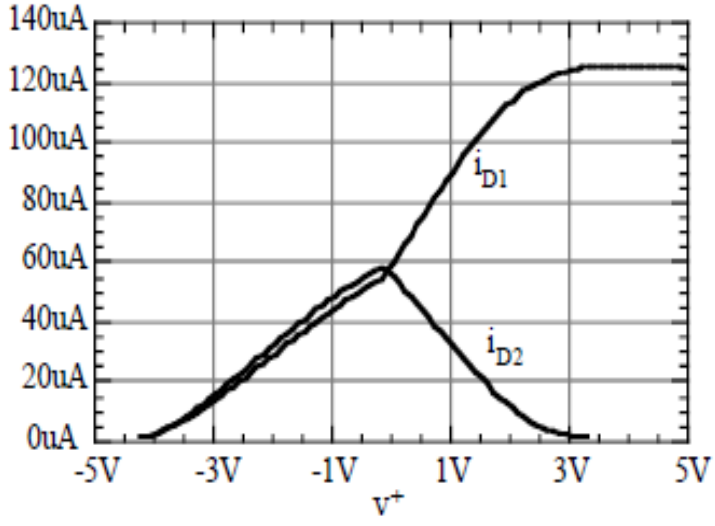


Transconductance Characteristics of the Differential Amplifier

Circuit



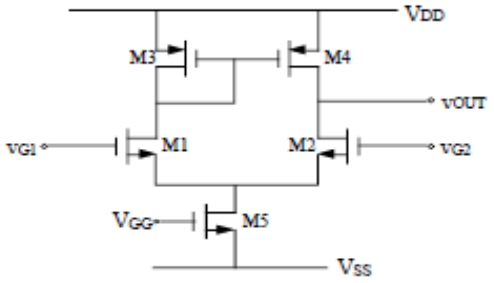
Simulation Results



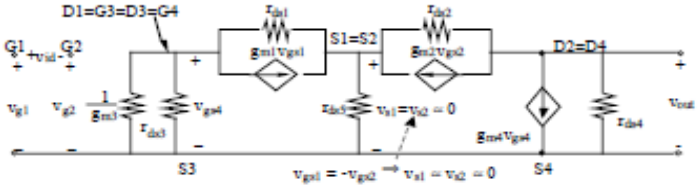
CMOS DIFFERENTIAL AMPLIFIER

Small Signal Differential Mode Gain

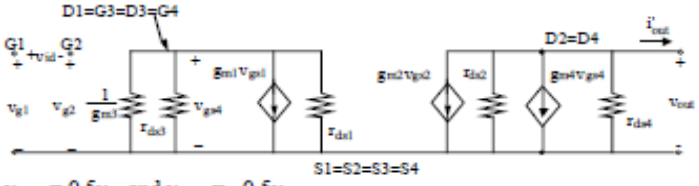
N-Channel input differential amplifier -



Exact small signal model -



Simplified small signal model using symmetry -



$v_{gs1} = 0.5v_{id}$ and $v_{gs2} = -0.5v_{id}$

CMOS DIFFERENTIAL AMPLIFIER

Unloaded Differential Transconductance Gain

($R_L = 0$)

$$i_{out}' = -g_{m4}v_{gs4} - g_{m2}v_{gs2} = \frac{g_{m1}g_{m4}(r_{ds1} \parallel r_{ds3})}{1 + g_{m3}(r_{ds1} \parallel r_{ds3})} v_{gs1} - g_{m2}v_{gs2}$$

If $g_{m3}(r_{ds1} \parallel r_{ds3}) \gg 1$, $g_{m3} = g_{m4}$, and $g_{m1} = g_{m2} = g_{md}$, then

$$i_{out}' \approx g_{m1}v_{gs1} - g_{m2}v_{gs2} = g_{md}(v_{gs1} - v_{gs2}) = g_{md}v_{id}$$

or

$$\boxed{i_{out}' \approx g_{md}v_{id} = \sqrt{\frac{K_N'WI_{SS}}{L}}\, v_{id}}$$

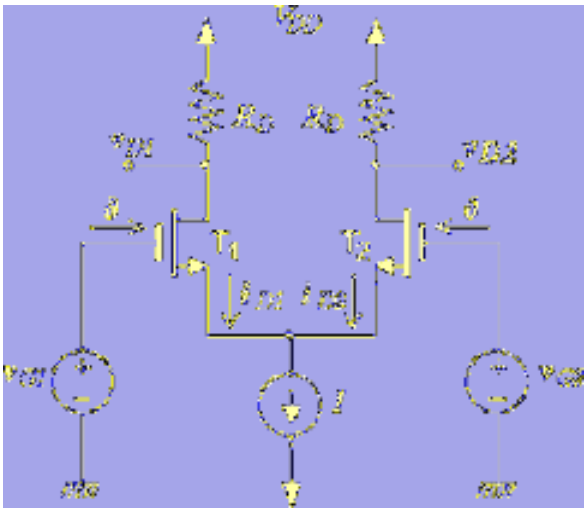
Unloaded Differential Voltage Gain

($R_L = \infty$)

$$\boxed{v_{out} \approx \frac{g_{md}}{g_{ds2} + g_{ds4}} v_{id} = \frac{2}{(\lambda_N + \lambda_P)}\sqrt{\frac{K_N'W}{I_{SS}L}}\, v_{id}}$$

Differential amplifier can be made using resistive and active load.

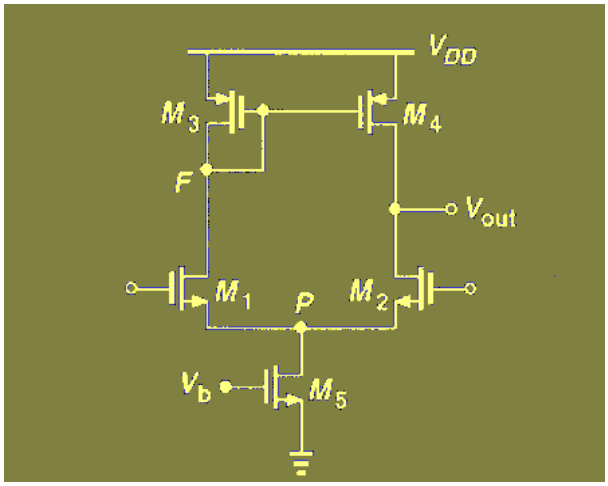
(i) Differential amplifier using resistive load:-



The voltage gain can be given as Av=(gm x RD / 2)

The problem with resistive load has been discuss in previous topic. To overcome this we will use active load instead of resistive load.

(ii) Differential amplifier using active load:-

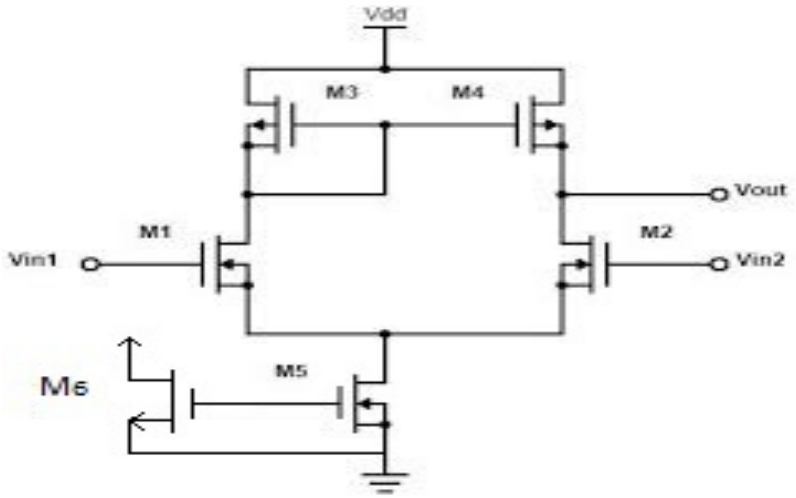


The voltage gain is given by Av = gm / (g02 + go4).

3. Differential amplifier with current mirror:-

The current mirror load provides double-ended to single-ended conversion without suffering the loss of a factor of two in differential-mode gain (the common-mode gain is twice as large also, but still very small) . It comes in a variety of versions (pnp, npn, nMOS, p-MOS); the examples below use p-channel MOSFETs in the mirror loading an nchannel common-source differential gain stage.

The active nature of the load doubles the current delivered to the load with differential-mode inputs, and while not sending any current to the load with common-mode inputs.



$$Av = gm1\ (rds2 \parallel rds4)$$

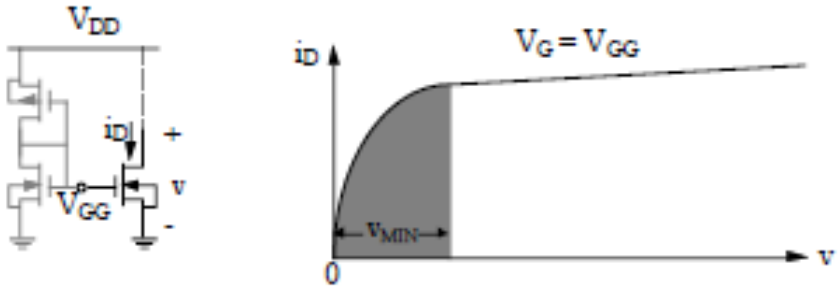
One of the important use of diff-amp with current mirror is that it is very useful in removing noise from the circuit. Due to its ability to reject common mode signal it is use as noise remover in a circuit.

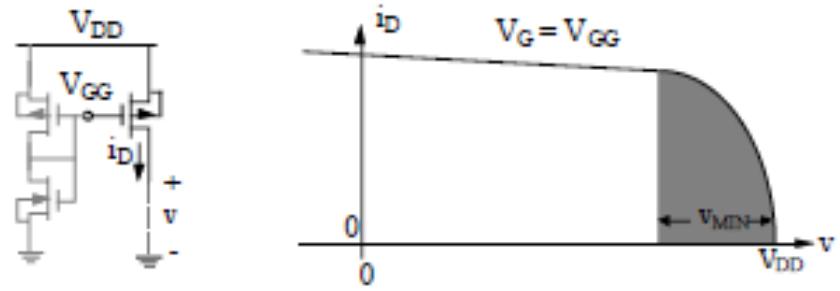
4. Source and sink

CHARACTERIZATION OF SOURCES & SINKS

1). Minimum voltage (v_{MIN}) across sink or source for which the current is no longer constant.
2). Output resistance which is a measure of the "flatness" of the current sink or source.

CMOS Current Sinks & Sources





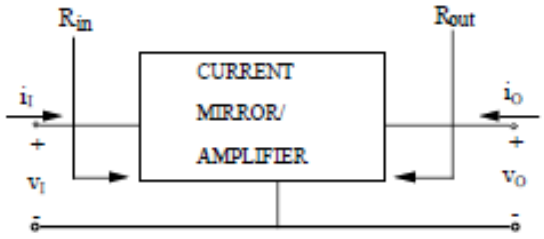
$$r_{OUT} = \frac{1}{\lambda I_D}$$

$v_{MIN} = v_{DS(SAT.)} = v_{ON}$ where $v_{ON} = v_{GS} - V_T$

5. Current mirror

V.4 - CURRENT MIRRORS/AMPLIFIERS

What Is A Current Mirror/Amplifier ?

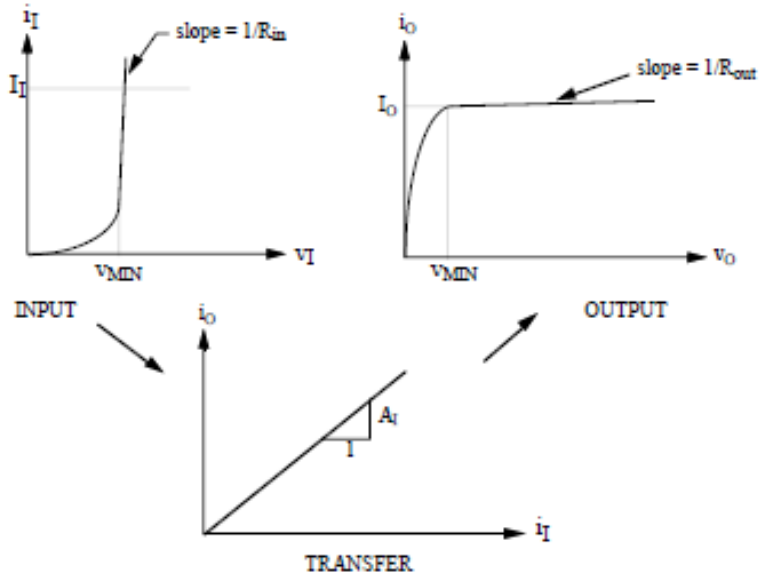


Ideally,

$i_O = A_I\, i_I$

$R_{in} = 0 \qquad R_{out} = \infty$

Graphical Characterization



FPGA (Field Programmable Gate Array**)**

Overview and Design Considerations

Xilinx® Field Programmable Gate Arrays (FPGAs) are highly flexible, reprogrammable logic devices that leverage advanced CMOS manufacturing technologies, similar to other industry-leading processors and processor peripherals. Like processors and peripherals, Xilinx FPGAs are fully user programmable. For FPGAs, the program is called a *configuration bitstream*, which defines the FPGA's functionality. The bitstream loads into the FPGA at system power-up or upon demand by the system.

The process whereby the defining data is loaded or programmed into the FPGA is called *configuration*. Configuration is designed to be flexible to accommodate different application needs and, wherever possible, to leverage existing system resources to minimize system costs. Similar to microprocessors, Xilinx FPGAs optionally load or boot themselves automatically from an external nonvolatile memory device. Alternatively, similar to microprocessor peripherals, Spartan-3 generation FPGAs can be downloaded or programmed by an external “smart agent”, such as a microprocessor, DSP processor, microcontroller, PC, or board tester. In either case, the configuration data path is either serial to minimize pin requirements or byte-wide for maximum performance or for easier interfaces to processors or to byte-wide Flash memory.

Similar to both processors and processor peripherals, Xilinx FPGAs can be reprogrammed, in system, on demand, an unlimited number of times. After configuration, the FPGA configuration bitstream is stored in highly robust CMOS configuration latches (CCLs).

Although CCLs are reprogrammable like SRAM memory, CCLs are designed primarily for data integrity, not for performance. The data stored in CCLs is written only during configuration and remains static unless changed by another configuration event.

This user guide provides both an introduction to the configuration options available to the user, and a detailed description of the configuration logic. This user guide includes the Extended Spartan-3A family, which includes the Spartan-3A, Spartan-3AN, and Spartan- 3A DSP platforms. The user guide also includes the earlier Spartan-3 and Spartan-3E families. Together, these families are sometimes referred to as the Spartan-3 generation.

Most basic configuration features are similar between the families, and differences are noted where necessary.

Design Considerations

Before starting a new FPGA design, spend a few minutes to consider which FPGA configuration mode best matches your system requirements. Each configuration mode dedicates certain FPGA pins and may borrow others. Similarly, the configuration mode may place voltage restrictions on some FPGA I/O banks.

If you have already selected an FPGA configuration mode, feel free to jump to the relevant section in the user guide. Otherwise, please evaluate the following design considerations to understand the options available.

Will the FPGA load configuration data itself from external or internal memory or will an external processor/microcontroller download configuration data?

Spartan-3 generation FPGAs are designed for maximum flexibility. The FPGA either automatically loads itself with configuration data, like a processor, or alternatively, another external intelligent device like a processor or microcontroller can download the configuration data. It is your choice and Table 1-2 summarizes the available options.

The self-loading FPGA configuration modes, generically called ***Master*** modes, are available with either a serial or byte-wide data path as shown in Figure 1-1. The Master modes leverage various types of non-volatile memories to store the FPGA's configuration information, as shown in Table 1-1. In Master mode, the FPGA's configuration bit stream typically resides in non-volatile memory on the same board, generally external to the FPGA. The FPGA internally generates a configuration clock signal called CCLK and the FPGA controls the configuration process.

Spartan-3AN FPGAs optionally configure from internal In-System Flash (ISF) memory, as shown in Figure 1-1c. In this mode, the configuration memory and the control and data signals are inside the package. Spartan-3AN FPGAs also optionally support all the other Spartan-3A FPGA configuration modes, as well.

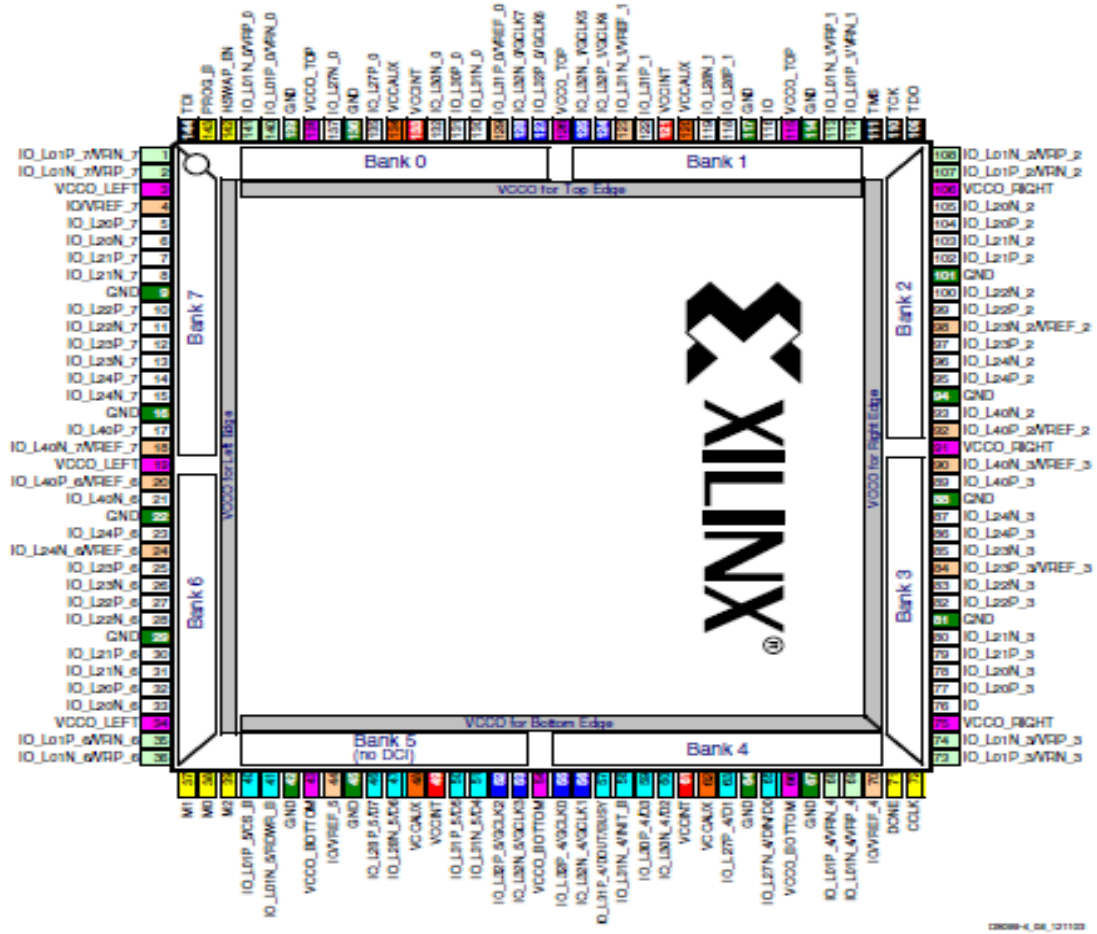


Figure 46: **TQ144 Package Footprint (Top View). Note pin 1 indicator in top-left corner and logo orientation.**

51	**I/O:** Unrestricted, general-purpose user I/O	12	**DUAL:** Configuration pin, then possible user I/O	12	**VREF:** User I/O or input voltage reference for bank
14	**DCI:** User I/O or reference resistor input for bank	8	**GCLK:** User I/O or global clock buffer input	12	**VCCO:** Output voltage supply for bank
7	**CONFIG:** Dedicated configuration pins	4	**JTAG:** Dedicated JTAG port pins	4	**VCCINT:** Internal core voltage supply (+1.2V)
0	**N.C.:** No unconnected pins in this package	16	**GND:** Ground	4	**VCCAUX:** Auxiliary voltage supply (+2.5V)

Literature Survey

Author	Publish in year	Title	Outcome
Yongjian Tang	2004	A 10-bit 20-Msample/s 49mW CMOS pipelined A/D converter	Designed a 10 bit ADC made in 0.6µm double-poly double-metal CMOS process having 5V supply voltage and 49 **mW** of power consumption
Hati, M.K.	2011	Design of a low power, high speed complementary input folded regulator cascode OTA for a parallel pipeline ADC	Designed 10-bit ADC using OTA with 180 nm technology with 1.8V and power consumption is only **3.24 mW**.
S.Hassan Mirhossien, AhmadAyahtollahi	2012	Design a 10 bit 100 MHz pipelined ADC using RB-OTA in 90 nm CMOS technology	Designed a 10 bit ADC using OTA in 90 nm technolgy with 1V of bias volatage and power consumption of **14.4 mW**
A J Sowjanya.K1 , D.S.Shylu2 , Dr.D.Jackuline Moni3 , Neetha C John4 , Anita Antony5	2012	A Low Power Gain Boosted Fully Differential OTA for a 10bit pipelined ADC	Designed a 10 bit pipelined ADC using OTA with 1.8V power supply and 70 **mW** of power consumption.

Problem Statement

The reduction of power consumption is a crucial task for battery-operated applications.There are OTA based ADC's which has been made with power consumption of approximately in some mW.

In high performance analog circuit, it is a challenging task to design a high performance CMOS OTA for use in Analog to Digital convertor.

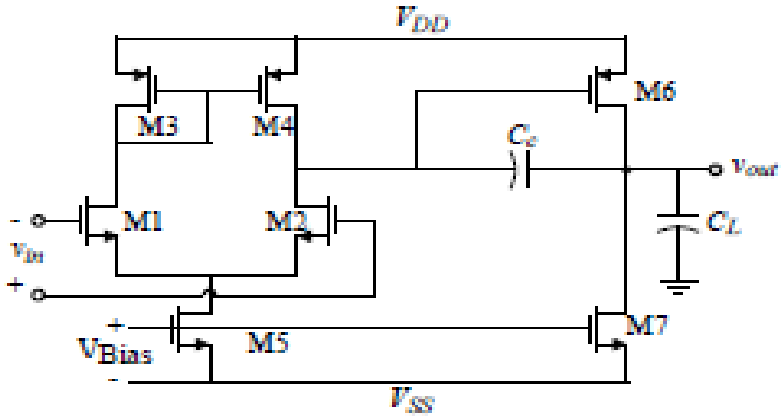
As we are dealing with high performance circuits, to meet these requirement, both accuracy and fast settling of system is needed, op-amp with high DC gain can satisfy this requirement, but still there are many aspects which leads to contradictory demands, as the intrinsic gain of devices is limited.

OTA is an op-amp without and output driver. It is capable of driving small capacitance loads. This make the OTA well suited for pipeline application.

The whole procedure is focused on the development of ultra-low power amplifier requiring low silicon area but being able to drive high capacitive loads.

Design and Analysis

Two-Stage Operational Amplifier Design



Important relationships:

$g_{m1} = g_{m2} = g_m$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$.

Slew rate $SR = \frac{I_5}{C_c}$ (1)

First-stage gain $A_{v1} = \frac{g_{m1}}{g_{ds2} + g_{ds4}} = \frac{2g_{m1}}{I_5(\lambda_2 + \lambda_4)}$ (2)

Second-stage gain $A_{v2} = \frac{g_{m6}}{g_{ds6} + g_{ds7}} = \frac{g_{m6}}{I_6(\lambda_6 + \lambda_7)}$ (3)

Gain-bandwidth $GB = \frac{g_{m1}}{C_c}$ (4)

Output pole $p_2 = \frac{-g_{m6}}{C_L}$ (5)

RHP zero $z_1 = \frac{g_{m6}}{C_c}$ (6)

Positive CMR $V_{in(max)} = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|_{(max)} + V_{T1(min)}$ (7)

$$\text{Negative CMR } V_{in(min)} = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1(max)} + V_{DS5}(\text{sat}) \qquad (8)$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \qquad (9)$$

All transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given:

1. Gain at dc, *Av* (0)
2. Gain-bandwidth, *GB*
3. Input common-mode range, ICMR
4. Load Capacitance, *CL*
5. Slew-rate, *SR*
6. Output voltage swing
7. Power dissipation.

Choose a device length to establish of the channel-length modulation parameter

Design the compensation capacitor *Cc*. It was shown that placing the loading pole *p*2 2.2 times higher than the *GB* permitted a 60^o phase margin (assuming that the RHP zero *z*1 is placed at or beyond ten times *GB*). This results in the following requirement for the minimum value for *Cc*.

$$C_c > 0.22C_L$$

Next, determine the minimum value for the tail current *I*5, based upon slew-rate requirements. Using Eq. (1), the value for *I*5 is determined to be

$$I_5 = SR \cdot C_c$$

$$I_5 \cong 10\left(\frac{V_{DD} + |V_{SS}|}{2 \cdot T_s}\right)$$

If the slew-rate specification is not given, then one can choose a value based upon settling time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail.

The value of *I*5 resulting from this calculation can be changed later if need be. The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for (*W*/*L*)3 was derived from Eq. (7).

$$S_3 = \frac{I_5}{K'_3[V_{DD} - V_{in}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

If the value determined for (*W*/*L*) 3 is less than one, then it should be increased to a value that minimizes the product of *W* and *L*. This minimizes the area of the gate region, which in turn reduces the gate capacitance. This gate capacitance will affect a pole-zero pair which causes a small degradation in phase margin. Requirements for the transconductance of the input transistors can be determined from knowledge of *Cc* and *GB*. The transconductance *gm*2 can be calculated using the following equation

$$\frac{g_{m3}}{2C_{gs3}} > 10GB.$$

The aspect ratio (*W*/*L*)1 is directly obtainable from *gm*1 as shown below

$$g_{m1} = GB \cdot C_c \Rightarrow S_2 = \frac{g_{m2}^2}{K'_2 I_5}$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate *VDS*5 using the following relationship derived from Eq. (8).

$$V_{DS5}(\text{sat}) = V_{in}(\min) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}(\max) \geq 100 \text{ mV}$$

If the value for *VDS*5 is less than about 100 mV then the possibility of a rather large (*W*/*L*)5 may result. This may not be acceptable. If the value for *VDS*5 is less than zero, then the ICMR specification may be too stringent. To solve this problem, *I*5 can be reduced or(*W*/*L*)1 increased.

The effects of these changes must be accounted for in previous design steps. One must iterate until the desired result is achieved. With *VDS*5 determined, (*W*/*L*) 5 can be extracted using Eq. (9) in the following way

$$S_5 = \frac{2I_5}{K'_5[V_{DS5}(\text{sat})]^2}$$

For a phase margin of 60□, the location of the loading pole was assumed to be placed at 2.2 times *GB*. Based upon this assumption and the relationship for |*p*2| in Eq. (5), the transconductance *gm*6 can be determined using the following relationship

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

Since *S*3 is known as well as *gm*6 and *gm*3, assuming balanced conditions,

$$S_6 = S_3\left(\frac{g_{m6}}{g_{m3}}\right)$$

can be calculated from the consideration of the "proper mirroring" of first-stage the current mirror load of Fig. 6.3-1. For accurate current mirroring, we want *VSD*3 to be equal to *VSD*4. This will occur if *VSG*4 is equal to *VSG*6. *VSG*4 will be equal to *VSG*6 if

$$I_6 = (S_6/S_4)I_4 = (S_6/S_4)(I_5/2)$$

Choose the larger of these two values for *I*6 (Eq. 19 or Eq. 20). If the larger value is found in Eq (19), then (*W*/*L*)6 must be increased to satisfy Eq. (20). If the larger value is found in Eq. (20), then no other adjustments must be made. One also should check the power dissipation requirements since *I*6 will most likely determine the majority of the power dissipation. The device size of M7 can be determined from the balance equation given below

$$S_7 = (I_6/I_5)S_5$$

The first-cut design of all *W*/*L* ratios are now complete. Fig. 6.3-2 illustrates the above design procedure showing the various design relationships and where they apply in the two-stage CMOS op amp.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)I_6(\lambda_6 + \lambda_7)}$$

If the gain is too low, a number of things can be adjusted. The best way to do this is to use the table below, which shows the effects of various device sizes and currents on the different parameters generally specified. Each adjustment may require another pass through this design procedure in order to insure that all specifications have been met. Below table summarizes the above design procedure.

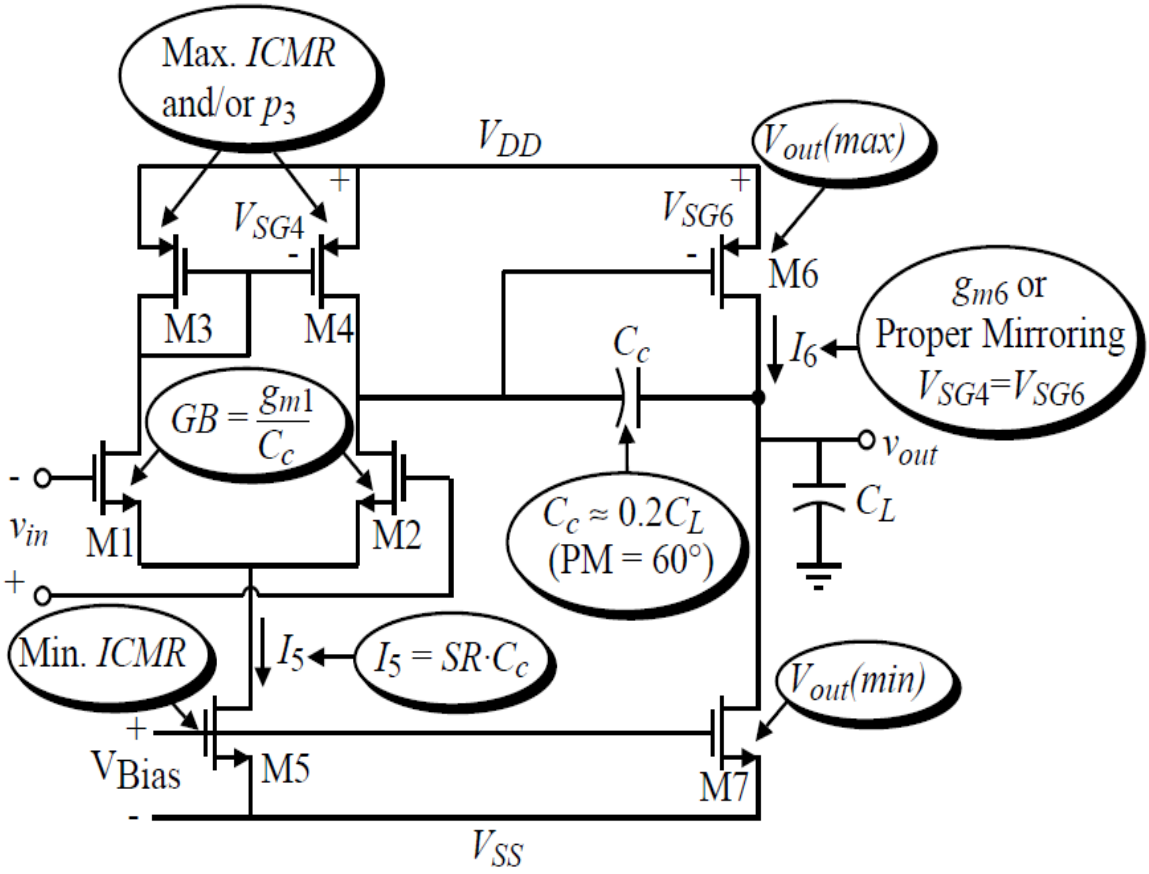


Fig: Illustration of the design relationships and the circuit for
a two-stage CMOS op amp. At this point in the design procedure, the total amplifier gain must be checked against the Specifications

Dependencies of device performance on various parameters

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Comp. Cap..
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase DC Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase GB	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\downarrow$

Design Technology

- The 180 nanometer (180 nm) process refers to the level of semiconductor process technology that was reached in the 1999-2000 timeframe by most leading semiconductor companies, like Intel, Texas Instruments, IBM, and TSMC.
- The origin of the 180 nm value is historical, as it reflects a trend of 70% scaling every 2–3 years. The naming is formally determined by the International Technology Roadmap for Semiconductors (ITRS).
- Some of the CPU's manufactured with this process include Interl Coppermine family of Pentium III processors. This was the first technology using a gate length shorter than that of light used for lithography (which has a minimum of 193nm).
- Some more recent microprocessors and microcontrollers (e.g. PIC) are using this technology because it is typically low cost and does not require upgrading of existing equipment.

10 µm – 1971

6 µm – 1974

3 µm – 1977

1.5 µm – 1982

1 µm – 1985

800 nm – 1989

600 nm – 1994

350 nm – 1995

250 nm – 1997

180 nm – 1999

130 nm – 2001

90 nm – 2004

65 nm – 2006

45 nm – 2008

32 nm – 2010

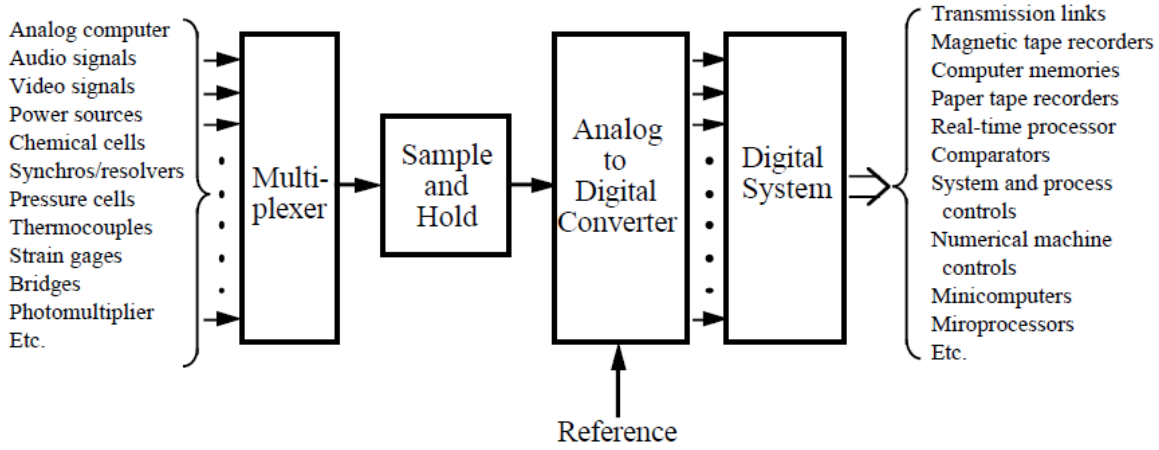
22 nm – 2012

14 nm – 2014

10 nm – *2016-2017*

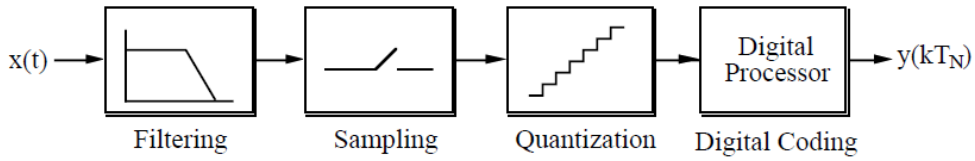
Application

A/D and D/A Converters in Data Systems



CHARACTERIZATION OF ANALOG TO DIGITAL CONVERTERS

General A/D Converter Block Diagram



A/D Converter Types

1.) Serial.

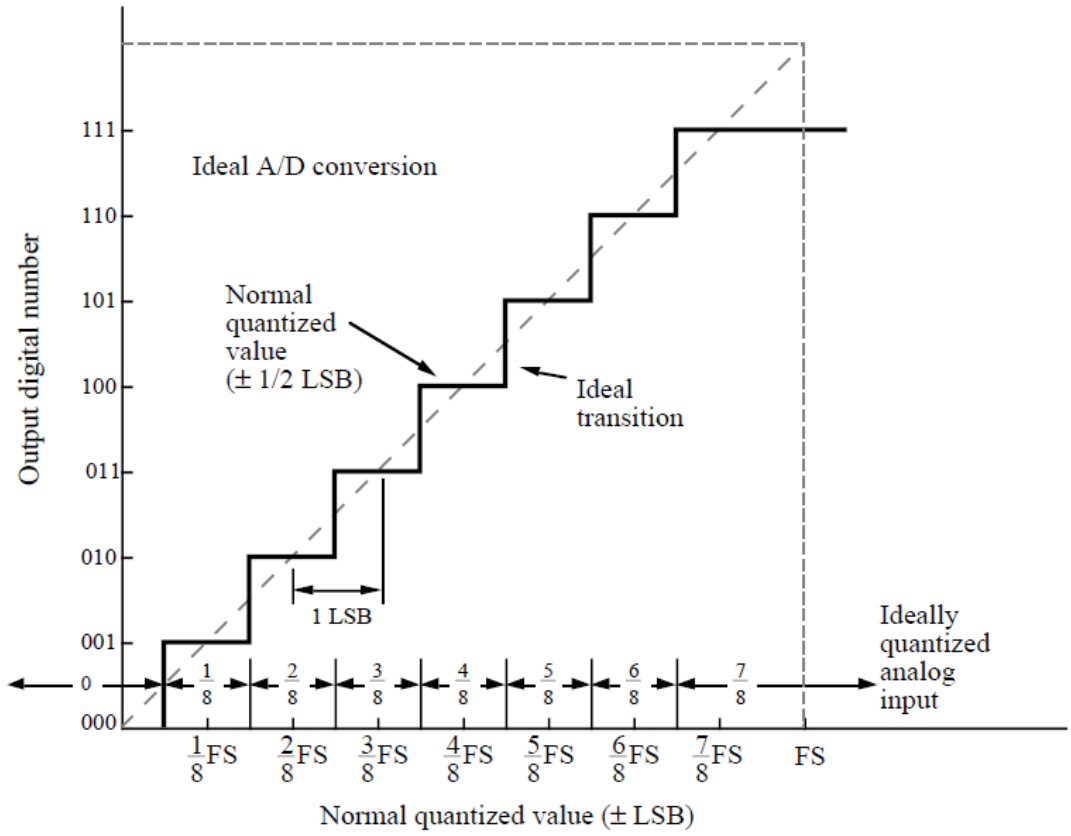
2.) Medium speed.

3.) High speed and high performance.

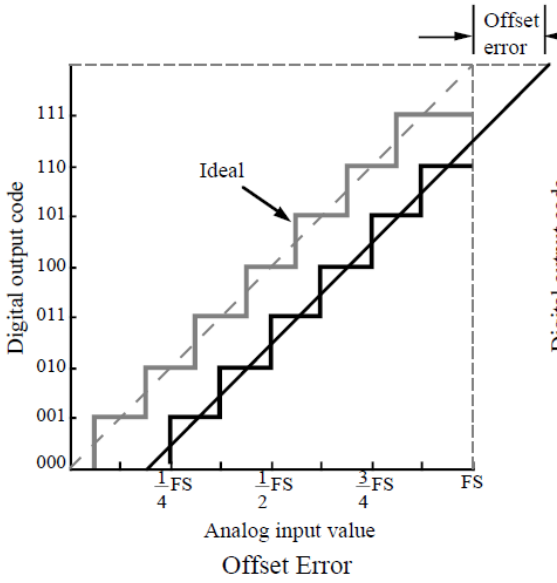
4.) New converters and techniques.

Characterization of A/D Converters

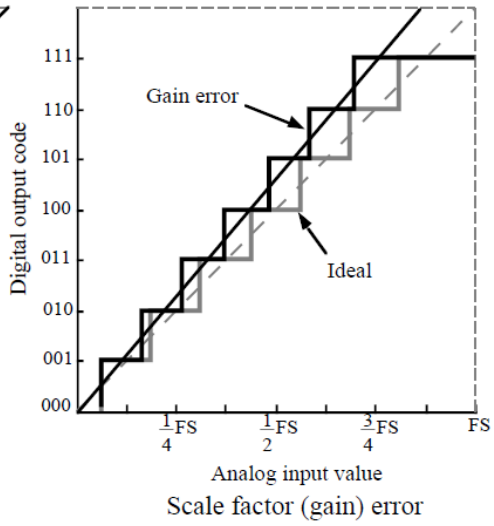
Ideal Input-Output Characteristics for a 3-bit ADC



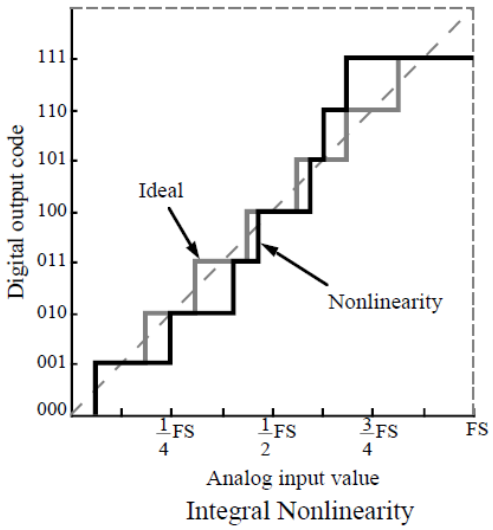
Non-ideal Characteristics of A/D Converters



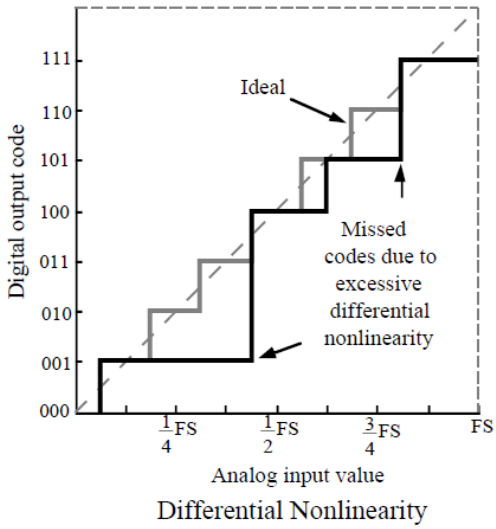
Offset Error



Scale factor (gain) error

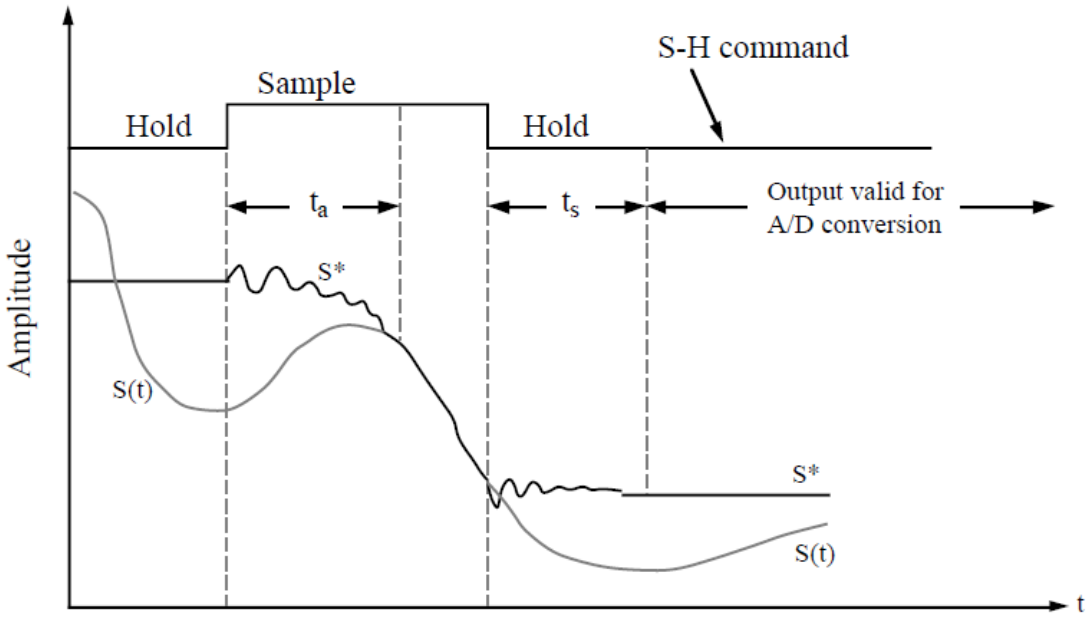


Integral Nonlinearity



Differential Nonlinearity

Sampled Data Aspect of ADC's



Tsample = ts + ta

ta = acquisition time

ts = settling time

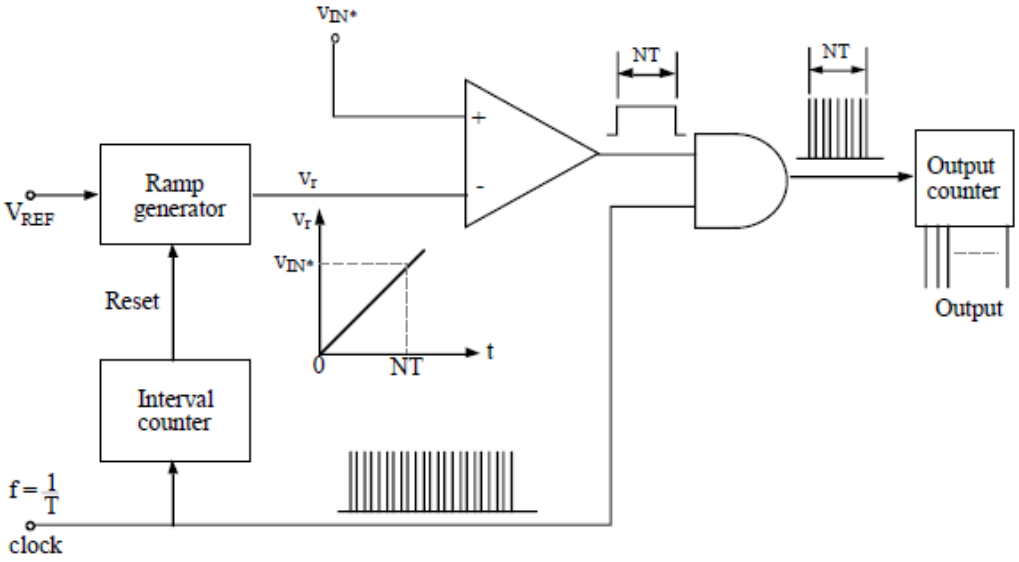
tADC = time for ADC to convert analog input to digital word.

Conversion time = ts + ta + tADC.

Noise = (kT/C) V^2 (rms)

X.7 - SERIAL A/D CONVERTERS

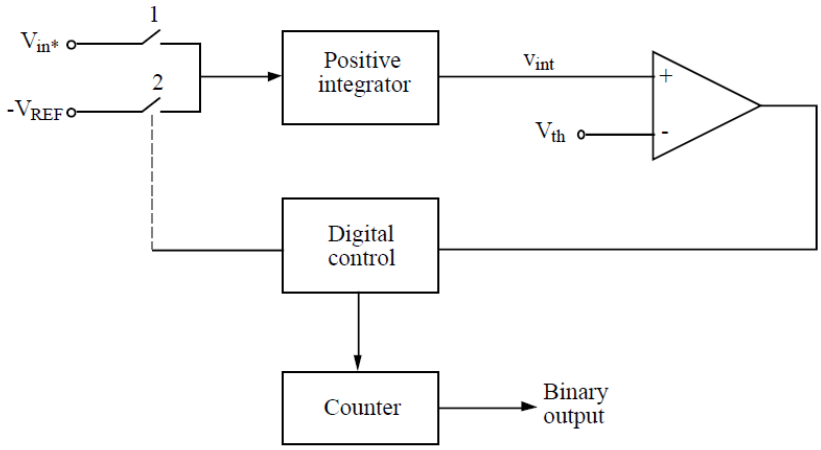
Single-Slope, A/D Converter



- Simplicity of operation
- Subject to error in the ramp generator
- Long conversion times

Dual Slope, A/D Converter

Block Diagram:



Operation :

1.) Initially $v_{int} = 0$ and v_{in} is sampled and held ($V_{in}^* > 0$).

2.) Reset by integrating until $v_{int}(0) = V_{th}$.

3.) Integrate V_{in}^* for N_{ref} clock cycles to get,

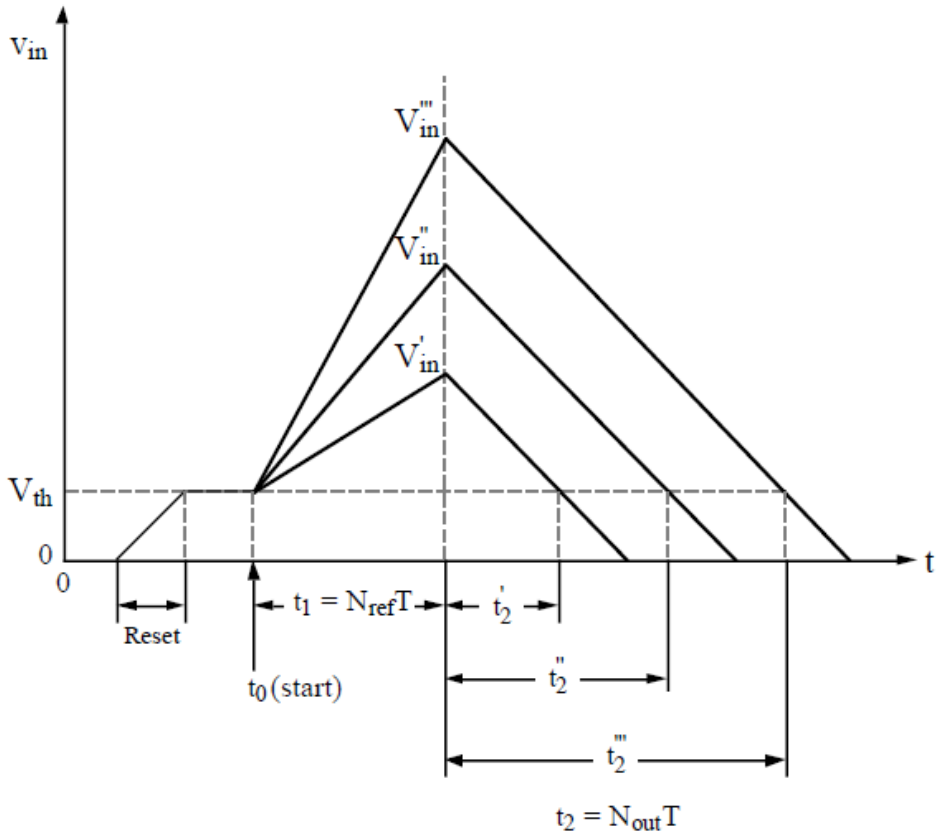
$$v_{int}(t_1) = v_{int}(N_{ref}T) = k\int_0^{N_{ref}T} V_{in}^* dt + v_{int}(0) = kN_{ref}TV_{in}^* + V_{th}$$

4.) The Carry Output on the counter is used to switch the integrator from V_{in}^* to $-V_{REF}$. Integrate until v_{int} is equal to V_{th} resulting in

$$v_{int}(t_1 + t_2) = v_{int}(t_1) + k\int_{t_1}^{N_{out}T + t_1} -V_{REF}dt = V_{th}$$

$$\therefore kN_{ref}TV_{in}^* + V_{th} - kV_{REF}N_{out}T = V_{th} \Rightarrow \boxed{V_{REF}\frac{N_{out}}{N_{ref}} = V_{in}^*}$$

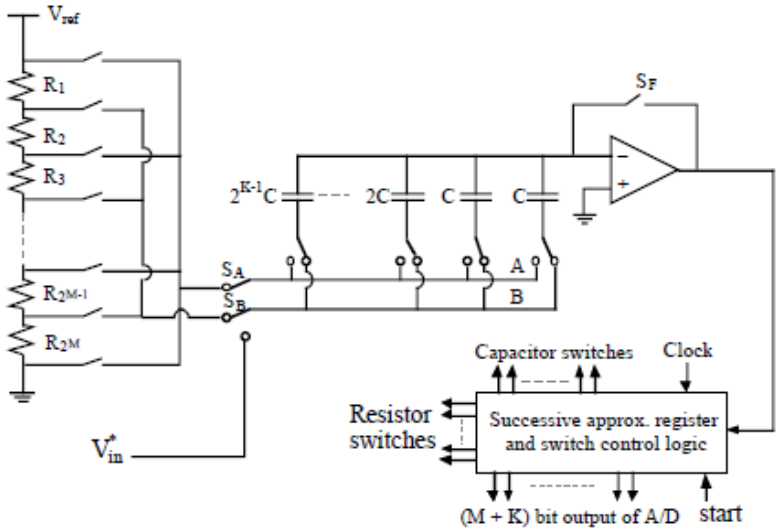
Waveform of the Dual -Slope A/D Converter



1) Very accurate method of A/D conversion.

2) Requires a long time -2(2N) T

A Voltage-Charge Scaling Successive Approximation ADC



Operation:

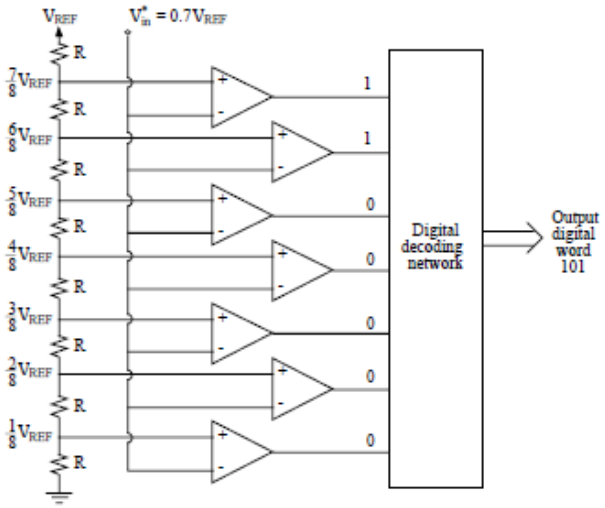
1.) With S_F closed, the bottom plates of all capacitors are connected through switch S_B to Vin^*. (Automatically accounts for voltage offsets).

2.) After S_F is opened, a successive approximation search among the resistor string taps to find the resistor segment in which the stored sample lies.

3.) Buses A and B are then connected across this segment and the capacitor bottom plates are switched in a successive approximation sequence until the comparator input voltage converges back to the threshold voltage.

Capable of 12-bit monotonic conversion with a DL of ±0.5LSB within 50µs.

FLASH A/D CONVERTER



- Fast conversion time, one clock cycle
- Requires 2^{N}-1 comparators
- Maximum practical bits is 6 or less
- 6 bits at 10 MHz is practical

SOURCES OF ERRORS IN ΣΔ A/D CONVERTERS

1. Quantization in time and amplitude
   Jitter and hysteresis
2. Linear Errors
   Gain and delay
3. Nonlinear Errors
   Harmonic distortion
   Thermal noise

Music recording:

Analog-to-digital converters are integral to current music Reproduction technology.

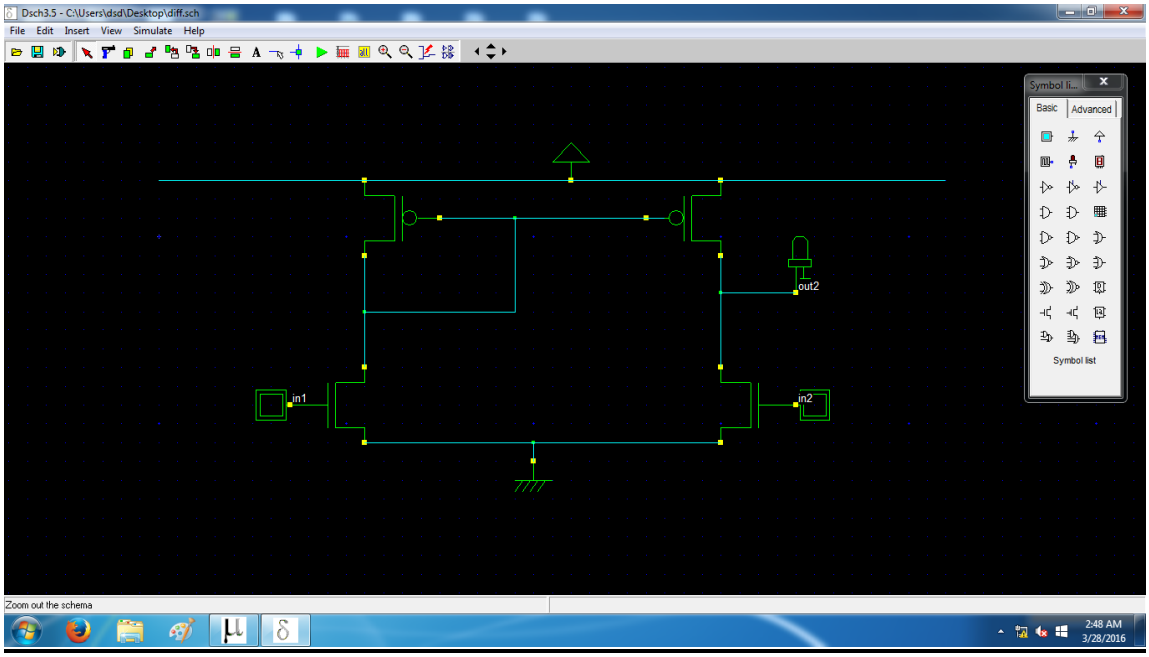
Digital signal processing:

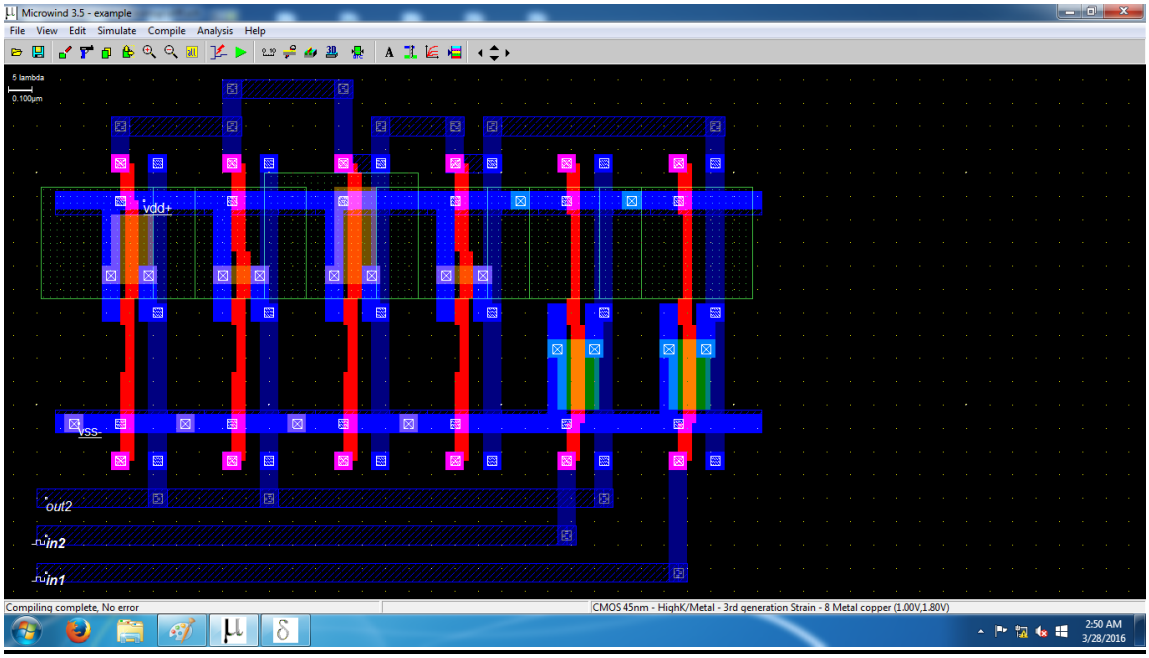
People must use ADCs to process, store, or transport virtually any analog signal in digital form.

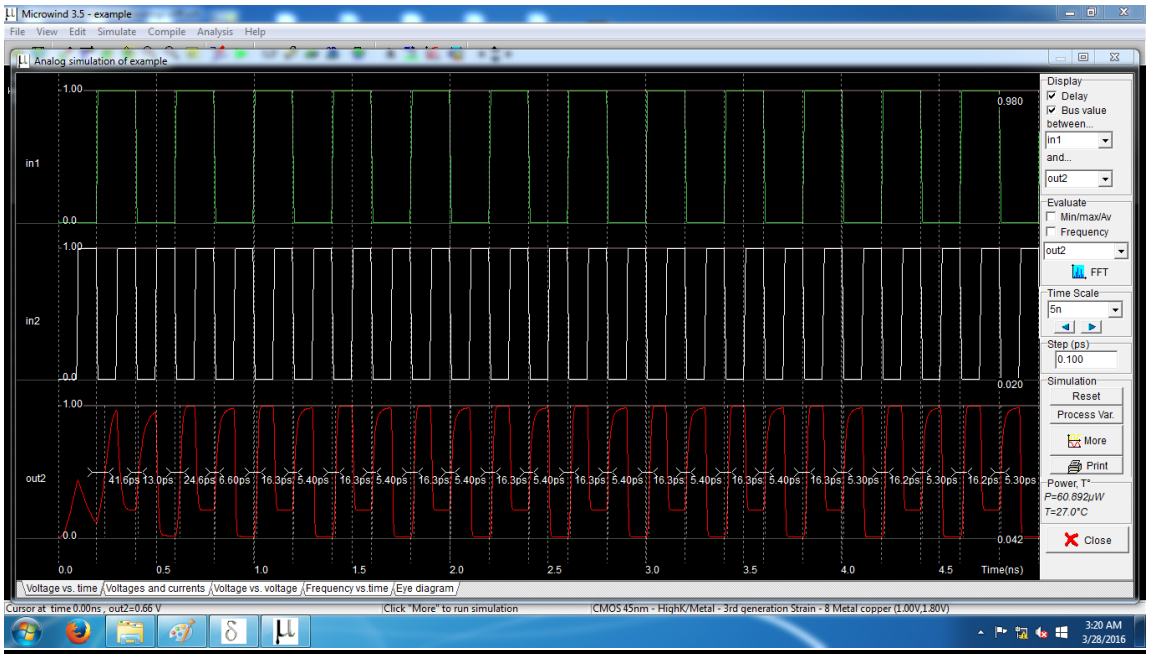
Scientific instruments:

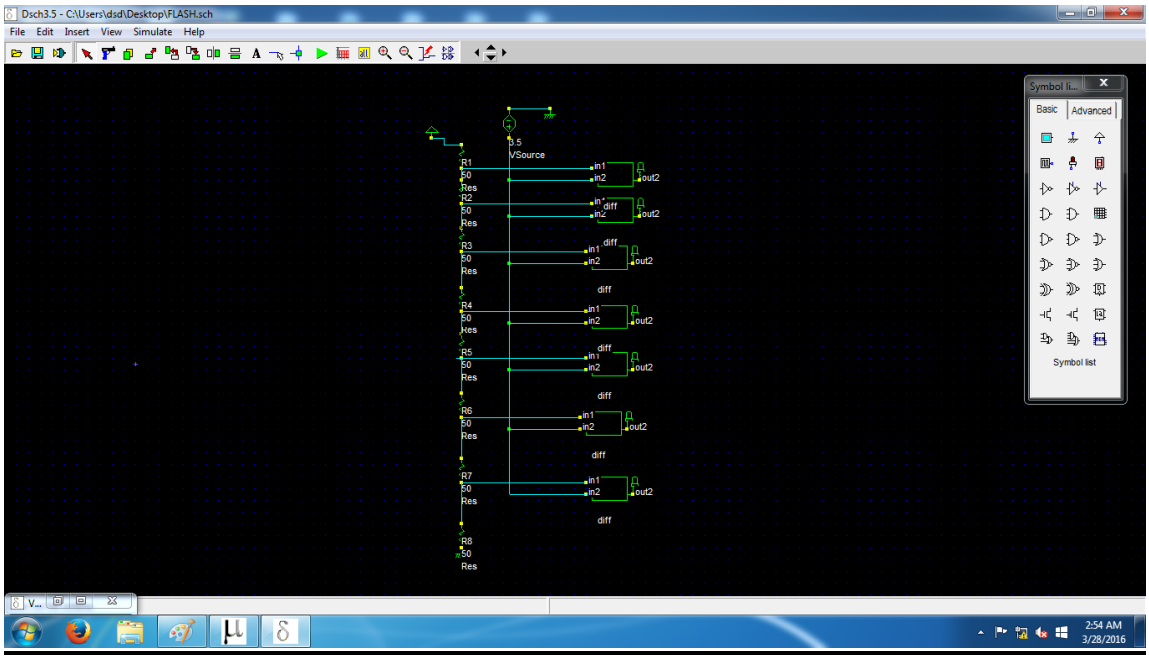
Digital imaging systems commonly use analog-to-digital converters in digitizing pixels.

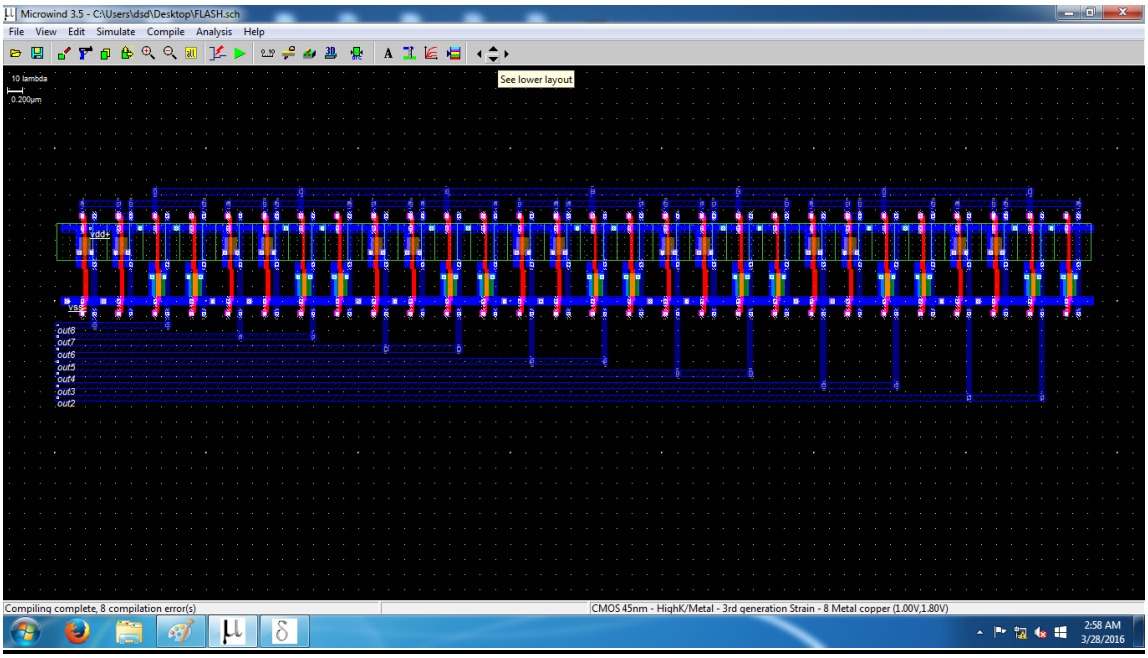
Results

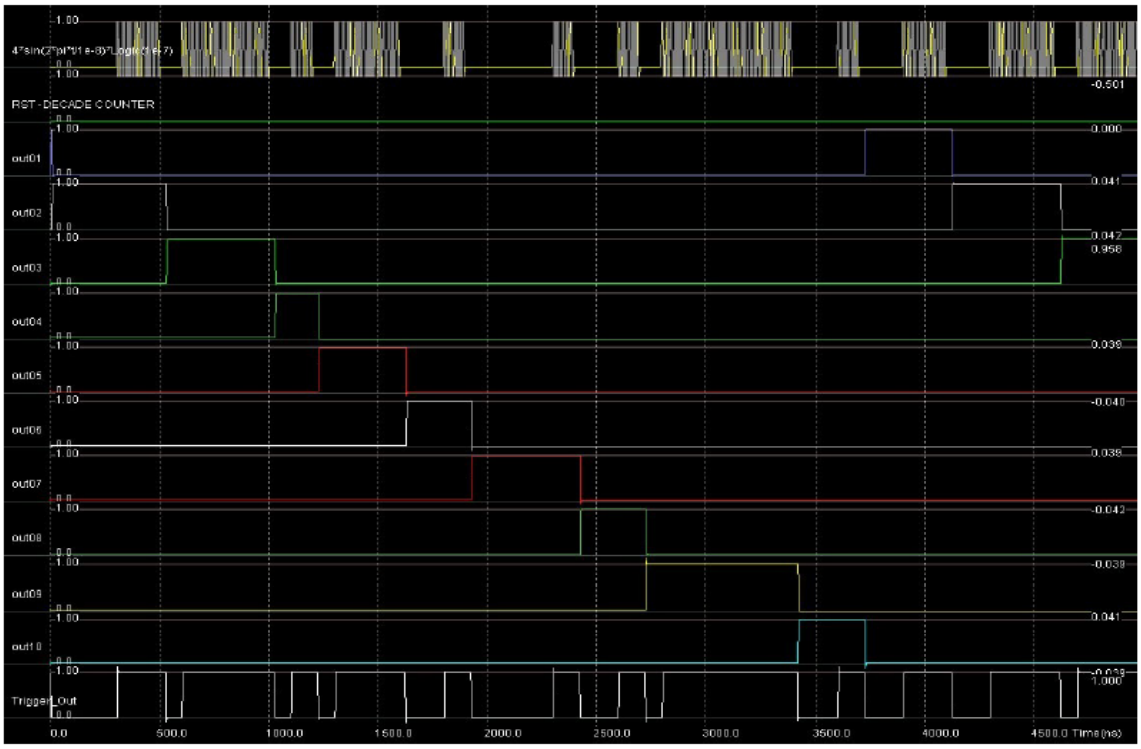

Dsch3.5 - C:\Users\dsd\Desktop\diff.sch
File Edit Insert View Simulate Help
Symbol li...
Basic
Advanced
Symbol list
out2
in1
in2
Zoom out the schema
2:48 AM
3/28/2016


Microwind 3.5 - example
File View Edit Simulate Compile Analysis Help
5 lambda
0.100µm
vdd
vss
out2
in2
in1
Compiling complete, No error
CMOS 45nm - HighK/Metal - 3rd generation Strain - 8 Metal copper (1.00V,1.80V)
2:50 AM
3/28/2016


Microwind 3.5 - example
File View Edit Simulate Compile Analysis Help
Analog simulation of example
in1
in2
out2
1.00
0.0
0.980
0.020
0.042
41.6ps 13.0ps 24.6ps 6.60ps 16.3ps 5.40ps 16.3ps 5.40ps 16.3ps 5.40ps 16.3ps 5.40ps 16.3ps 5.40ps 16.3ps 5.40ps 16.3ps 5.30ps 16.2ps 5.30ps 16.2ps 5.30ps
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 Time(ns)
Display
Delay
Bus value between...
in1
and...
out2
Evaluate
Min/max/Av
Frequency
out2
FFT
Time Scale
5n
Step (ps)
0.100
Simulation
Reset
Process Var.
More
Print
Power, T°
P=60.892µW
T=27.0°C
Close
Voltage vs. time
Voltages and currents
Voltage vs. voltage
Frequency vs.time
Eye diagram
Cursor at time 0.00ns , out2=0.66 V
Click "More" to run simulation
CMOS 45nm - HighK/Metal - 3rd generation Strain - 8 Metal copper (1.00V,1.80V)
3:20 AM
3/28/2016


Dsch3.5 - C:\Users\dsd\Desktop\FLASH.sch
File Edit Insert View Simulate Help
3.5
VSource
R1
R2
R3
R4
R5
R6
R7
R8
50
Res
in1
in2
out2
diff
Symbol li...
Basic
Advanced
Symbol list
2:54 AM
3/28/2016


Microwind 3.5 - C:\Users\dsd\Desktop\FLASH.sch
File View Edit Simulate Compile Analysis Help
See lower layout
10 lambda
0.200µm
vdd
vss
out8
out7
out6
out5
out4
out3
out2
Compiling complete, 8 compilation error(s)
CMOS 45nm - HighK/Metal - 3rd generation Strain - 8 Metal copper (1.00V,1.80V)
2:58 AM
3/28/2016


RST - DECADE COUNTER
out01
out02
out03
out04
out05
out06
out07
out08
out09
out10
Trigger_Out
0.0
500.0
1000.0
1500.0
2000.0
2500.0
3000.0
3500.0
4000.0
4500.0 Time (ns)

Verilog code

```
// DSCH 3.5
// 3/28/2016 2:49:51 AM
// C:\Users\dsd\Desktop\diff.sch
module diff( in2,in1,out2);
 input in2,in1;
 output out2;
 wire w5;
 pmos #(1) pmos_1(out2,vdd,w5); // 0.5u 0.05u
 pmos #(2) pmos_2(w5,vdd,w5); // 0.5u 0.05u
 nmos #(1) nmos_3(out2,vss,in2); // 0.3u 0.05u
 nmos #(2) nmos_4(w5,vss,in1); // 0.3u 0.05u
endmodule
// Simulation parameters in Verilog Format
always
#200 in2=~in2;
#400 in1=~in1;
// Simulation parameters
// in2 CLK 1 1
// in1 CLK 2 2
```

Conclusion

Designing a low power ADC using OP-AMP in Microwind using180nm technology. It will have supply voltage of 1.8V and power consumption of around 35 uW. It will have variance of approximately around 10mW. The OTA adds controllability to the various integrated circuit commonly implemented with conventional OP-AMP. The above OTA has high input impedance and low output impedance, and its size is considerably reduce because there is no need of another circuit for impedance matching. The power consumption of the OTA is also reduced considerably.

Paper Published at IETE Cynosure, NCCEEE-2016.

DESIGN AND ANALYSIS OF MUTI-STAGE OTA & ITS APPLICATION USING 180 nm TECHNOLOGY

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A-I-Kalsekar Technical Campus, Electronics and Telecommunication Department, New Panvel

***Abstract*—The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's trans conductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. Operational Transconductance Amplifier (OTA) is a Op-amp without an output driver. It is capable of driving small capacitive load. This makes the OTA well suited for pipeline application .The design is based on a fully differential, 1.8V OTA to be used in a pipeline ADC which will have power consumption of about 100mW and will be made in 180nm technology.**

Software Tools Used

Xylinx, Microwind & DSCH 3.5.

***Keywords*—OTA, VLSI, DIFF AMP, FPGA.**

I. INTRODUCTION

In high performance analog circuit, it is a very challenging task to design a high performance complementary metal oxide semi-conductor, which is used in either ADC or DAC [1]-[2]. As we are dealing with high performance circuit, to meet these requirement both accuracy and fast settling of system is needed, OP-Amp with high DC gain frequency can satisfy both of these requirement [3]. Although a Op-amp with high DC gain satisfy these requirement, but still in many aspects which leads to complementary demands, as the intrinsic gain of many devices are limited.

OTA is an Op-amp without an output driver. It is capable of driving small capacitive load. These makes $_{OTA}$ a well suitable for pipeline application. The whole procedure is focused on the development of ultra-low power amplifier requiring low silicon area but been able to drive high capacitive load.

Our project consist of three major parts:

- Design of Diff Amp.
- Analysis of Diff Amp.
- Application of Diff Amp and testing result on simulation software's like xylinx, microwind, DSCH 3.5 and executing on FPGA board. (Spartans 3A).

II. DESIGN DESCRIPTION

The Block diagram of the project is mentioned below in fig-1.

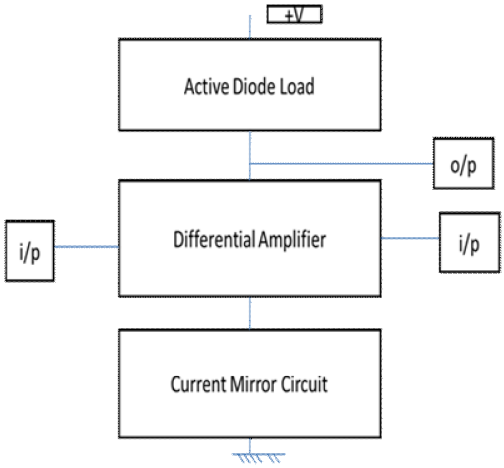


Fig. 1: Block Diagram of Basic OTA.

As from the Block diagram above, it is pretty much evident that the project is distributed into the following major sections,

1.Active load:- when resistor is replaced by an active device which acts as a resistor then this is called active load.

Besides power saving there is additional advantage, because today very large number of circuits are actually in integrated circuit form, in integrated circuits remember one thing that creating one for example, in a unit one mosfet and one resistance is more expensive and it will take more steps for fabrication then two resistors. That means, if we can replace this resistance by a mosfet then the circuit will take two mosfets, but making of two mosfets are in fact, just multiplying in some component is much more economical and convenient in a integrated circuit rather than creating a different element all together resistance and mosfet two are very different elements and two mosfets they are belong to the same category and hence their construction is very simple and more economical.

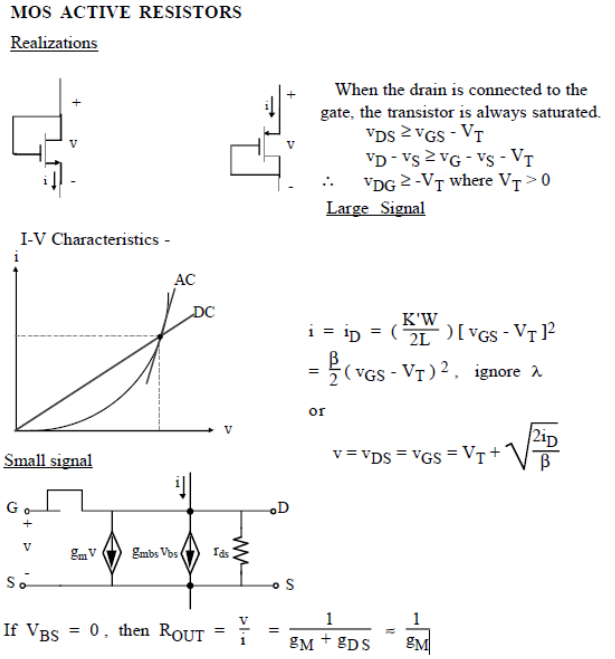


Fig. 2: Charactristics of Active Load

2.Differential Amplifier

A differential amplifier is a type of electronic amplifier that amplifies the difference between two input voltages but suppresses any voltage common to the two inputs. It is an analog circuit with two inputs V_{in}^- and V_{in}^+ and one output V_{out} in which the output is ideally proportional to the difference between the two voltages

$$V_{out} = A(V_{in}^+ - V_{in}^-)$$

where A is the gain of the amplifier.

The differential pair (differential amplifier) configuration

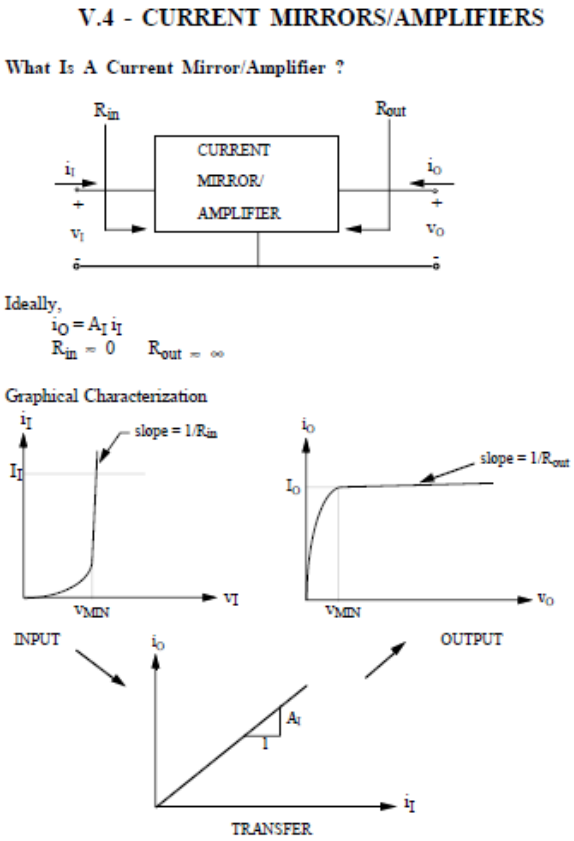
Widely used building block in analog integrated circuit design

- Performance depends critically on the matching of the devices
- Utilizes more components than single-ended circuits
- Well suited for IC fabrication

Advantages of using differential pair

- Less sensitive to noise and interference than single-ended circuits
- Bias is provided without the need for bypass and coupling capacitors.

3.Current mirror.



III. FPGA (FIELD PROGRAMMABLE GATE ARRAY)

Field Programmable Gate Arrays (FPGAs) are highly flexible, reprogrammable logic devices that leverage advanced CMOS manufacturing technologies, similar to

other industry-leading processors and processor peripherals. Like processors and peripherals, Xilinx FPGAs are fully user programmable. For FPGAs, the program is called a *configuration bit stream*, which defines the FPGA's functionality. The bit stream loads into the FPGA at system power-up or upon demand by the system. The process whereby the defining data is loaded or programmed into the FPGA is called *configuration*. Configuration is designed to be flexible to accommodate different application needs and, wherever possible, to leverage existing system resources to minimize system costs. Similar to microprocessors, Xilinx FPGAs optionally load or boot themselves automatically from an external non-volatile memory device. Alternatively, similar to microprocessor peripherals, Spartan-3 generation FPGAs can be downloaded or Programmed by an external "smart agent", such as a microprocessor, DSP processor, microcontroller, PC, or board tester. In either case, the configuration data path is either serial to minimize pin requirements or byte-wide for maximum performance or for easier interfaces to processors or to byte-wide Flash memory. Similar to both processors and processor peripherals, Xilinx FPGAs can be reprogrammed, in system, on demand, an unlimited number of times. After configuration, the FPGA configuration bitstream is stored in highly robust CMOS configuration latches (CCLs). Although CCLs are reprogrammable like SRAM memory, CCLs are designed primarily for data integrity, not for performance. The data stored in CCLs is written only during configuration and remains static unless changed by another configuration event.

This user guide provides both an introduction to the configuration options available to the user, and a detailed description of the configuration logic. This user guide includes the Extended Spartan-3A family, which includes the Spartan-3A, Spartan-3AN, and Spartan- 3A DSP platforms. The user guide also includes the earlier Spartan-3 and Spartan-3E families. Together, these families are sometimes referred to as the Spartan-3 generation. Most basic configuration features are similar between the families, and differences are noted where necessary.

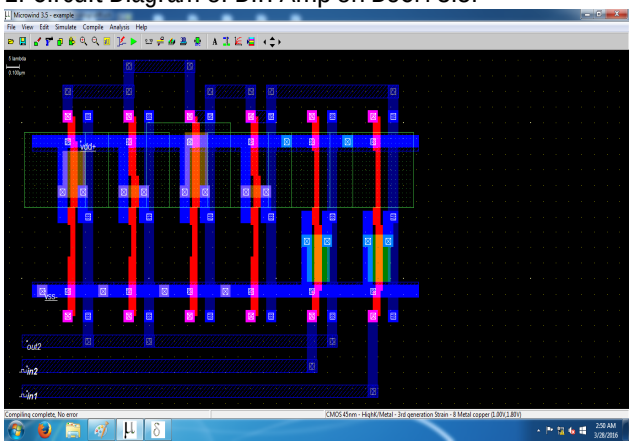
IV. SOFTWARE

Mircowind is truly integrated software encompassing IC designs from concept to completion, enabling chip designer to design beyond their imagination. Microwind integrates traditionally separated frontend and backend chip design into an integrated flow, accelerating the design cycle and reducing the design complexities.
This software allows the designer to simulate and design an integrated circuit at physical description level. Mircowind unifies schematic entry, pattern based simulator, SPICE extraction of schematic Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional and 3D viewer, netlist extraction, to deliver unmatched design performance & productivity.

V. RESULTS

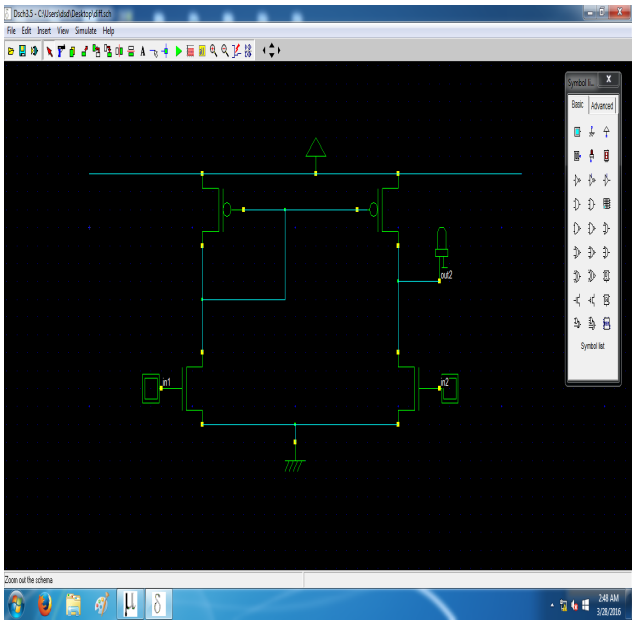
Simulation which were done on softwares like DSCH and microwind, the results of the Diff Amp are shown below:

1. Circuit Diagram of Diff Amp on DSCH 3.5.

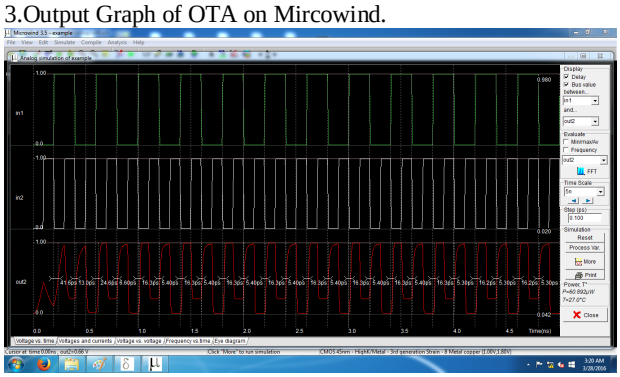


2. Layout of Diff Amp on microwind.

S



3.Output Graph of OTA on Mircowind.



VI. CONCLUSIONS

Design a low power ADC using OTA in Microwind using180nm technology.It will have supply voltage of 1.8V and power consumption of around 100uW. It will have variance of approximately around 10mW.

VII. ACKNOWLEDGEMENT

I am grateful to Prof. Afzal Shaikh and I acknowledge with gratitude to my supervisor Prof. Afzal Shaikh, Department of Electronics & Telecommunication Engineering, and all staff members for his innovative thinking, continuous guidance, genius role and encouragement throughout the whole project period.

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DECLARATION

We hereby declare that the project entitled "DESIGN AND ANALYSIS OF MULTI-STAGE OTA & ITS APPLICATION USING 180nm TECHNOLOGY" submitted for the B.E Degree is our original work and the project has not formed the basis for the award of any degree, associateship, fellowship or any other similar titles.

Signature of the Students:

Mr. SHARIK ABDUL SALIM PATEL (12ET44)

Mr. IRFAN ABDUL KADER SHAIKH (12ET48)

Mr. MOHAMMEDBILAL ABRAR SHAIKH (12ET51)

Mr. SHEMNA NEEHAL (12ET57)

Place:

Date:

CERTIFICATE

This is to certify that the project entitled "DESIGN AND ANALYSIS OF MULTI-STAGE OTA & ITS APPLICATION USING 180nm TECHNOLOGY" is the bonafide work carried out by Sharik, Irfan, Mohammedbilal, Neehal students of B.E, KALSEKAR Technical Campus, Panvel, during the year 2014, in partial fulfillment of the requirements for the award of the Degree of B.E EXTC and that the project has not formed the basis for the award previously of any degree, diploma, associateship, fellowship or any other similar title.

(Prof. Mujib Tamboli)	(Prof. Afzal Shaikh)
H.O.D	Asst. Prof.

(External)

ABSTRACT

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS). There is usually an additional input for a current to control the amplifier's transconductance. The OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback. Operational Transconductance Amplifier (OTA) is a Op-amp without an output driver. It is capable of driving small capacitive load. This makes the OTA well suited for pipeline application. We are designing a fully differential, 1.8V OTA to be used in a pipeline ADC which will have power consumption of about 100mW and will be made in 180nm technology.

ACKNOWLEDGEMENT

We have taken efforts in this project. However, it would not have been possible without the kind support and help of many individuals and institute. We would like to extend our sincere thanks to all of them.

We are highly indebted to (Prof. Afzal Shaikh) for his guidance and constant supervision as well as for providing necessary information regarding the project & also for his support in completing the project. We would like to express our gratitude towards our parents & members of (AIKTC) for their kind co-operation and encouragement which help us in completion of this project.

Our thanks and appreciations also go to our colleague in developing the project and people who have willingly helped us out with their abilities.

Table of Content