A

PROJECT REPORT ON

"ANALYSIS OF INDUCTION MOTOR BY USING CASCADED MULTILEVEL INVERTER"

(INFORMATIVE REPORT)

2015-16

SUBMITTED BY:

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New Panvel

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Submitted to:

Prof. VIVEK TIWARI

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We would like to acknowledge the contributions of those who assisted in the preparation of this report.

We are particularly grateful for the work done by members of my group. Before we get into this report we would like to thanks to the members of the group who are a part of this report and have given their unending contribution from start to end of this report.

We would like to our **Prof. VIVEK TIWARI** for providing as the required guidance in process of preparing the report. We would also like to express our deep regards and gratitude to the director **Dr. ABDUL RAZZAK HONNUTAGI**.

Finally, I would also like to thanks GOOGLE and WIKIPEDIA for the same.

PREFACE

We take the opportunity to present this report "**ANALYSIS OF INDUCTION MOTOR BY USING CASCADED MLTILEVEL INVERTER".** The object of this report is to focus the various method to reduce harmonics.

The report is supported by graphs and images to bring out the purpose and message. We have made sincere attempts and taken every care to present this report in precise and compact form, the language being as simple as possible.

The task of completion of the project though being difficulty was made quite simple, interesting and successful due to deep involvement and complete dedication of our group members.

CERTIFICATE

This is to certify that the report entitled "**ANALYSIS OF INDUCTION MOTOR BY USING CASCADED INVERTER**" submitted by **DAHATONDE AKSHAY DILIP, CHAUDHARY FAIYAZ AHMED, KHAN HAIDAR ALI, MOURYA SATISH KUMAR** in partial fulfillment of the requirement for the award of Bachelor of engineering in "**ELECTRICAL ENGINEERING**" is an authentic word carried by them under my supervision and guidance.

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ABSTRACT

Multilevel inverters had gain popularity over the years in industrial applications such as motor drives, static VAR compensators and renewable energy system. Multilevel inverters have received this attention as it promises less disturbance and possibility to function at lower switching frequency than traditional two level inverters. Out of many level inverters topologies proposed, cascaded multilevel inverters features a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure and modulation. With large numbers of advantages CMI has one major limitations of voltage unbalance across the dc capacitor.

This thesis explores basis structure and operating principles of CMI. Common modulation techniques are summarized. This thesis also presents the total harmonics distortion (THD) analysis of seven level CMI with phase shifted (PS) sinusoidal pulse width modulation (SPWM) and level shifted (LS) SPWM techniques such as phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD). The harmonic spectrum for PS and LS SPWM techniques are compared. Module capacitor voltage balancing algorithm such as sorting strategy is proposed for CMI.

DECLARATION

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

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CHAPTER 1

1.1 INTRODUCTION

Most of the industrial drives use ac induction motor because these motors are rugged, reliable, and relatively inexpensive. Induction motors are mainly used for constant speed applications because of unavailability of the variable frequency supply voltage but many applications need variable speed operations. Present day drive types are the Induction motor drives with voltage source inverters. Also the voltage waveforms of traditional two level inverter fed Induction motor shows that the voltage across the motor contains not only the required “fundamental” sinusoidal components, but also pulses of voltage i.e. “ripple “voltage. The recent advancement in power electronics has initiated to improve the level of inverter instead increasing the size of filter. The total harmonic distortion of the classical inverter is very high. The performance of the multilevel inverter is better than classical inverter. In other words the total harmonic distortion for multilevel inverter is low. The total harmonic distortion is analyzed between multilevel inverter and other classical inverter. To get the speed control of induction motor, we need vary both voltage and current. This technique is called as constant V/F method. By choosing the suitable inverter we can vary both voltage and frequency of the induction motor to get the required speed control. Normally the conventional H-bridge inverter produces a square output, which contains infinite number of odd harmonics and dv/dt stress is also high. Normal PWM inverter can reduces the THD, but Switching losses are high and also this inverter is restricted to low power applications. The importance of multilevel inverters [MLI] has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum and with less THD. Generally MLIs are classified into three types: they are

1.Diode Clamped MLIs

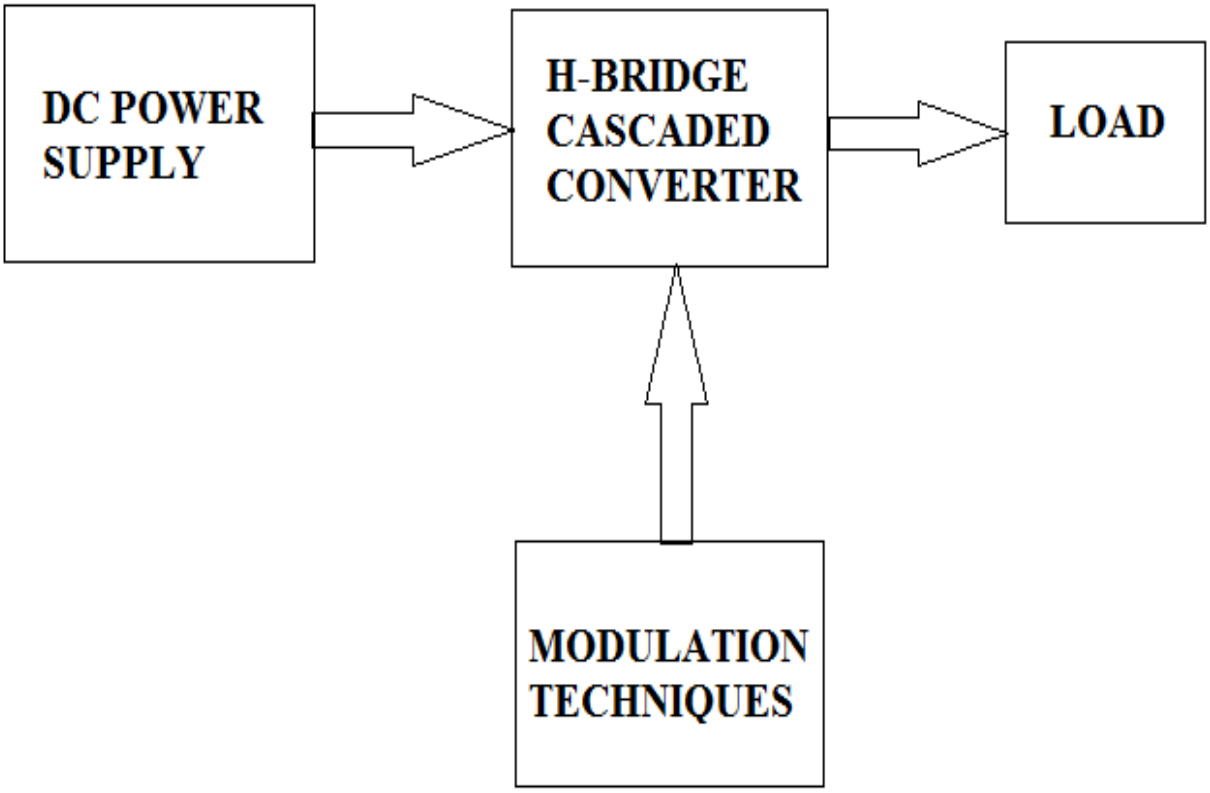
2. Flying capacitor MLIs

3. Cascaded H- bridge MLIs.

Diode clamped MLIs require large number of clamping diodes as the level increases. In flying capacitor MLIs, Switching utilization and efficiency are poor and also it requires large number of capacitors as the level increases and cost is also high.

Cascaded H-bridge MLIs are mostly preferred for high power applications as the regulation of the DC bus is simple. But it requires separate dc sources and also the complexity of the structure is increases as the level predominantly increase. In order to address the above concerns, this paper proposes a new type of multilevel inverter which requires less number of DC sources and switches compared to Cascaded H-bridge MLIs.

1.2 BLOCK DIAGRAM OF CMLI



CHAPTER 2

2.1 Multilevel Inverter structures

A voltage level of three is considered to be the smallest number in multilevel converter topologies. Due to the bi-directional switches, the multilevel VSC can work in both rectifier and inverter modes. This is why most of the time it is referred to as a converter instead of an inverter in this dissertation. A multilevel converter can switch either its input or output nodes (or both) between multiple (more than two) levels of voltage or current. As the number of levels reaches infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage-imbalance problems, voltage clamping requirements, circuit layout and packaging constraints complexity of the controller, and, of course, capital and maintenance costs.

Three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. The multilevel inverter structures are the main focus of discussion in this chapter; however, the illustrated structures can be implemented for rectifying operation as well. Although each type of multilevel converters share the advantages of multilevel voltage source inverters, they may be suitable for specific application due to their structures and drawbacks. Operation and structure of some important type of multilevel converters are discussed in the following sections

. In a multilevel VSI, the dc-link voltage Vdc is obtained from any equipment which can yield stable dc source. Series connected capacitors constitute energy tank for the inverter providing some nodes to which multilevel inverter can be connected. Primarily, the series connected capacitors will be assumed to be any voltage sources of the same value. Each capacitor voltage Vc is given by Vc=Vdc/ (n-1), where n denotes the number of level.

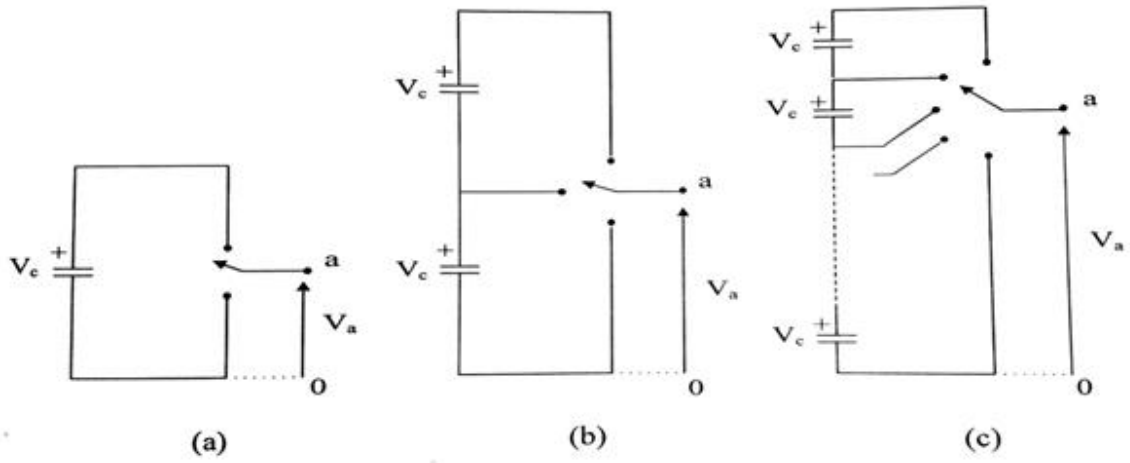


Fig.2.1: One phase leg of an inverter with (a) two level, (b) three level, (c) n level

2.2 Diode-Clamped Multilevel Inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage so as to achieve steps in the output voltage. The neutral point converter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. A three-level diode clamped inverter consists of two pairs of switches and two diodes. Each switch pairs works in complimentary mode and the diodes used to provide access to mid-point voltage. In a three-level inverter each of the three phases of the inverter shares a common dc bus, which has been subdivided by two capacitors into three levels. The DC bus voltage is split into three voltage levels by using two series connections of DC capacitors, C1 and C2. The voltage stress across each switching device is limited to Vdc through the clamping diodes Dc1 and Dc2.

It is assumed that the total dc link voltage is Vdc and mid-point is regulated at half of the dc link voltage, the voltage across each capacitor is Vdc/2 (Vc1=Vc2=Vdc/2). In a three level diode clamped inverter, there are three different possible switching states which apply the stair case voltage on output voltage relating to DC link capacitor voltage rate. For a three-level inverter, a set of two switches is on at any given time and in a five-level inverter, a set of four switches is on at any given time and so on.

Fig-2.2 shows the circuit for a diode clamped inverter for a three-level and a five-level inverter.

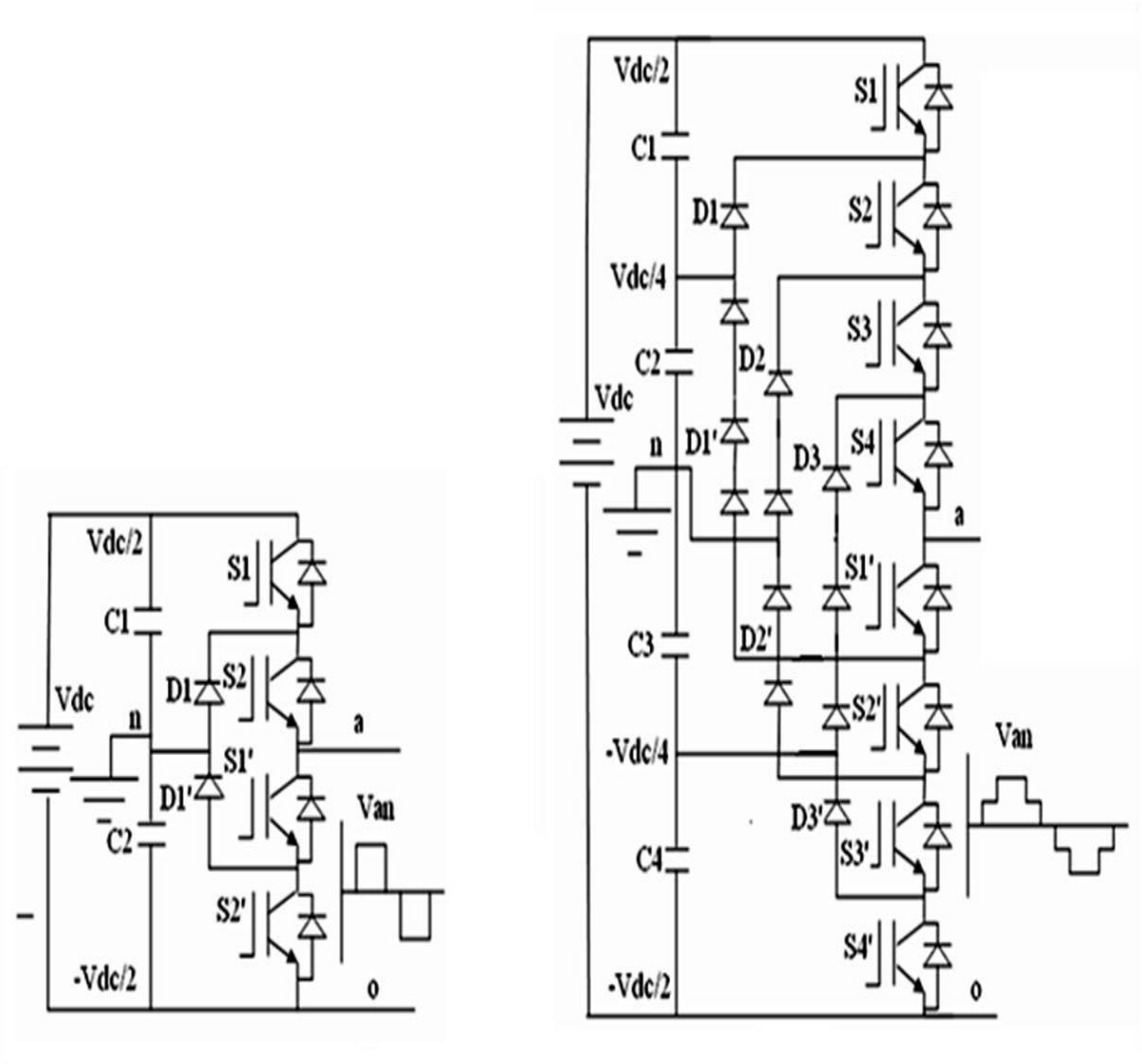


Fig 2.2: Topology of the diode-clamped inverter (a) three-level inverter, (b) five -level inverter.

Switching states of the three level inverter are summarized in table-1.

Table-2.2. Switching states in one leg of the three-level diode clamped inverter

Switch Status	State	Pole Voltage
S1=ON,S2=ON S1'=OFF,S2′=OFF	S=+ve	Vao=Vdc/2
S1=OFF,S2=ON S1'=ON,S2′=OFF	S=0	Vao=0
S1=OFF,S2=OFF S1'=ON,S2′=ON	S= -ve	Vao=-Vdc/2

Fig 2.2 shows the phase voltage and line voltage of the three-level inverter in the balanced condition. The line voltage Vab consists of a phase-leg *a* voltage and a phase-leg *b* voltage. The resulting line voltage is a 5-level staircase waveform for three-level inverter and 9-level staircase waveform for a five-level inverter. This means that an N-level diode-clamped inverter has an N-level output phase voltage and a (2N-1)-level output line voltage. In general the voltage across each capacitor for an N level diode clamped inverter at steady state is Vdc/ (N-1). Although each active switching device is required to block only a voltage level of Vdc, the clamping diodes require different ratings for reverse voltage blocking.

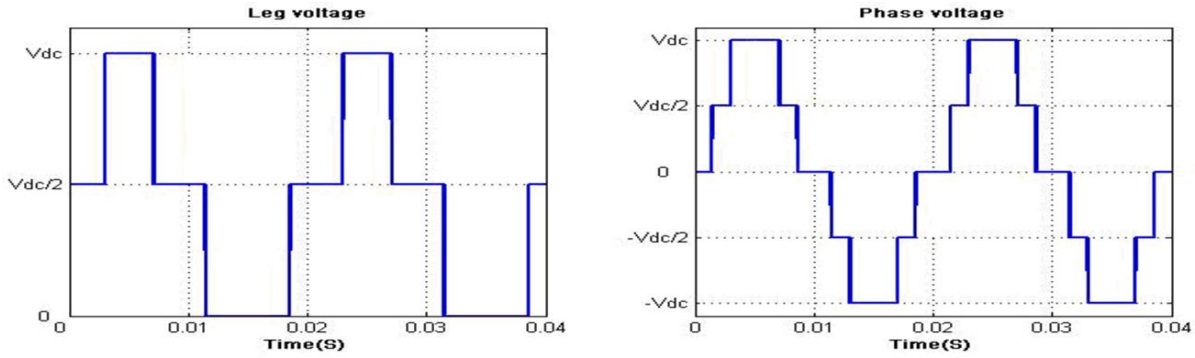


Fig: 2.2. Output voltage in three-level diode- clamped inverter (a) leg voltage (b) output phase voltage

Switching states of the five level inverter are summarized in table-2.2.

Table-2.2. Switching states in one leg of the five-level diode clamped inverter

Voltage Vao	Switch state							
	S1	S2	S3	S4	S1‟	S2‟	S3‟	S4”
Vao=Vdc	1	1	1	1	0	0	0	0
Vao=Vdc/2	0	1	1	1	1	0	0	0
Vao=0	0	0	1	1	1	1	0	0
Vao=Vdc/2	0	0	0	1	1	1	1	0
Vao=-Vdc	0	0	0	0	1	1	1	1

To explain how the staircase voltage is synthesized, the neutral point n is considered as the output phase voltage reference point. There are five switch combinations to synthesize five level voltages across a and n.

1) Voltage level Van= Vdc; turn on all upper switches S1, S2, S3 and S4.

2) Voltage level Van= Vdc/2, turn on the switches S2, S3, S4 and S1′.

3) Voltage level Van= 0, turn on the switches S3, S4, S1′ and S2′.

4) Voltage level Van= - Vdc/2 turn on the switches S4, S1′, S2′, S3′.

5) Voltage level Van= - Vdc; turn on all lower switches S1′, S2′ S3′ and S4′.

2.2.1 Advantages:

1. All of the phases share a common dc bus, which minimizes the capacitance requirements of the converter. For this reason, a back-to-back topology is not only possible but also practical for uses such as a high-voltage back-to-back inter-connection or an adjustable speed drive.

2. The capacitors can be pre-charged as a group.

3. Efficiency is high for fundamental frequency switching.

4. When the number of levels is high enough, harmonic content will be low enough to avoid the need for filters

2.2.2 Disadvantages:

1. Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.

2. The number of clamping diodes required is quadratically related to the number of levels, which can be cumbersome for units with a high number of levels.

2.3 Flying Capacitor Structure.

The capacitor clamped inverter alternatively known as flying capacitor was proposed by Meynard and Foch in 1992. The structure of this inverter is similar to that of the diode-clamped inverter except that instead of using clamping diodes, the inverter uses capacitors in their place. The flying capacitor involves series connection of capacitor clamped switching cells. This topology has a ladder structure of dc side capacitors, where the voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. Figure 2.4 shows the three-level and five-level capacitor clamped inverters respectively. phase to positive node V3 occurs when S1 and S2 are turned on and to the neutral point voltage when S2 and S1′ are turned on. The negative node V1 is connected when S1′ and S2′are turned on. The clamped capacitor C1 is charged when S1 and S1′ are turned on and is discharged when S2 and S2′ are turned on. The charge of the capacitor can be balanced by proper selection of the zero states. In comparison to the three-level diode-clamped inverter, an extra switching state is possible. In particular, there are two transistor states, which make up the level V3. Considering the direction of the a-phase flying capacitor current Ia for the redundant states, a decision can be made to charge or discharge the capacitor and therefore, the capacitor voltage can be regulated to its desired value by switching within the phase. As with the three-level flying capacitor inverter, the highest and lowest switching states do not change the charge of the

capacitors. The two intermediate voltage levels contain enough redundant states so that both capacitors can be regulated to their ideal voltages.

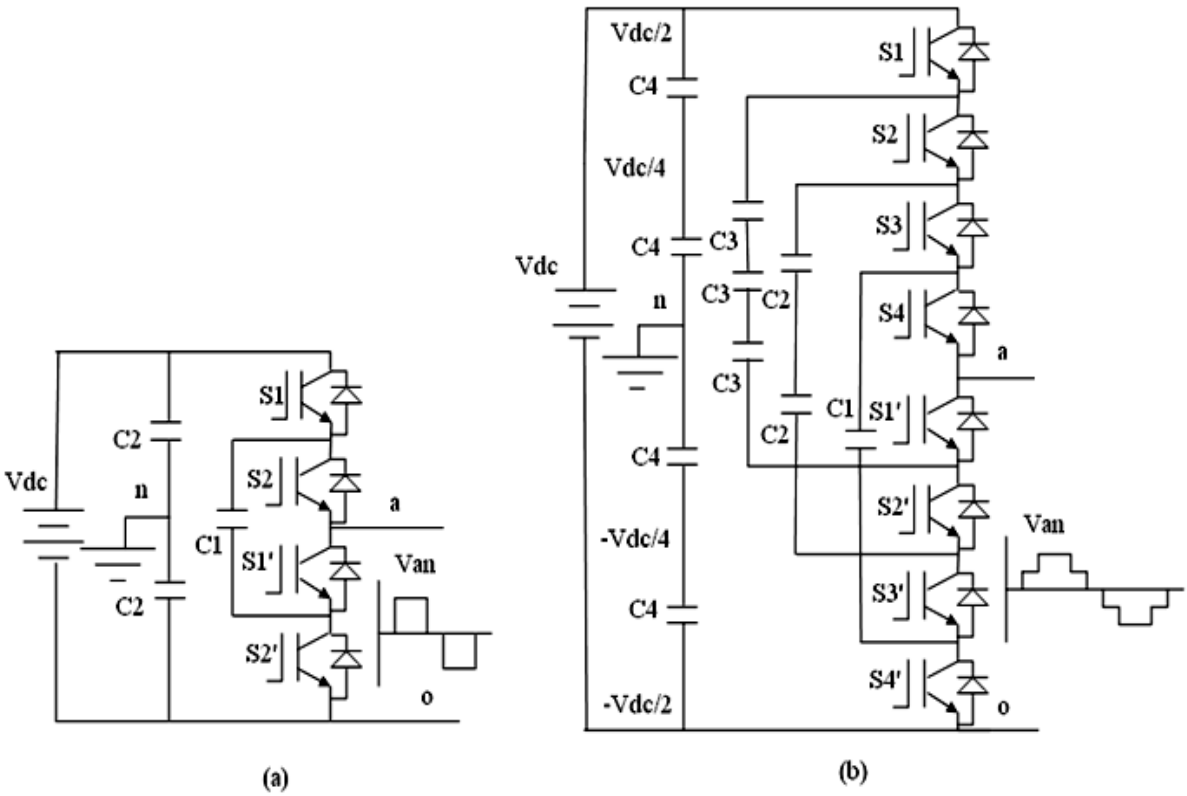


Fig.2.3 Capacitor-clamped multilevel inverter circuit topologies, (a) 3-level inverter (b) 5- level inverter

Table-2.3: Switching states of the five level flying capacitor multilevel inverter

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
Vdc/2	1	1	1	1	0	0	0	0
Vdc/4	1	1	1	0	1	0	0	0
0	1	1	0	0	1	1	0	0
-Vdc/4	1	0	0	0	1	1	1	0
-Vdc/2	0	0	0	0	1	1	1	1

In the operation of flying capacitor multi-level inverter, each phase node (a, b, or c) can be connected to any node in the capacitor bank (V3, V2, V1). Connection of the a- Similar to the diode clamped inverter, the capacitor clamping requires a large number of bulk capacitors to clamp the voltage. Provided that the voltage rating of each capacitor used is the same as that of the main power switch, an N level converter will require a total of (N-1) * (N-2) / 2 clamping capacitors per phase in addition to the (N-1) main dc bus capacitors. Unlike the diode-clamped inverter, the flying-capacitor inverter does not require all of the switches that are on (conducting) in a consecutive series. Moreover, the flying-capacitor inverter has phase redundancies, whereas the diode-clamped inverter has only line-line redundancies [1,3]. These redundancies allow a choice of charging/discharging specific capacitors and can be incorporated in the control system for balancing the voltages across the various levels

The voltage synthesis in a five-level capacitor-clamped converter has more flexibility than a diode-clamped converter. Using Fig. 2.4(b) as the example, the voltage of the five-level phase-leg „a‟ output with respect to the neutral point n (i.e.Van), can be synthesized by the following switch combinations.

1) Voltage level Van= Vdc/2, turn on all upper switches S1 - S4.
2) Voltage level Van= Vdc/4, there are three combinations.
a) Turn on switches S1, S2, S3 and S1′. (Van= Vdc/2 of upper C4‟s - Vdc/4 of C1‟s).
b) Turn on switches S2, S3, S4 and S4’. (Van= 3Vdc/4 of upper C3‟s - Vdc/2 of C4‟s).
c) Turn on switches S1, S3, S4 and S3′. (Van= Vdc/2 of upper C4‟s - 3Vdc/4 or C3‟s + Vdc/2 of upper C2„).
3) Voltage level Van= 0, turn on upper switches S3, S4, and lower switch S1′, S2′.
4)Voltage level Van= -Vdc/4, turn on upper switch S1 and lower switches S1′, S2′and S3′.
5) Voltage level Van= -Vdc/2, turn on all lower switches S1′, S2′, S3′ and S4′.

2.3.1 Advantages:

i) Added clamping diodes are not needed.

ii) It has switching redundancy within the phase, which can be used to balance the flying capacitors so that only one dc source is needed.

iii) The required number of voltage levels can be achieved without the use of the transformer. This assists in reducing the cost of the converter and again reduces power loss.

iv) Unlike the diode clamped structure where the series string of capacitors share the same voltage, in the capacitor-clamped voltage source converter the capacitors within a phase leg are charged to different voltage levels.

v) Real and reactive power flow can be controlled.

vi) The large number of capacitors enables the inverter to ride through short duration outages and deep voltage sags.

2.3.2 Disadvantages

i) Converter initialization i.e., before the converter can be modulated by any modulation scheme the capacitors must be set up with the required voltage level as the initial charge. This complicates the modulation process and becomes a hindrance to the operation of the converter.

ii) Control is complicated to track the voltage levels for all of the capacitors.

iii) Recharging all of the capacitors to the same voltage level and startup are complex.

iv) Switching utilization and efficiency are poor for real power transmission.

v) Since the capacitors have large fractions of the dc bus voltage across them, rating of the capacitors are a design challenge.

vi) The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters.

2.4 Cascaded multilevel inverter

One more alternative for a multilevel inverter is the cascaded multilevel inverter or series H-bridge inverter. The series H-bridge inverter appeared in 1975. Cascaded multilevel inverter was not fully realized until two researchers, Lai and Peng. They patented it and presented its various advantages in 1997. Since then, the CMI has been utilized in a wide range of applications. With its modularity and flexibility, the CMI shows superiority in high-power applications, especially shunt and series connected FACTS controllers. The CMI synthesizes its output nearly sinusoidal voltage waveforms by combining many isolated voltage levels. By adding more H-bridge converters, the amount of Var can simply increased without redesign the power stage, and build-in redundancy against individual H-bridge converter failure can be realized.

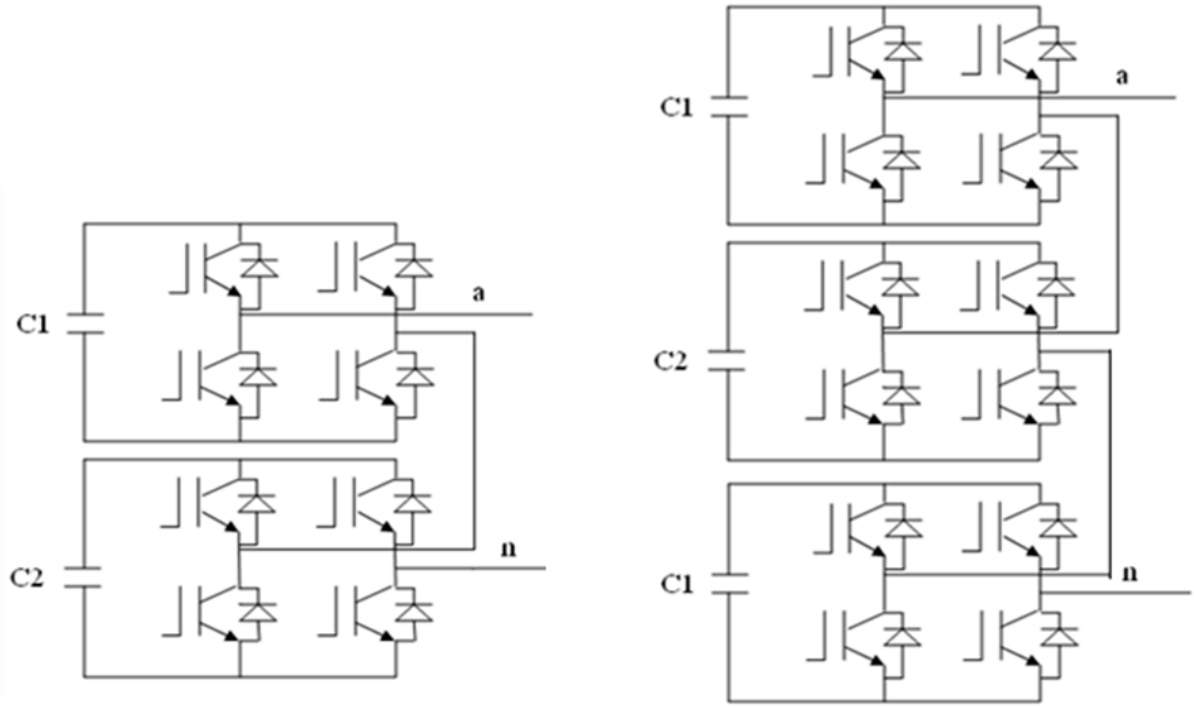


Fig 2.4: Single phase structures of Cascaded inverter (a) 5-level, (b) 7-level

A series of single-phase full bridges makes up a phase for the inverter. A three-phase CMI topology is essentially composed of three identical phase legs of the series-chain of H-bridge converters, which can possibly generate different output voltage

waveforms and offers the potential for AC system phase-balancing. This feature is impossible in other VSC topologies utilizing a common DC link. Since this topology consists of series power conversion cells, the voltage and power level may be easily scaled. The dc link supply for each full bridge converter is provided separately, and this is typically achieved using diode rectifiers fed from isolated secondary windings of a three-phase transformer. Phase-shifted transformers can supply the cells in medium-voltage systems in order to provide high power quality at the utility connection.

2.4.1 Operation of CMLI.

The converter topology is based on the series connection of single-phase inverters with separate dc sources. Fig. 2.5 shows the power circuit for one phase leg of a three-level , five-level and seven-level cascaded inverter. The resulting phase voltage is synthesized by the addition of the voltages generated by the different cells. In a 3-level cascaded inverter each single-phase full-bridge inverter generates three voltages at the output: +Vdc, 0, -Vdc (zero, positive dc voltage, and negative dc voltage). This is made possible by connecting the capacitors sequentially to the ac side via the power switches. The resulting output ac voltage swings from -Vdc to +Vdc with three levels, -2Vdc to +2Vdc with five-level and -3Vdc to +3Vdc with seven-level inverter. The staircase waveform is nearly sinusoidal, even without filtering.

2.4.2 Advantages:

i)The regulation of the DC buses is simple.

ii) Modularity of control can be achieved. Unlike the diode clamped and capacitor clamped inverter where the individual phase legs must be modulated by a central controller, the full-bridge inverters of a cascaded structure can be modulated separately.

iii) Requires the least number of components among all multilevel converters to achieve the same number of voltage levels.

iv) Soft-switching can be used in this structure to avoid bulky and lossy resistor-capacitor-diode snubbers.

2.4.3 Disadvantages:

i) Communication between the full-bridges is required to achieve the synchronization of reference and the carrier waveforms.

ii) Needs separate dc sources for real power conversions, and thus its applications are somewhat limited

CHAPTER 3

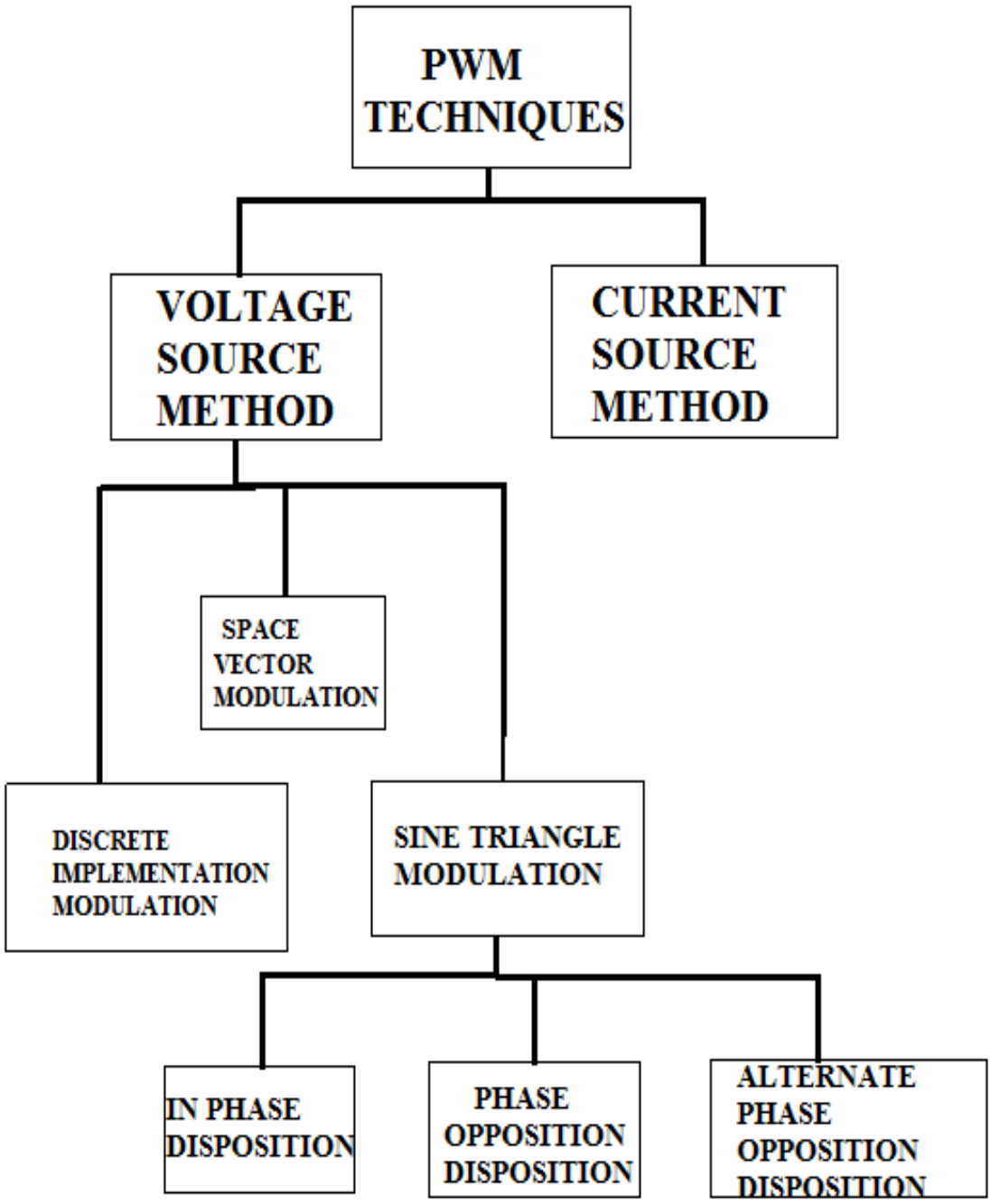
3.1 A Definition of Modulation.

Mainly the power electronic converters are operated in the “switched mode”. Which means the switches within the converter are always in either one of the two states - turned off (no current flows), or turned on (saturated with only a small voltage drop across the switch). Any operation in the linear region, other than for the unavoidable transition from conducting to non-conducting, incurs an undesirable loss of efficiency and an unbearable rise in switch power dissipation. To control the flow of power in the converter, the switches alternate between these two states (i.e. on and off). This happens rapidly enough that the inductors and capacitors at the input and output nodes of the converter average or filter the switched signal. The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses.

For maximum attenuation of the switching component, the switch frequency *fc* should be high- many times the frequency of the desired fundamental AC component f1 seen at the input or output terminals. In large converters, this is in conflict with an upper limit placed on switch frequency by switching losses. For GTO converters, the ratio of switch frequency to fundamental frequency fc/f1 (= N, the pulse number) may be as low as unity, which is known as square wave switching. Another application where the pulse number may be low is in converters which are better described as amplifiers, whose upper output fundamental frequency may be relatively high. These high power switch-mode amplifiers find application in active power filtering, test signal generation, servo and audio amplifiers. These low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible.

The low pulse numbers place the greatest demands on effective modulation to reduce the distortion as much as possible. In these circumstances, multi-level converters can reduce the distortion substantially, by staggering the switching instants of the multiple switches and increasing the apparent pulse number of the overall converter.

3.2 Classification of Multilevel Modulation Methods



3.3 PWM Techniques

The fundamental methods of pulse-width modulation (PWM) are divided into the traditional voltage-source and current-regulated methods. Voltage-source methods more easily lend themselves to digital signal processor (DSP) or programmable logic device (PLD) implementation. However, current controls typically depend on event scheduling and are therefore analog implementations which can only be reliably operated up to a certain power level. In discrete current-regulated methods the harmonic performance is not as good as that of voltage-source methods. A sample PWM method is described below.

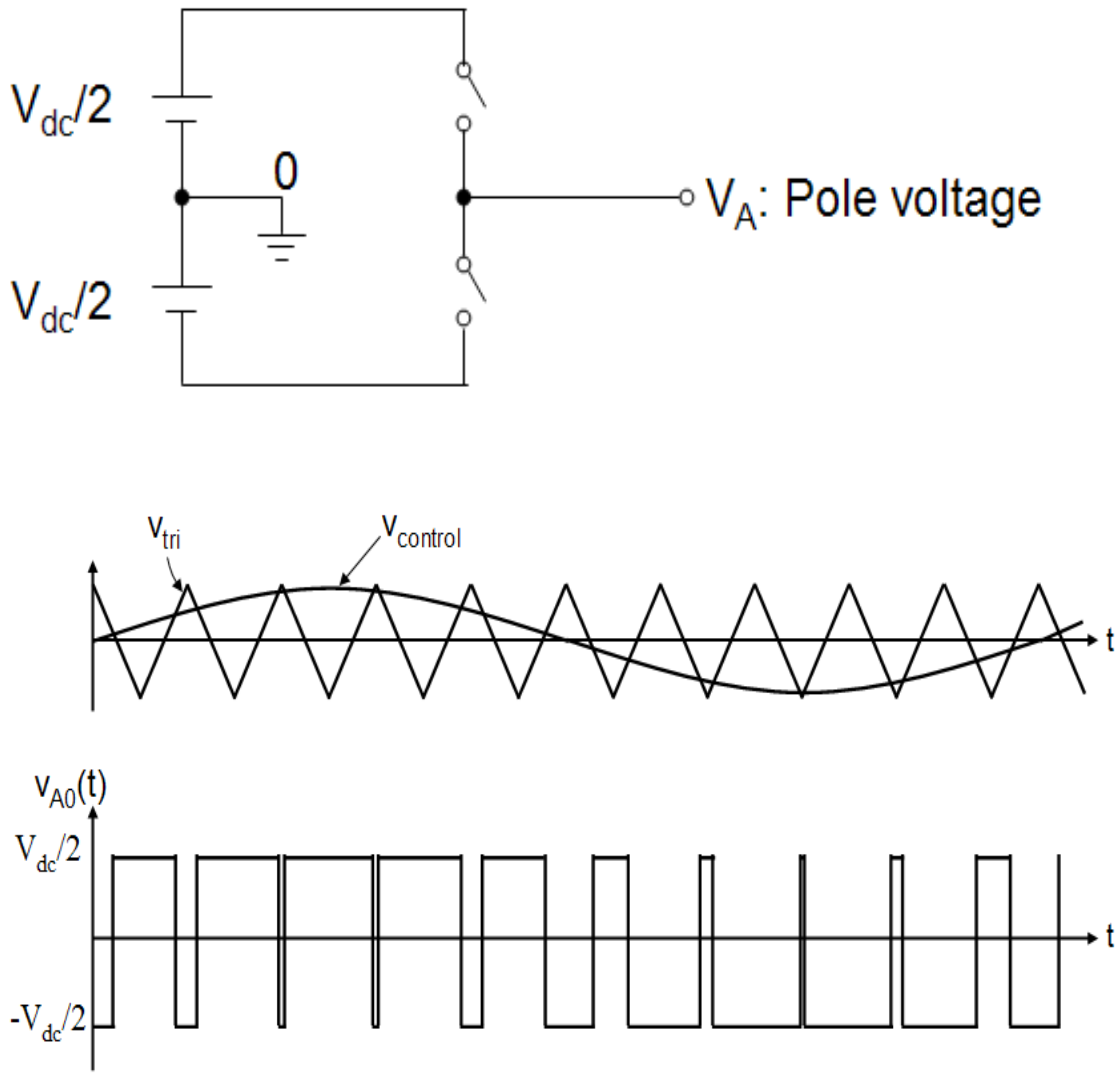


Fig. 3.1 Pulse-width modulation.

Inverter output voltage, VA0 = Vdc/2, When vcontrol > vtri, and

VA0 = -Vdc/2, When vcontrol < vtri.

PWM frequency is the same as the frequency of vtri. Amplitude is controlled by the peak value of vcontrol and Fundamental frequency is controlled by the frequency of vcontrol.

3.4 Voltage-source method

Voltage-source modulation has taken two major paths; sine triangle modulation in the time domain and space vector modulation in the q-d stationary reference frame. Sine-triangle and space vector modulation are exactly equivalent in every way. Adjusting some parameters in the sine-triangle scheme (such as the triangle shape and sine wave harmonics) is equivalent to adjusting other parameters in the space vector scheme (such as the switching sequence and dwell time).

The inverter line-to-ground voltage can be directly controlled through the switching state. For a specific inverter, the switching state is broken out into transistor signals. However, as a control objective, it is more desirable to regulate the line-to-neutral voltages of the load. In a three-phase system, the common terms include dc offset and any triplen harmonics. To narrow the possibilities, the commanded line-to-ground voltages will be defined herein as:

(I) Sine-triangle modulation

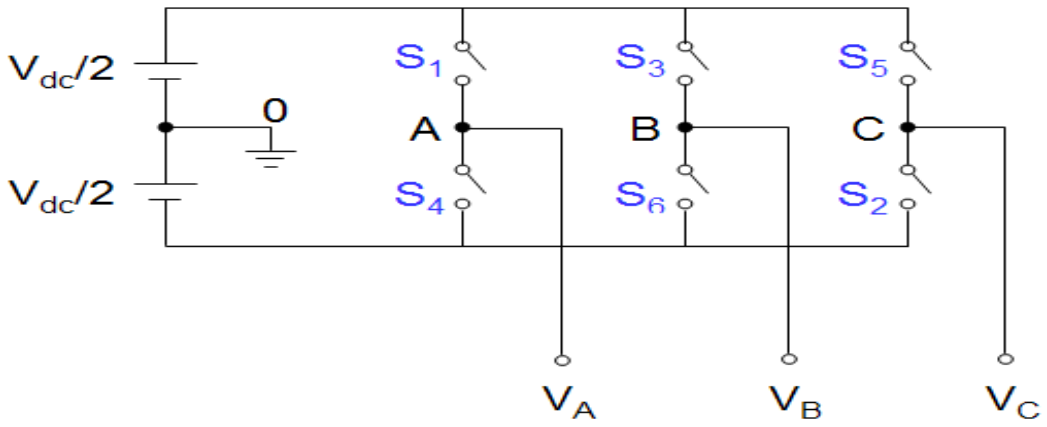


Fig. 3.2 Three-phase Sinusoidal PWM inverter

The carrier-based modulation schemes for multilevel inverters can be generally classified into two categories: phase-shifted and level-shifted modulations. Both modulation schemes can be applied to the cascaded H-bridge(CHB) inverters.THD of phase-shifted modulation is much higher than level-shifted modulation. Therefore we have considered level-shifted modulation. An m-level CHB inverter using level-shifted multicarrier modulation scheme requires (m-1) triangular carriers, all having the same frequency and amplitude. The (m-1) triangular carriers are vertically disposed such that the bands they occupy are contiguous. There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

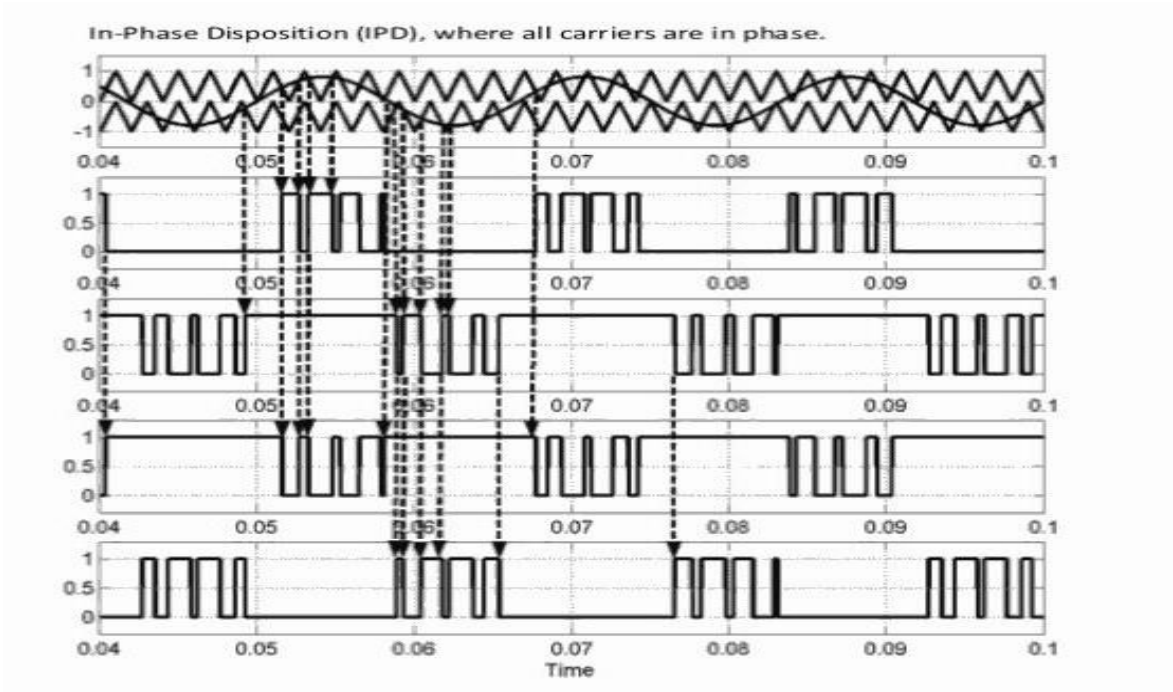
(i) In-phase disposition (IPD), where all carrier waveforms are in phase.

(ii) Phase opposition disposition (POD),

where all carrier waveforms above zero reference are in phase and are 1800 out of phase with those below zero.

(iii) Alternate phase disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 1800.

a) In Phase Disposition (IPD)



In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Figure demonstrates the sine-triangle method for a three-level inverter. Therein, the a-phase modulation signal is compared with two (n-1 in general) triangle waveforms.

The rules for the in phase disposition method, when the number of level N = 3, are

• The N –1 = 3-1=2 carrier waveforms are arranged so that every carrier is in phase.

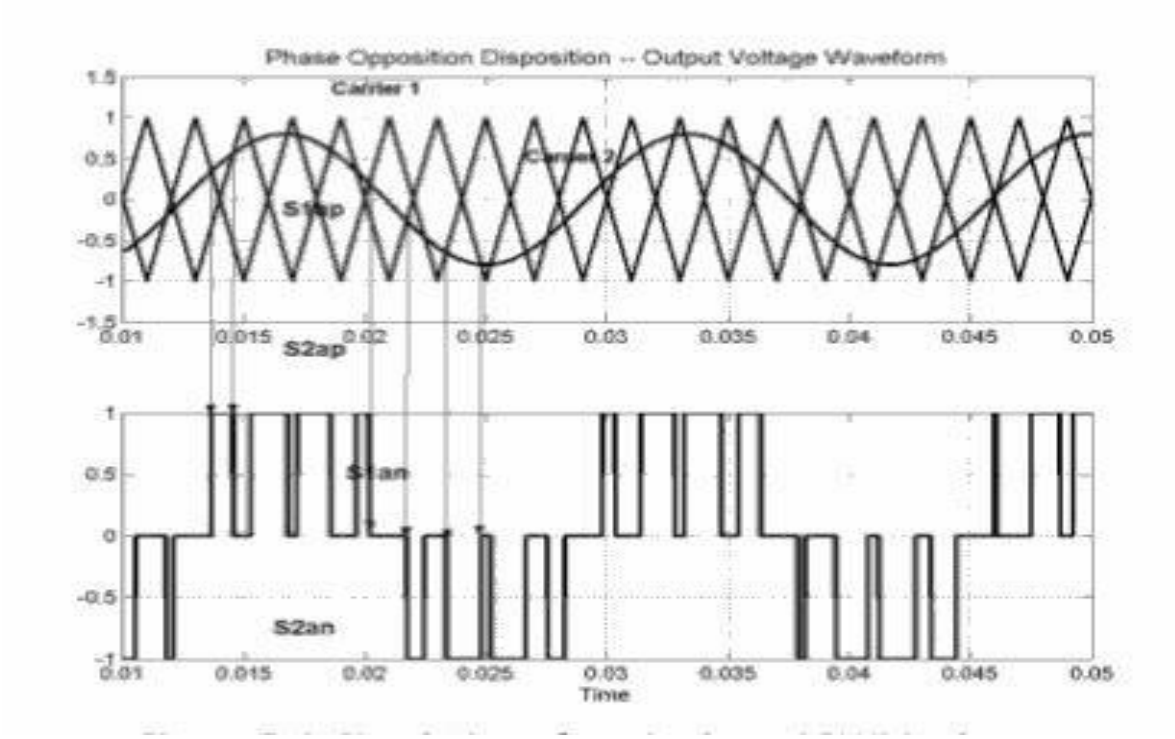
• The converter is switched to +Vdc/ 2 when the reference is greater than both carrier waveforms.

• The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

• The converter is switched to - Vdc/ 2 when the reference is less than both carrier waveforms.

In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated.

b) Phase Opposition Disposition (POD).



For phase opposition disposition (POD) modulation all carrier waveforms above zero reference are in phase and are 1800 out of phase with those below zero. The rules for the phase opposition disposition method, when the number of level N = 3 are;

(i) The N –1 = 2 carrier waveforms are arranged so that all carrier waveforms above zero are in phase and are 1800 out of phase with those below zero.

(ii) The converter is switched to + Vdc / 2 when the reference is greater than both carrier waveforms.

(iii) The converter is switched to zero when the reference is greater than the lower carrier waveform but less than the upper carrier waveform.

(iv) The converter is switched to - Vdc / 2 when the reference is less than both carrier waveforms.

As seen from Figure, the figure illustrates the switching functions produced by POD carrier-based PWM scheme. In the PWM scheme there are two triangles, upper triangle magnitude from 1 to 0 and the lower triangle from 0 to –1 and these two triangle waveforms are in out of phase. When the modulation signal is greater than both the carrier waveforms, S1ap and S2ap are turned on and the converter switches to positive node voltage and when the reference is less than the upper carrier waveform but greater than the lower carrier, S2ap and S1an are turned on and the converter switches to neutral point. When the reference is lower than both carrier waveforms, S1an and S2an are turned on and the converter switches to negative node voltage. . Figure shows the output voltage waveform of phase “a” and it is clear the waveform has three steps.

(C) Alternate Phase Opposition Disposition(APOD)

In case of alternate phase disposition (APOD) modulation, every carrier waveform is in out of phase with its neighbor carrier by 1800. Since APOD and POD schemes in case of three-level inverter are the same, a five level inverter is considered to discuss about the APOD scheme.

The rules for APOD method, when the number of level N = 5, are:

i) The N – 1 = 4 carrier waveforms are arranged so that every carrier waveform is in out of phase with its neighbor carrier by 1800. The converter switches to + Vdc / 2 when the reference is greater than all the carrier waveforms.

(ii) The converter switches to Vdc / 4 when the reference is less than the uppermost carrier waveform and greater than all other carriers.

(iii) The converter switches to 0 when the reference is less than the two uppermost carrier waveform and greater than two lowermost carriers.

(iv) The converter switches to - Vdc / 4 when the reference is greater than the lowermost carrier waveform and lesser than all other carriers.

(v) The converter switches to -Vdc / 2 when the reference is lesser than all the carrier waveforms.

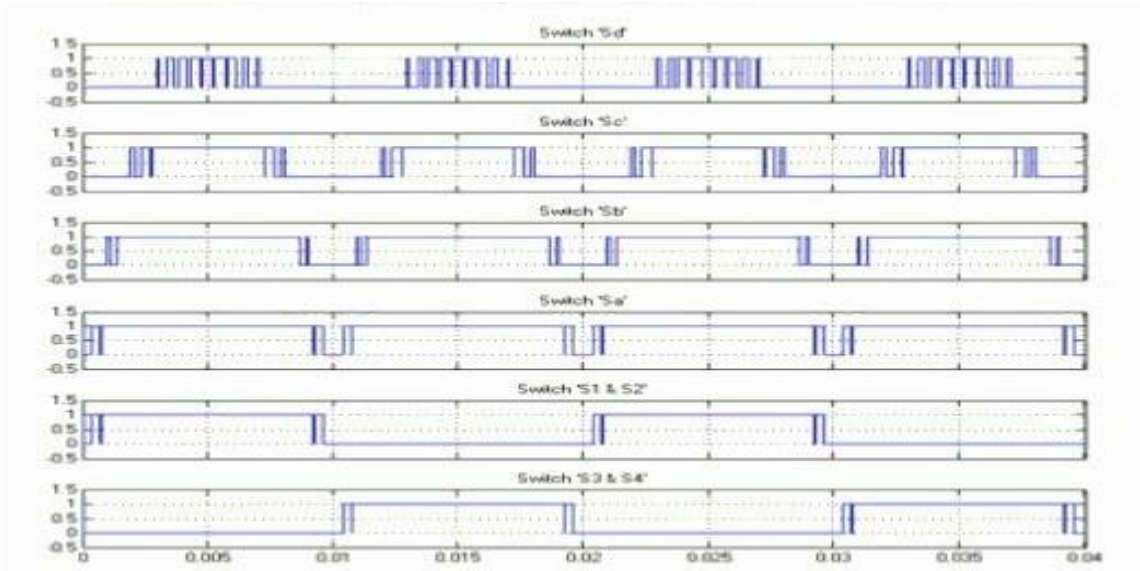
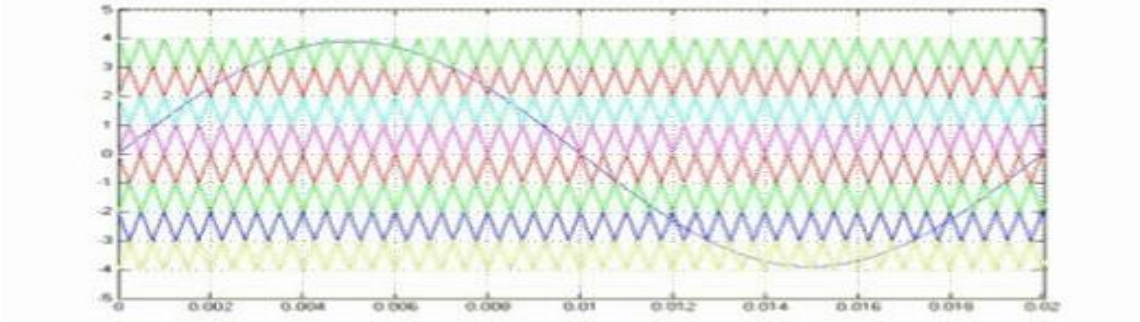


Figure 5: Complete Gate signal for 9-level MC-MLI using Phase Opposition Disposition PWM strategy

. Alternate Phase Opposition Disposition PWM strategy (APODWM)



CHAPTER 4

4.1 SIMULATION

Sr.No	PARAMETERS	NO.OF UNITS	RATINGS
1	Sine wave	1	As per requirement
2	Repeating sequence	4 (for 3 – level) 6 (for 7 –level)	-
3	Relational operator	4 (for 3 – level) 6 (for 7 –level)	-
4	Logical operator (NOT)	4 (for 3 – level) 6 (for 7 –level)	-
5	IGBT	8 (for 5 – level) 12 (for 7 – level)	-
6	DC voltage source	2 (for 5 – level) 3 (for 7- level)	100 V (2) 100 V (3)
7	Single phase Synchronous Machine (capacitor start)	1	-
8	Constant , Bus selector , scope , Mux , voltage measurement.	As per requirement	-

4.2 RESULTS:

A) IN PHASE DISPOSITION METHOD

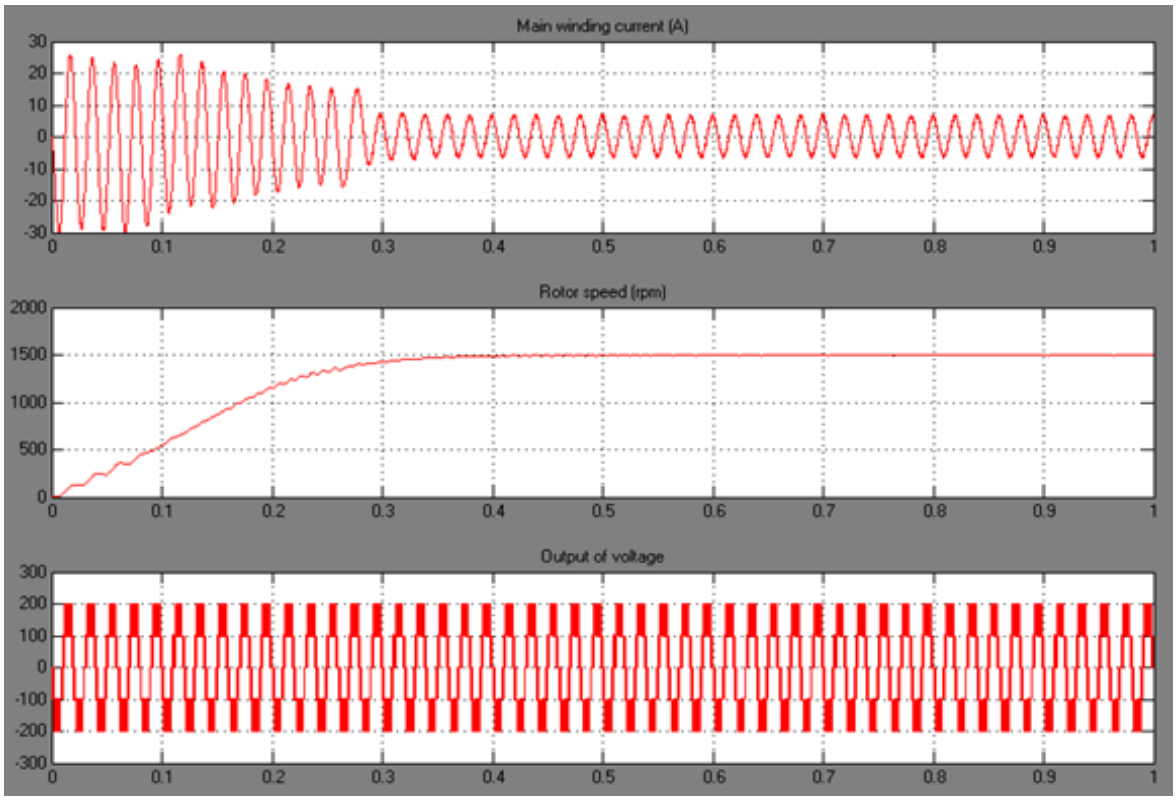


Fig. (a) For Five Level

For five level in phase disposition method the main winding current (THD) is 3.60%. The output of voltage (THD) is 26.95% and the Speed of induction motor (1 phase) is 1500.3 rpm.

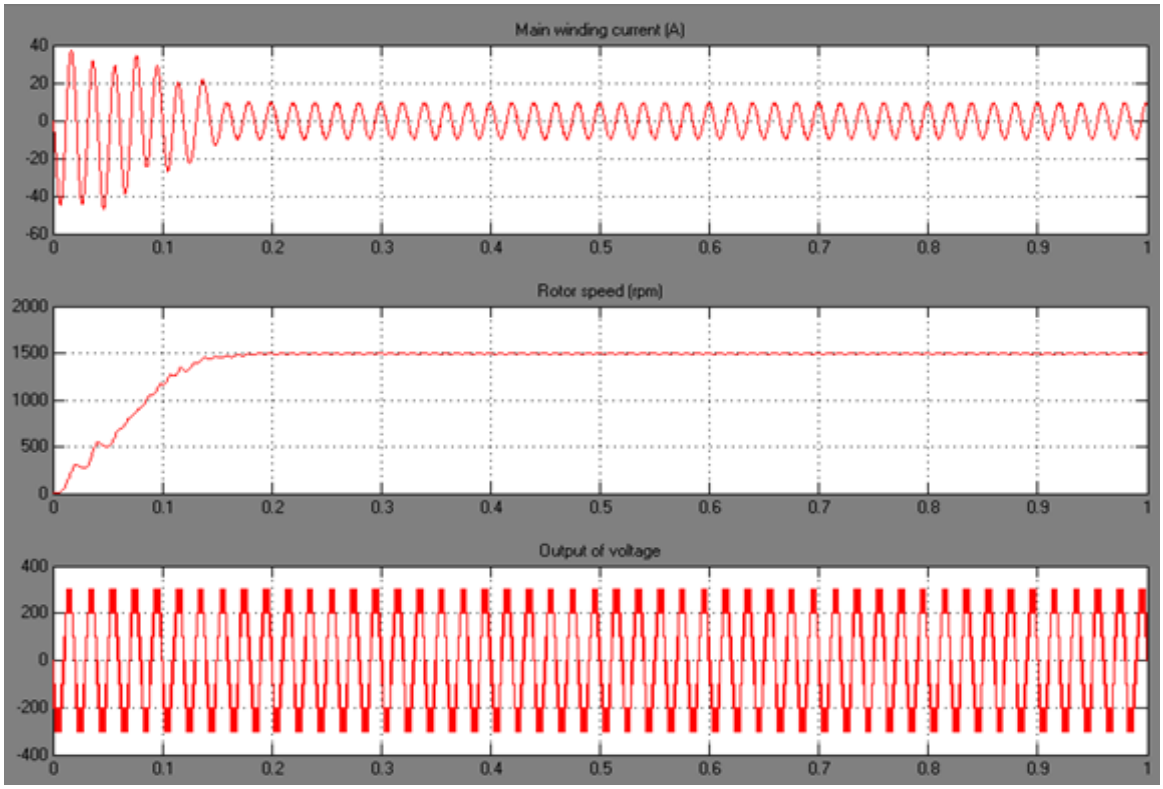


Fig. (b) For Seven Level

For seven level in phase disposition method the Main winding current (THD) is 2.67%, the Output of voltage (THD) is 18.35% and the Speed of induction motor (1 phase) is 1504.8 rpm.

B) PHASE OPPOSITION DISPOSITION

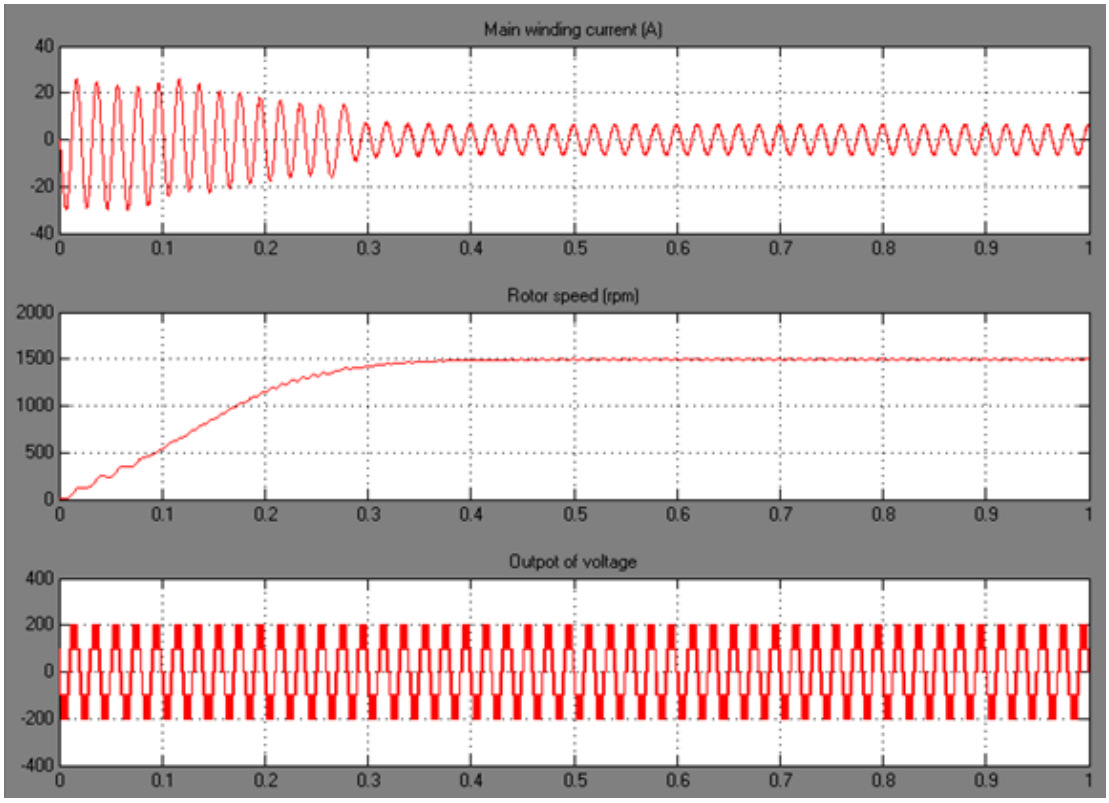


Fig. (a) For Five Level

For five level in phase apposition method Main winding current (THD) is 3.50%, the Output of voltage (THD) is 26.95% and the Speed of induction motor (1 phase) is 1493.9 rpm**.**

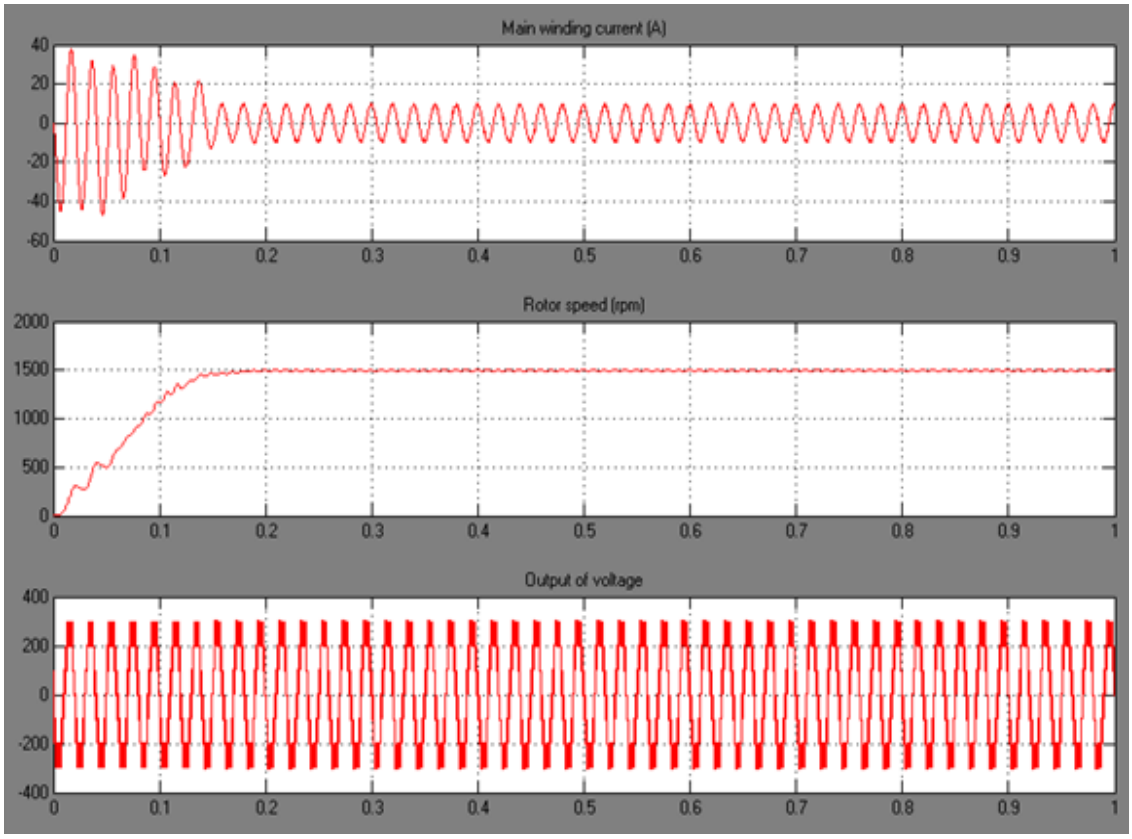


Fig. (b) For Seven Level

For seven level in phase apposition method the Main winding current (THD) is 2.67% , the Output of voltage (THD) is 18.10% and the Speed of induction motor (1 phase) is 1503.5 rpm.

C) ALTERNATE PHASE OPPOSITON DISPOSITION

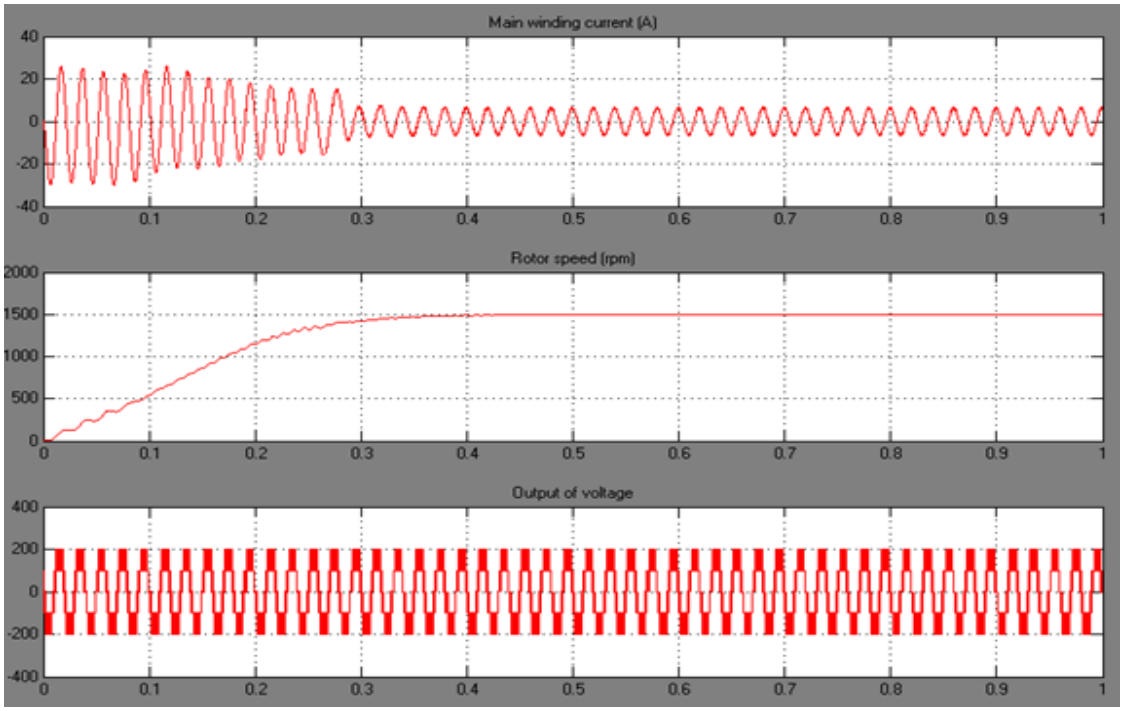


Fig. (a) For Five Level

For five level in alternate phase apposition disposition method the Main winding current (THD) is 3.57%, the Output of voltage (THD) is 27.07% and the Speed of induction motor (1 phase) is 1499.9 rpm.

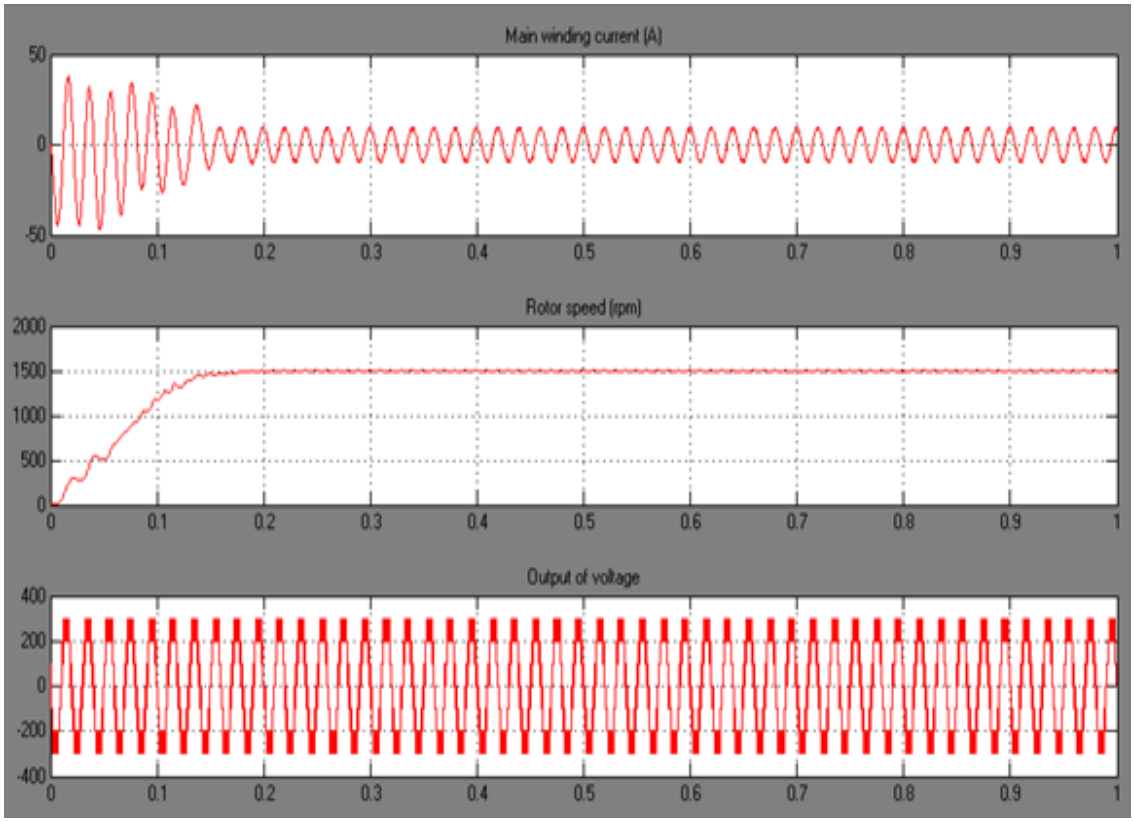
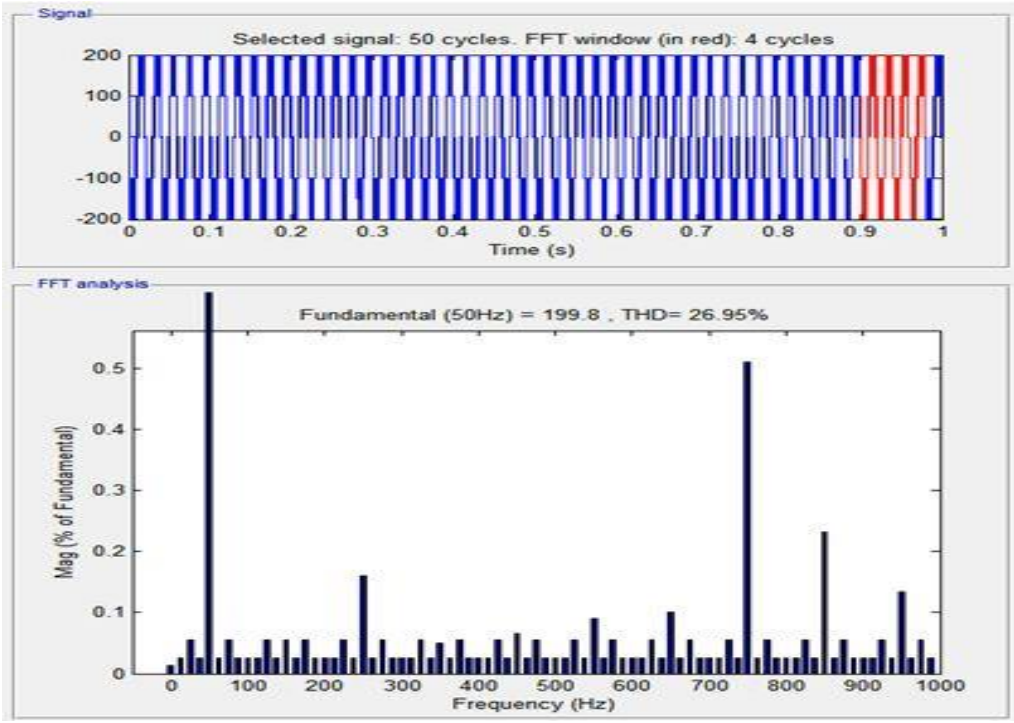


Fig. (b) For Seven Level

For seven level in Alternate phase apposition disposition method then Main winding current (THD) is 2.67%, the Output of voltage (THD) is 17.95% and the Speed of induction motor (1 phase) is 1504.6 rpm.

4.4FFT Analysis



4.3 COPMARISON BETWEEN IPD, POD AND APOD:

PARAMETERS (THD)	IPD		POD		APOD	
	5 LEVEL	7 LEVEL	5 LEVEL	7 LEVEL	5 LEVEL	7 LEVEL
CURRENT (%)	3.60	2.67	3.50	2.67	3.57	2.67
VOLTAGE (%)	26.95	18.35	26.95	18.10	27.07	7.95
SPEED (rpm)	1500.3	1504.8	1493.9	1503.5	1499.9	1504.6

4.5 CONCLUSION

IGBT based cascaded multilevel inverter fed induction motor modeled and simulated using the block of Simulink. It is able to maintain constant speed by maintaining constant voltage the simulation agree with the analytical prediction .The multilevel inverter fed induction motor is successfully simulated in MATLAB. The software system used in present work as obvious advantage using single phase supply. This drive can be used for variable speed applications like electrical vehicles, robotics etc., the proposed techniques was experimented using MATLAB Simulink software and result are verified. And also current, voltage and speed waveform are plotted and also reduces harmonics and produce almost sinusoidal waveform.

The total harmonic distortion is very low compared to that of classical inverter. The simulation result shows that the harmonics have been reduced considerably. The multilevel inverter fed induction motor system has been successfully simulated and the results of voltage waveforms, current waveforms, motor speed for the output were obtained. The inverter system can be used for industries where the adjustable speed drives are required.

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