(81) SE-sem-IV-CBGS-Electrical-ADIC 6/6/16

QP Code :544002

(3 Hours) **[Total Marks: 80]**

N.B.:- (1) Question No. **One** is compulsory.
(2) **Attempt** any **Three** questions out of remaining **five** questions.
(3) Assume suitable data wherever necessary.

Q 1. Answer any **Five** of the following :

a. State important characteristic of IC 741 and compare their value with those of an ideal op-amp. **4**
b. Show how op-amp can be used to give output $V_o = (V_1 + V_2 + V_3)/3$ **4**
c. Draw and explain the output waveforms of a differentiator for step and square input. **4**
d. Convert SR flip-flop to T flip-flop. **4**
e. Define: i> Propagation delay ii> Noise Margin **4**
f. Convert **4**
i> Convert gray to binary (101011)
ii> $(11101101110.1001101)_2$ to hexadecimal equivalent.

Q 2 a) What is instrumentation amplifier? State its advantages. State its applications and explain any one application in details. **10**

Q 2 b) Draw and explain the operation of first order high pass filter. Derive expression for voltage gain and explain its frequency response. **10**

Q 3 a) Draw schematic diagram of IC 555 as astable multivibrator. **10**
An IC 555 is configured to run in astable mode with $R_A = 4\ k\Omega$ $R_B = 4\ k\Omega$ and $C = 0.01\ \mu F$. Determine the frequency of the output and duty cycle. Also draw the waveform for output voltage and voltage across capacitor.

Q 3 b) i> Explain op-amp as zero crossing detector. **10**
ii> Compare Schmitt trigger with comparator.

Q 4 a) List the various methods of A/D conversion. Explain successive approximation type ADC with neat diagram. **10**

Q 4 b) Design a 3 bit synchronous up-counter using T flip-flop. **10**

Q5 Solve

Q 5 a) Prove : $(X + \bar{X}Y)(X + \bar{X}\,Y)(X + Z) = X$ **5**

Q 5 b) Write short note on full adder. **5**

Q5 c) Implement Ex-OR gate using NAND gates. **5**

Q5 d) Implement the following Boolean expression using 8 : 1 multiplexer **5**

$$f(A,B,C,D) = \Sigma\, m\,(2,4,5,7,10,14)$$

Q 6 a) Minimize the function using K map and realize using logic gates. **10**

$$f(A,B,C,D) = \Sigma\, m(1,4,8,12,13,15) + d(3,14)$$

Q 6 b) i>Write a note on parity generators. **10**

Q 6 b) ii>Compare between CMOS and TTL logic families.
