SE-sem-IV-old-EXTC-EDC-2

18/5/16

**QP Code : 28715**



(b) Draw circuit diagram of JFET small signal CS amplifier with self-bias and derive the expression for, small signal mid-band voltage gain, input impedance and output impedance. 10

5. (a) Explain the biasing techniques for D- MOSFET and E-MOSFET. 10

(b) A JFET amplifier with voltage divider biasing circuit shown in figure 2 below has the following parameters: $I_{DSS} = 4mA$, $V_P = -2V$ The circuit parameters: RD = lkΩ, $R_1 = 12M\Omega$ ,$I_{DQ} = 3.4mA$ and $V_{DS} = 10.5V$, $V_{DD} = 24V$. Determine the values of $R_2$ and $R_S$ 10

6. (a) Design L section LC filter with full wave rectifier to meet following specifications: The DC output voltage $V_{DC} = 220V$, deliver $I_L = 70mA \pm 20mA$ to the resistive load, and required ripple factor is 0.04. Also find bleeder resistance if required. 12

(b) Design a simple Zener voltage regulator to meet the following specifications: Output voltage $V_O = 6.8V$, Load current $I_{L\,max} = 60mA, I_{Lmin} = 0mA$, $I_{Zmax} = 100mA, I_Z min = 5mA$, $P_Z = 440m$ W and Input voltage $V_i = 20V$to30V. 8

7. Write a short note on following (**any two**) 20

(a) SCR (Construction and Characteristics).

(b) Bias compensation techniques.

(c) E-MOSFET (Construction and Characteristics).

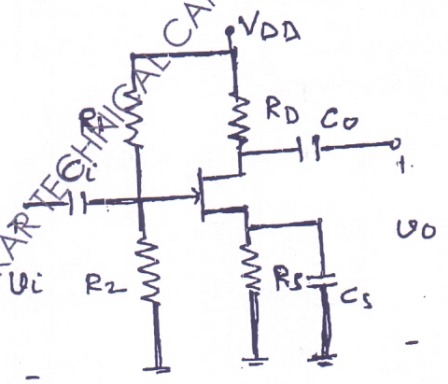


Fig.2

[TURN OVER

**QP Code : 28715**

(3 Hours) [ Total Marks : 100

**N.B. :** (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume suitable **data** whenever **necessary** but **justify** the same.

1. (a) Design single stage RC coupled C E amplifier for the followingspecifications: 15
$A_v \geq 110$, $V_O = 3.5V$, $F_L = 20Hz$ .Use $V_{CC} = 15V$.
(b) For the above designed amplifier determine; voltage gain, input impedance, output impedance. 5

2. (a) Design single stage CS amplifier employing JFET type BFW11 for the following specifications; $A_V \geq 12$, $V_O = 4.2V$ , $I_{DSQ} = 1.2mA$ , $V_{CC} = 21V$ and $F_L = 20Hz$. 15
(b) For the designed amplifier, determine what will be the maximum output voltage that can be obtained without distortion and corresponding input voltage that can be applied in the worst condition. 5

3. (a) Draw small signal hybrid parameter equivalent circuit for CE amplifier and define the same. What are the advantages of h-parameters? 10
(b) Design voltage divider bias circuit for $I_E = 1.2mA$ $V_{CE} = 2.2V$, $R_E = 1k\Omega$ and $\beta = 60$ . $S_{ICO} = 8$. Assume $V_{CC} = 9V$ . 10

4. (a) For the amplifier shown in figure.1 analyze and determine 10
(i) D C bias condition
(ii) Small-signal voltage gain
(iii) Input and output impedance.
The circuit parameters are:
$R_1 = 56k\Omega$ , $R_2 = 12.2k\Omega$ $R_E = 0.4k\Omega$, $R_C = 2k\Omega$,$R_L = 10k\Omega R_S = 0.5k$, $V_{CC} = 10V$
and BJT parameters are $\beta = 100$, $V_{BE} = 0.7V$

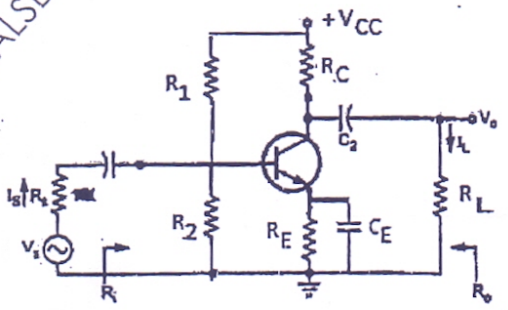

Fig.1

| Transistor type | Pdmax @ 25°C Watts | Icmax @ 25°C Amps | $V_{CE}$ sat volts d.c. | $V_{CEO}$ volts d.c. | $V_{CEO}$ (Sus) volts d.c. | $V_{CES}$ (Sus) volts d.c. | $V_{CEX}$ volts d.c. | $V_{EBO}$ volts d.c. | $T_j$ max °C | D.C. current gain min | typ. | max. | Small Signal min. | typ. | $h_{fe}$ max. | $V_{BE}$ max. | $\theta_{ja}$ °C/W | Derate above 25°C W/°C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N3055 | 115·5 | 15·0 | 1·1 | 100 | 60 | 70 | 90 | 7 | 200 | 20 | 50 | 70 | 15 | 50 | 120 | 1·8 | 1·5 | 0·7 |
| ECN055 | 50·0 | 5·0 | 1·0 | 60 | 50 | 55 | 60 | 5 | 200 | 25 | 50 | 100 | 25 | 75 | 125 | 1·5 | 3·5 | 0·4 |
| ECN149 | 30·0 | 4·0 | 1·0 | 50 | 40 | — | — | 8 | 150 | 30 | 50 | 110 | 33 | 60 | 115 | 1·2 | 4·0 | 0·3 |
| ECN100 | 5·0 | 0·7 | 0·6 | 70 | 60 | 65 | — | 6 | 200 | 50 | 90 | 280 | 50 | 90 | 280 | 0·9 | 35 | — |
| BC147A | 0·25 | 0·1 | 0·25 | 50 | 45 | 50 | — | 6 | 125 | 115 | 180 | 220 | 125 | 220 | 260 | 0·9 | — | — |
| 2N525(PNP) | 0·225 | 0·5 | 0·25 | 85 | 30 | — | — | — | 100 | 35 | — | 65 | — | 45 | — | — | — | — |
| BC147B | 0·25 | 0·1 | 0·25 | 50 | 45 | 50 | — | 6 | 125 | 200 | 290 | 450 | 240 | 330 | 500 | 0·9 | — | — |

| Transistor type | hie | hoe | hre | oja |
|---|---|---|---|---|
| BC 147A | 2·7 K Ω | 18μ ℧ | 1·5 × 10⁻⁴ | 0·4°C/mw |
| 2N 525 (PNP) | 1·4 K Ω | 25μ ℧ | 3·2 × 10⁻⁴ | — |
| BC 147B | 4·5 K Ω | 30μ ℧ | 2 × 10⁻⁴ | 0·4°C/mw |

BFW 11—JFET MUTUAL CHARACTERISTICS

| −Vgs volts | 0·0 | 0·2 | 0·4 | 0·6 | 0·8 | 1·0 | 1·2 | 1·6 | 2·0 | 2·4 | 2·5 | 3·0 | 3·5 | 4·0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Ios max. mA | 10 | 9·0 | 8·3 | 7·6 | 6·8 | 6·1 | 5·4 | 4·2 | 3·1 | 2·2 | 2·0 | 1·1 | 0·5 | 0·0 |
| Ios typ. mA | 7·0 | 6·0 | 5·4 | 4·6 | 4·0 | 3·3 | 2·7 | 1·7 | 0·8 | 0·2 | 0·0 | 0·0 | 0·0 | 0·0 |
| Ios min. mA | 4·0 | 3·0 | 2·2 | 1·6 | 1·0 | 0·5 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 | 0·0 |

N-Channel JFET

| Type | $V_{DS}$ max. Volts | $V_{DG}$ max. Volts | $V_{GS}$ max. Volts | $P_d$ max. @25°C | $T_j$ max. | $I_{DSS}$ | $g_{fs}$ | $-V_p$ Volts | $r_d$ | Derate above 25°C | $\theta_{ja}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N3822 | 50 | 50 | 50 | 300 mW | 175°C | 2 mA | 3000 μΩ | 6 | 50 KΩ | 2 mW/°C | 0·59°C/mW |
| BFW 11 (typical) | 30 | 30 | 30 | 300 mW | 200°C | 7 mA | 5000 μΩ | 2·5 | 50 KΩ | — | 0·59° C/mW |

| UJT type | $P_d$ max. @25°C | $I_E$ max. @25°C | $I_P$ peak pulse current max. | $V_{EB2}$ Volts max. | $V_{EB1}$ Volts | $T_j$ max | η min. | η max. | $R_{BB}$ KΩ min. | $R_{BB}$ KΩ typ. | $I_P$ μA max. | $I_V$ mA min. | $I_{EO}$ μA max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2N2646 | 300mW | 50mA | 2Amp. | 30 | 35 | 125°C | 0·56 | 0·75 | 4·7 | 7·0 | 9·1 | 5·0 | 4·0 | −2·0 |