## 7E-sem-VI-01d-computers-Adv. Micro. 16/5/16

Q.P. Code: 580701

(3 Hours)

[ Total Marks: 100

Note:	1) Question no. 1 is compulsory	
	2) Answer any four from Q.2 to Q.7	
	3) Draw diagram wherever necessary.	
Q.1	a) Explain architecture of Pentium processor with neat diagram.	10
	b) Explain address translation mechanism of 80386.	10
Q.2	a) Draw and explain code cache organisation of Pentium processor.	10
	b) Explain protection mechanism used in 80386DX processor.	10
Q.3	a) How flushing problem is minimised in Pentium processor?	10
	b) Explain PCI workstation.	10
Q.4	a) Draw the block diagram of super SPARC processor and explain.	10
	b) Explain pipeline hazards with examples.	10
Q.5	a) Explain layered architecture of SCS!.	10
	b) Discuss data formats of SPARC processor.	10
Q.6	a) Draw block diagram of Itanium processor and write its features.	10
	b) Draw and explain segment descriptor.	10
Q. 7	Write note on (Any four)	20
	a) Floating point pipeline stages of Pentium processor.	
	b) Principles of designing of pipelined processor.	
	c) USB	
	d) RISC and CISC	
	e) Flag register of 80386.	