# FLASH ADC

Submitted in partial fulfillment of the requirements
of the degree of

**Bachelor of Engineering**

in

**Electronics and Telecommunication**

by

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University of Mumbai

2018-19

# CERTIFICATE


Department of Electronics and Telecommunication Engineering
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University of Mumbai

This is to certify that the project entitled **Flash ADC** is a bonafide work of **Tanzeem Matin Shaikh (15DET), Asad Syed Ahmed Qadri (15DET115), Usama Zulfikar Arai (15DET86), Danish Chandwale (14DET)** submitted to the University of Mumbai in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering in Department of Electronics and Telecommunication Engineering.

| | |
|---|---|
| Supervisor | Examiner |
| Head of Department | Director |

# Project Report Approval for Bachelor of Engineering

This project entitled **"Flash ADC"** by **Tanzeem Matin Shaikh (15DET80), Asad Syed Ahmed Qadri (15DET115), Usama Zulfikar Arai (15DET86), Danish Chandwale (14DET74)** is approved for the degree of **Bachelor of Engineering in Electronics and Telecommunication**.

Examiner

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Supervisor

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# Declaration

I declare that this written submission represents my ideas in my own words and where others ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

…….
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.

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## Abstract:

The main concept behind this project is to convert analog data into digital data. Analog to Digital converter (ADC) finds the major role in Analog Circuit Design. Analog signal is characterized by the signal whose amplitude is continuously changing with respect to time while the amplitude and time is discrete in case of digital signal. A flash ADC (also known as a direct-conversion ADC) is a type of analog-to-digital converter that uses a linear voltage ladder with a comparator at each "rung" of the ladder to compare the input voltage to successive reference voltages. Often these reference ladders are constructed of many resistors however, modern implementations show that capacitive voltage division is also possible. The output of these comparators is generally fed into a digital encoder, which converts the inputs into a binary value. Flash converters are extremely fast compared to many other types of ADCs, which usually narrow in on the "correct" answer over a series of stages. Compared to these, a flash converter is also quite simple and, apart from the analog comparators, only requires logic for the final conversion to binary. For best accuracy, often a track-and-hold circuit is inserted in front of the ADC input. This is needed for many ADC types (like successive approximation ADC) but for flash ADCs there is no real need for this because the comparators are the sampling devices. A flash converter requires a huge number of comparators compared to other ADCs, especially as the precision increases. A flash converter requires comparators for an *n*-bit conversion. The size, power consumption and cost of all those comparators makes flash converters generally impractical for precisions much greater than 8 bits (255 comparators). In place of these comparators, most other ADCs substitute more complex logic and/or analog circuitry that can be scaled more easily for increased precision.

# CHAPTER 1

# INTRODUCTION

## 1.1 Aim Of The Project:

The purpose of our project is to meet the requirement of the present industrial and commercial scenario. The prime objective was to implement the project with the use of latest available technologies and component which can perform well even with increased accuracy. It provides high accuracy, speed, reliability, and ruggedness.

In this project we plan to implement a project based on Cadence "Flash ADC" which will improve the scenario of analog to digital conversion. This system gives you access of the status of conversion.

## 1.2 Salient Feature:

- Flash ADC also known as Parallel ADC
- It is the fastest way to convert an analog signal to digital signal
- It has very large Bandwidth
- Generally it is limited for 8 bit resolution

## 1.3 Introduction To Flash ADC:

Analog to digital convertor circuit is generally used for converting analog signal into respective digital signal. Analog signal is continuously vary with time and amplitude. So for conversion we have to convert continuously changing time into discrete time. For conversion there are different ways like sample and hold circuit. The ADC is characterized by three-factors namely speed, area, and power consumption, the cost of ADC is varying from application to application. Resistive ladder network is used for generating the internal reference voltage for comparator.

# CHAPTER 2

# DEVELOPMENT STAGES AND PROCESS

**The complete development of this system can be divided into following stages:**

- Problem definition stage.
- Research Paper.
- Designing a block diagram.
- Implementing circuits and components.
- Developing structural algorithm for Cadence software.
- Testing and running.

## 2.1 Problem definition stage:

This is very first stage to develop any project. It actually defines the aim and concept of the project. The aim of our project "Flash ADC" is that the output bits of ADC is very high and the power consumption is very low.

## 2.2 Research Paper:

At this stage we had to search for research papers which would be relevant for guidance our project.

## 2.3 Designing a block diagram:

At this stage we have categorized the whole system into different individual modules. These modules (block diagram) will be helpful in understanding the concept and working of the integrated system. It also simplifies the entire debugging and testing process.

## 2.4 Implementing circuits and components:

This is actual implementing of circuit of each block. At this stage we have actually designed each block separately and finally integrate them into complete working system.

**2.5 Developing structural algorithm for Cadence software:**

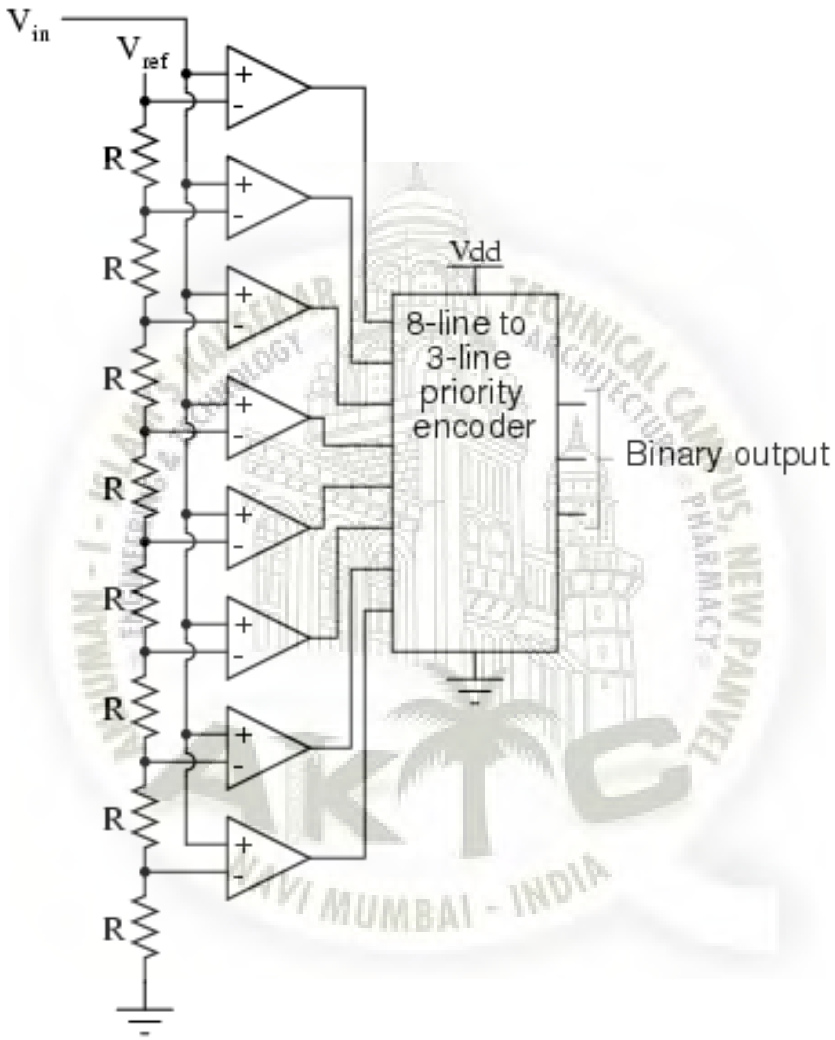
To get the logical flow of the software the development of structural algorithm is having a prominent role. So we have analyzed the complete system and organized the algorithm in such a manner that one can understand the complete working of the software.

**2.6 Testing and running:**

This time we tested our project for actual working. Any errors found were removed successfully. This is the last and final stage of development of our project.

CHAPTER 3

# DESIGNING A BLOCK DIAGRAM




Flash ADCs are made by cascading high-speed comparators. Figure above shows a typical flash ADC block diagram. For an N-bit converter, the circuit employs $2^N$-1 comparators. A resistive-divider with $2^N$ resistors provides the reference voltage. The reference voltage for each comparator is one least significant bit (LSB) greater than the reference voltage for the comparator immediately below it. Each comparator produces a 1 when its analog input voltage is higher than the reference voltage applied to it. Otherwise, the comparator output is 0.

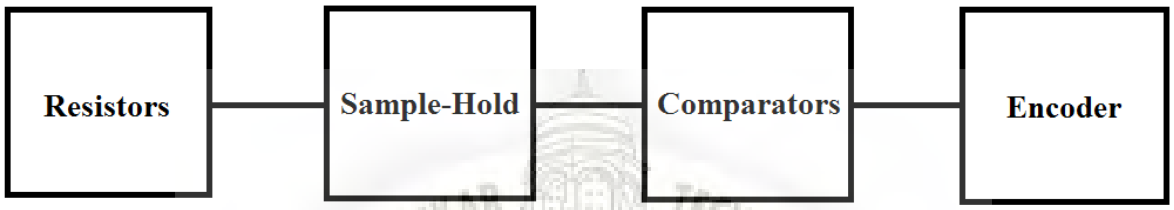
Thus, if the analog input is between $V_{X4}$ and $V_{X5}$, comparators $X_1$ through $X_4$ produce 1s and the remaining comparators produce 0s. The point where the code changes from ones to zeros is the point at which the input signal becomes smaller than the respective comparator reference-voltage levels.

This architecture is known as thermometer code encoding. This name is used because the design is similar to a mercury thermometer, in which the mercury column always rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is then decoded to the appropriate digital output code.

The comparators are typically a cascade of wideband low-gain stages. They are low gain because at high frequencies it is difficult to obtain both wide bandwidth and high gain. The comparators are designed for low-voltage offset, so that the input offset of each comparator is smaller than an LSB of the ADC. Otherwise, the comparator's offset could falsely trip the comparator, resulting in a digital output code that is not representative of a thermometer code. A regenerative latch at each comparator output stores the result. The latch has positive feedback, so that the end state is forced to either a 1 or a 0.Given these basics, some adjustments are needed to optimize the flash converter architecture.

# CHAPTER 4

## SOFTWARE IMPLENTATION




Software Implementation is done in four major steps:

1. Resistors Network.
2. Sample-Hold Network.
3. Comparator.
4. Encoder.

# CHAPTER 5

## LITERATURE REVIEW

| Author Name | Paper Title | Work Done |
|---|---|---|
| Jagpal Singh Ubbi, Akash Tomar, and Mukesh Kumar | Low Power 3-Bit Flash ADC Design with Leakage power reduction at 45 nm Technology | 3-bits 41.12 µW |
| Nayana Kalyani, Monica M | Design and Analysis of High Speed and low power 6-bit Flash ADC | 6-bits 8.8mW |
| Mehdi Nasrollahpour, Sotoudeh Hamedi | Extra Bit Generation for High-speed Time Based Flash ADCs in 65nm CMOS | 5-bits 7.7mM |
| Siddhart R K, Nithin Kumar Y B, Vasantha M H | A Low-Power Auxiliary Circuit for Level-Crossing ADCs on IOT-Sensor Applications | 5-bits 0.489 mW |
| LIU Haitao, WU junjie, Zhang Lizheng, Deng Qing | A 14b 250MSps pipelined ADC with Digital Self-calibration in 0.18µm CMOS process | 14-bits 398 mW |

# CHAPTER 6

# FLASH ADC

Analog to digital convertor circuit is generally used for converting analog signal into respective digital signal. Analog signal is continuously vary with time and amplitude. So for conversion we have to convert continuously changing time into discrete time. For conversion there are different ways like sample and hold circuit. The ADC is characterized by three-factors namely speed, area, and power consumption, the cost of ADC is varying from application to application. Resistive ladder network is used for generating the internal reference voltage for comparator. Threshold inverter quantizer (TIQ) is a part of Clocked Digital Comparator (CDC) eliminates resistive ladder network. CDC uses inverter for generation of internal reference voltage.

Flash Analog to Digital Convertor (FADC) consists of two stages. In first stage Clocked Digital Comparator (CDC) have back-to-back inverter configuration followed by transmission gate. In ADC Transmission gate is used as sampler. Second stage of ADC consists of multiplexer based decoder. In multiplexer based decoder, middle bit is used as select line of 2:1 MUX because it consists of two stages (0 and 1) rest of the bits follows the thermometer code hence the MSB of output binary code is exactly same as the middle bit. The second MSB and LSB's of output binary bits are obtained depending on the value of middle bit, if the value of middle bit is 0 then multiplexer based decoder circuit select the upper bits (Right side bits of middle bit) and if value of middle bit is 1 then it selects lower bits (Left side bits of middle bit).

## 6.1: Clocked Digital Comparator:

Quantizer, sampler and encoder are required for designing ADC. In clocked digital comparator as shown in figure 1, the first stage consist of two inverter, the first inverter is acting as the quantizer by settling the comparator voltages for comparison and the second inverter is acting as the logic level inversion. The need of second inverter arises due to the output of first inverter.

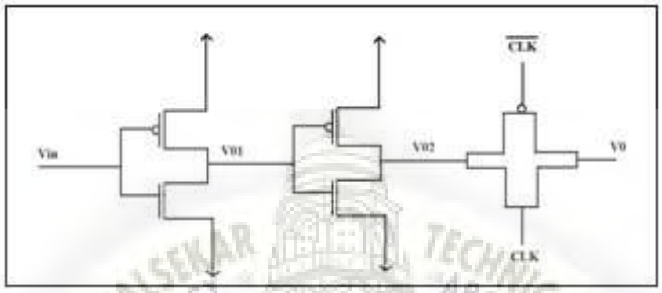



**Figure 1: Clocked Digital Comparator**

### 6.1.1: Threshold Inverter Quantizer:

In the first stage of Clocked Digital Comparator consist of Threshold Inverter Quantizer (TIQ) shown in figure 2, TIQ is used for generation of internal reference voltages required for comparison. There are different methods for comparison like resistive ladder network.

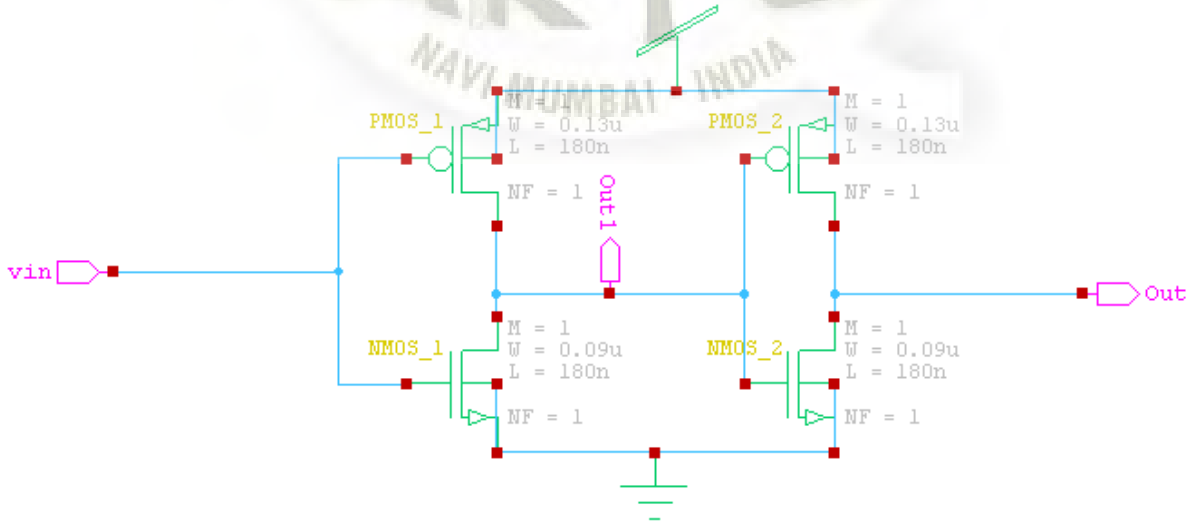



**Figure 2: Threshold Inverter Quantizer (TIQ)**

In TIQ by systematic varying the width of NMOS and PMOS transistors internal reference voltage can be generate. The length of transistor is depending upon technology.

### 6.1.2: CMOS Inverter As Phase Shifter:

The inverter provides phase shift, amplification, quantization stages. Let us consider the signal given to the clocked digital comparator is sine wave then inverter gives the output negative of sine wave.

### 6.1.3: Transmission Gate:

Transmission gate is in the second stage of CDC use for sampling the signal, as we know the transmission gate is depend upon the clock signal there are two different types of transmission gate Positive edge enabled clocked and Negative edge enabled clocked. The frequency on which clocked operates called as sampling frequency and the sampling frequency should be more than twice of input frequency, so the clocked digital comparator is acting as the quantizer and sampler.

## 6.2: Op-Amp:

The trend towards low voltage low power silicon chip systems has been growing due to the increasing demand of smaller size and longer battery life for portable applications in all marketing segments including telecommunications, medical, computers and consumer electronics. The operational amplifier is undoubtedly one of the most useful devices in analog electronic circuitry. Op-amps are built with different levels of complexity to be used to realize functions ranging from a simple dc bias generation to high speed amplifications or filtering. With only a handful of external components, it can perform a wide variety of analog signal processing tasks. Op-amps are among the most widely used electronic devices today, being used in a vast array of consumer, industrial, and scientific devices. Operational Amplifiers, more commonly known as Op-amps, are among the most widely used building blocks in Analog Electronic Circuits.

Op-amps are linear devices which has nearly all the properties required for not only ideal DC amplification but is used extensively for signal conditioning, filtering and for performing mathematical operations such as addition, subtraction, integration, differentiation etc . Generally an Operational Amplifier is a 3-terminal device.

It consists mainly of an Inverting input denoted by a negative sign, ("-") and the other a Non-inverting input denoted by a positive sign ("+") in the symbol for op-amp. Both these inputs are very high impedance. The output signal of an Operational Amplifier is the magnified difference between the two input signals or in other words the amplified differential input. Generally the input stage of an Operational Amplifier is often a differential amplifier.

An operational amplifier is a DC-coupled differential input voltage amplifier with an rather high gain. In most general purpose op-amps there is a single ended output. Usually an op-amp produces an output voltage a million times larger than the voltage difference across its two input terminals. For most general applications of an op-amp a negative feedback is used to control the large voltage gain. The negative feedback also largely determines the magnitude of its output ("closed- loop") voltage gain in numerous amplifier applications, or the transfer function required. The op-amp acts as a comparator when used without negative feedback, and even in certain applications with positive feedback for regeneration. An ideal Opamp is characterized by a very high input impedance (ideally infinite) and low output impedance at the output terminal(s) (ideally zero).to put it simply the op- amp is one type of differential amplifier. This section briefly discusses the basic concept of op-amp. An amplifier with the general characteristics of very high voltage gain, very high input resistance, and very low output resistance generally is referred to as an op-amp. Most analog applications use an Op-Amp that has some amount of negative feedback. The Negative feedback is used to tell the Op-Amp how much to amplify a signal. And since op-amps are so extensively used to implement a feedback system, the required precision of the closed loop circuit determines the open loop gain of the system.

A basic op-amp consists of 4 main blocks:
a. Current Mirror

b. Differential Amplifier
c. Level shift, differential to single ended gain stage
d. Output buffer

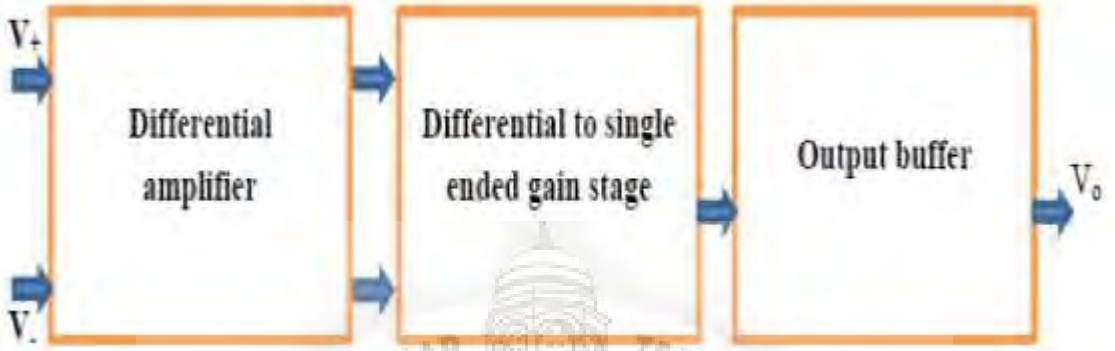



**Fig.1 General Structure of op-amp**

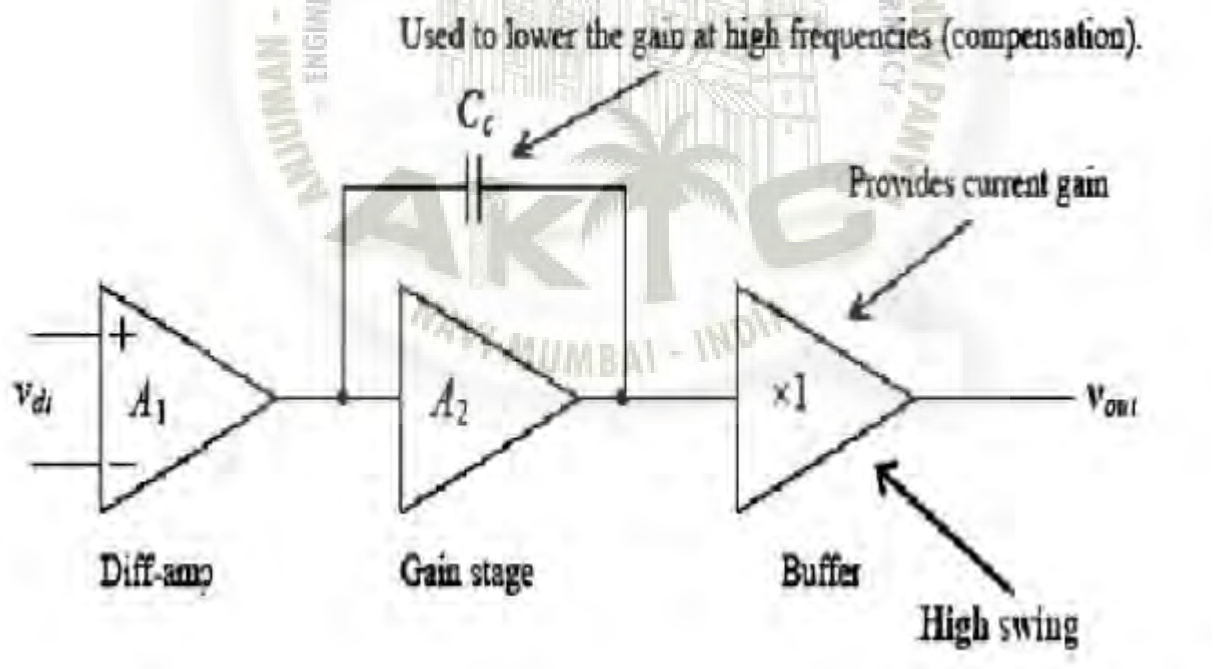



**Fig. 2 Functional Block Diagram of two stage opamp**

In above figures, The first block is input differential amplifier, which is designed so that it provides very high input impedance, a large CMRR and PSRR, a low offset voltage, low noise and high gain. The second stage performs Level shifting, added gain and differential to single

ended converter. The third block is the output buffer. The output buffer may sometimes be omitted to form a high output resistance un-buffered op-amp often referred to as Operational

trans conductance amplifier or an OTA. Those which have the final output buffer stage have a low output resistance (Voltage operational amplifiers).

CMOS Operational Amplifier is one of the most versatile and important building blocks in analog circuit design. Based upon the value of their output resistance they are being classified into two categories:

### 6.2.1. Unbuffered Operational Amplifier:

These are Operational Transconductance Amplifiers (OTA), which have high output resistance.

### 6.2.2. Buffered Operational Amplifier:

These are Voltage Operational Amplifiers, which have low output resistance. Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer – function is practically independent of the gain of the opamp. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement negative feedback concept.

CMOS op-amps are very similar in architecture to their bipolar counterparts.

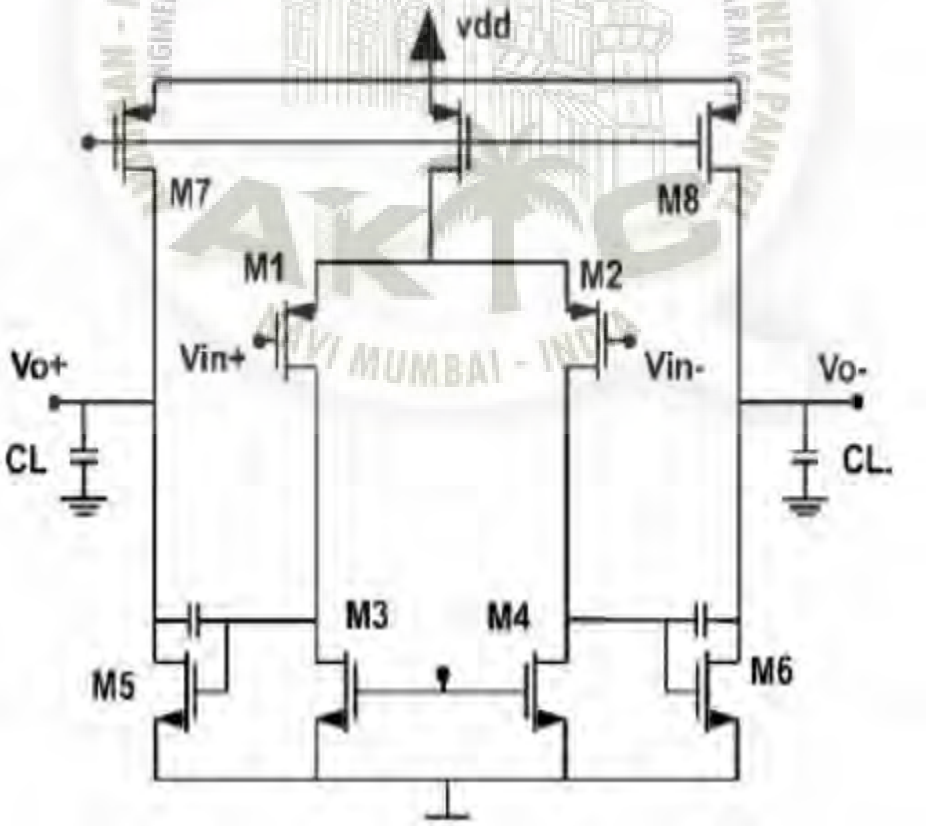



**Fig. 3 A Typical Two Stage Amplifier**

The Two Stage op-amp shown in fig 3 is widely used because of its structure and robustness.
Our aim is to create the physical design and fabricate a low power Op-amp. An ideal op-amp having a single- ended out is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down.

### 6.2.3 Designing Of Two Stage CMOS Op-Amp:

The designed op-amp has been simulated to find the different characteristics of the designed op-amp. The total design performed in Cadence tool. Different test benches have been created and extracted design has been then simulated with the parasitic values and compared with the schematic. Later in the chapter we also have compared the obtained parameters of the device through simulation to the specifications for the device.

Design Issues

| **Typical specs** | **Design factors** |
|---|---|
| ! DC Gain (Av) | Frequency Response |
| ! Unity Gain Bandwidth | Phase Margin |
| ! Power Dissipation | Load Capacitance |
| ! Slew Rate | Compensation |
| ! Input Offset Voltage | Device Dimensions |
| ! PSRR | |
| ! Output Voltage Swing | |
| ! ICMR | |
| ! CMRR | |

### 6.2.4 Steps In Designing CMOS Op-Amp:

Choosing or creating the basic structure of the op amp.
Decide on a suitable configuration determination of the type of compensation needed for meeting the specification
Selection of the dc currents and transistor sizes.
Physical implementation of the design.
Fabrication
Measurement

The design process involves the two major steps, the first is the conception of design ,and second one is optimization of design . The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the intuitive view point necessary for choices that must be made. Second step is to take the “first-cut” design and verify and optimize it. This is normally done by using Computer simulation and can include such influences as environmental or process variations.
Design procedure assumes that the gain at dc (Av), unity gain bandwidth (GB), input common mode range (Vin(min) and Vin(max)), load capacitance (CL), slew rate (SR), settling time (Ts), output voltage swing (Vout(max) and Vout(min)), and power dissipation (Pdiss) are given. Choose the smallest device length which will keep the channel modulation parameter constant and give good matching for current mirrors.

1. From the desired phase margin, have to choose the minimum value for *Cc*, i.e. for a 60° phase margin we use the following relationship. This assumes that

z>=10GB.
Cc>=0.22CL

2. Determine the minimum value for the "tail current" ( ) from

I5 =SR .Cc

Now , Tail Current (Iss/I5) can also be found by

$$2\Pi f_{T=} \quad {}^{2I_{SS}}/_{(V_{GS}-V_{TH})} \quad {}^{1}/_{C_L}$$

where Iss is the Tail Current.

3. Design for S5 from the minimum input voltage. First calculate *VDS*5 (sat) then find S5.

$$V_{DS5(SAT)} = V_{IN(MIN)} - V_{SS} - \sqrt{{}^{I_5}/_{\beta 1}} - V_{T1\,(MAX)} \geq 100\text{mv}$$

$$S5 = \frac{2I_5}{K'_5[V_{DS5\,(SAT)}]2}$$

4. Have to find S6 by letting the second pole (*p*2) be equal to 2.2 times GB and assuming that

VSG4 = VSG6.

### 6.3. Multiplexer Based Decoder:

The multiplexer based decoder Implementation is shown in figure 3. It consists of 2:1 multiplexer, which requires 11 multiplexer for implementation of 15 inputs. The 2:1 multiplexer requires two input signals with one select line, depending on the select line input will selected, the M.S.B. bit of binary input equal to middle bit of thermometer code because it uses the twin logic.

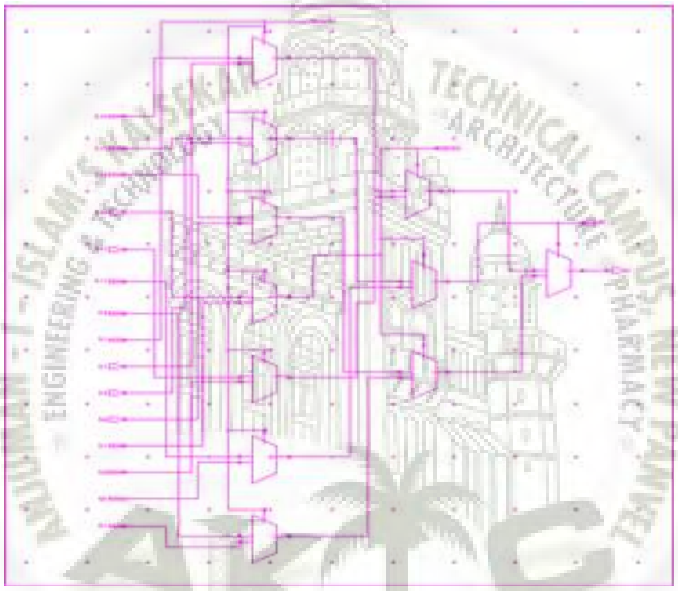


**Figure 3: Tanner Implementation of MUX Based Decoder**

**6.4: Binary Encoding:**

The binary output of the ADC can be encoded in several ways. If the signal being converted is unipolar, then it is usually encoded as a unipolar straight binary code. This code represents a zero value as all zeros (0000…) and the maximum input value as all ones (1111…).

If the signal is bipolar, then it is generally represented as either offset binary or two's complement binary as detailed using a 4-bit example.

| Input Value | Bipolar Offset Binary | Two's Complement Binary |
|---|---|---|
| - Full scale | 0000 | 1000 |
| Bipolar zero - 1 LSB | 0111 | 1111 |
| Bipolar zero | 1000 | 0000 |
| Bipolar zero + 1 LSB | 1001 | 0001 |
| + Full scale | 1111 | 0111 |

**Common binary encoding for bipolar digital signals. Two's complement binary is most widely used by microprocessor or math processors. (Image source: Digi-Key Electronics)**

Two's complement binary coding is the type of coding used by most microprocessor or math processor based systems as it facilitates arithmetic operations.

**6.5: Design Of ADC-CDC:**

The comparators require two input signal for comparison, One signal is generated from internal reference voltage and other signal is input signal (for example. Sine wave). The Comparator generates the Thermometer code and depending upon Table-I respective digital code is generated. The threshold voltages are laying in the range from 0.653 to 1.02 volt for this range ADC produces the respective binary bits. Below this range, the output equals to zero and above this range, the output equals to one. During positive interval of clock, it produces output; otherwise zero. The above logic is valid only when the amplitude of input signal starts from zero and reaches toward the maximum value as the amplitude falls from the maximum value toward zero value the effect of mobility arises. As we know, the mobility of electron is equal to the three times the mobility of hole, the output is not same as the input.

| Sr. No. | Internal Reference Voltage | W(p) | W(n) |
|---|---|---|---|
| 1 | 0.653 | 2.6u | 16u |
| 2 | 0.681 | 1.98u | 17u |
| 3 | 0.698 | 1.78u | 21u |
| 4 | 0.724 | 1.58u | .23u |
| 5 | 0.744 | 1.38u | .25u |
| 6 | 0.778 | 1.23u | .27u |
| 7 | 0.813 | 1.1u | .29u |
| 8 | 0.859 | .95u | .31u |
| 9 | 0.88 | .88u | .51u |
| 10 | 0.9 | .82u | .71u |
| 11 | 0.921 | .74u | .96u |

| | | | |
|---|---|---|---|
| 12 | 0.942 | .68u | 1.12u |
| 13 | 0.967 | .6u | 1.37u |
| 14 | 0.99 | .5u | 1.52u |
| 15 | 1.02 | .42u | 1.78u |

**TABLE I: Generation of Internal reference voltage.**

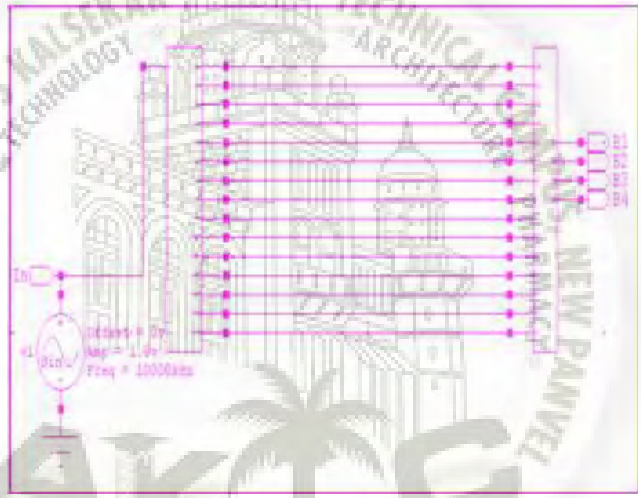


**Figure 6: Tanner Implementation of Analog to Digital Convertor.**

**6.6 Architectural Trade-Offs:**

ADCs can be implemented by employing a variety of architectures. The principal trade-offs among these alternatives are:

The time it takes to complete a conversion (conversion time). For flash converters, the conversion time does not change materially with increased resolution. The conversion time for successive approximation register (SAR) or pipelined converters, however, increases approximately linearly with an increase in resolution (Figure 3a). For integrating ADCs, the conversion time doubles with every bit increase in resolution.

Component matching requirements in the circuit. Flash ADC component matching typically limits resolution to around 8 bits. Calibration and trimming are sometimes used to improve the matching available on chip. Component matching requirements double with every bit increase in resolution. This pattern applies to flash, successive approximation, or pipelined converters, but not to integrating converters. For integrating converters, component matching does not materially increase with an increase in resolution (Figure 3b).

Die size, cost, and power. For flash converters, every bit increase in resolution almost doubles the size of the ADC core circuitry. The power also doubles. In contrast, a SAR, pipelined, or sigma-delta ADC die size will increase linearly with an increase in resolution; an integrating converter core die size will not materially change with an increase in resolution (Figure 3c). Finally, it is well known that an increase in die size increases cost.

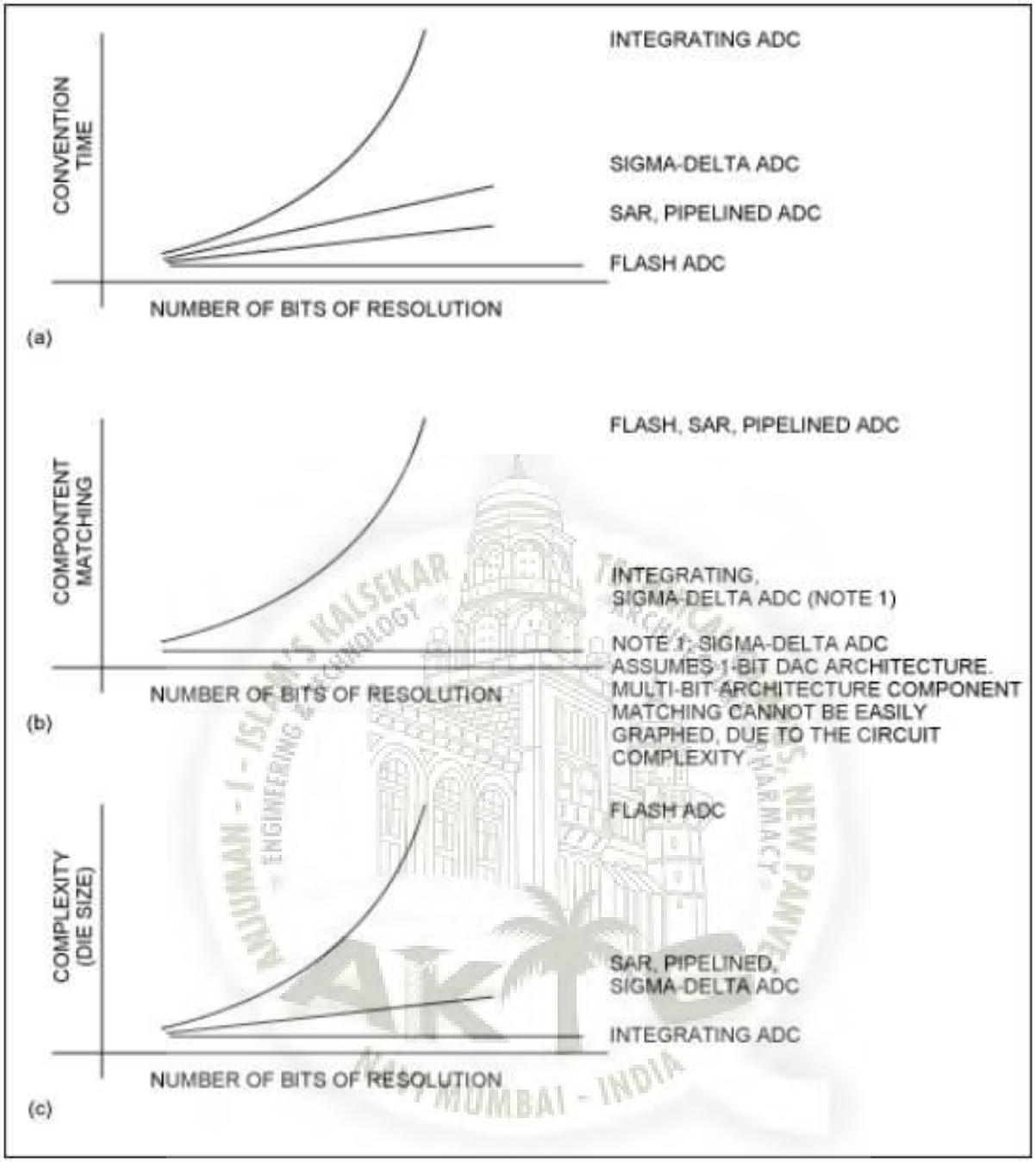



**Figure 3. Architectural Trade-Offs.**

# CHAPTER 7
# FLASH ADC VS OTHER ADC ARCHITECTURES

## 7.1. Flash Vs SAR ADCs:

In a SAR converter, a single high-speed, high-accuracy comparator determines the bits, one bit at a time (from the MSB down to the LSB). This is done by comparing the analog input with a DAC whose output is updated by previously decided bits and thus successively approximates the analog input. This serial nature of the SAR limits its speed to no more than a few mega-samples per second (Msps), while flash ADCs exceed giga-samples per second (Gsps) conversion rates.

SAR converters are available in resolutions up to 16 bits. An example of such a device is the MAX1132. Flash ADCs are typically limited to around 8 bits. The slower speed also allows the SAR ADC to be much lower in power. For example, the MAX1106, an 8-bit SAR converter, uses 100μA at 3.3V with a conversion rate of 25ksps. The MAX104 dissipates 5.25W, about 16,000 times higher power consumption than the MAX1106 and 40,000 times faster in terms of its maximum sampling rate.

The SAR architecture is also less expensive. The MAX1106 at 1k volumes sells at something over a dollar (U.S.), while the MAX104 sells at several hundred dollars (U.S.). Package sizes are larger for flash converters. In addition to a larger die size requiring a larger package, the package needs to dissipate considerable power and needs many pins for power and ground signal integrity. The package size of the MAX104 is more than 50 times larger than the MAX1106.

## 7.2. Flash Vs. Pipelined ADCs:

A pipelined ADC employs a parallel structure in which each stage works on one to a few bits of successive samples concurrently. This design improves speed at the expense of power and latency, but each pipelined stage is much slower than a flash section. The pipelined ADC requires accurate amplification in the DACs and interstage amplifiers, and these stages have to settle to the desired linearity level. By contrast, in a flash ADC the comparator only needs to be low offset and to resolve its inputs to a digital level; there is no linear settling time involved. Some flash converters require pre-amplifers to drive the comparators. Gain linearity needs to be specified carefully.

Pipelined converters convert at speeds of around 100Msps at 8- to 14-bit resolutions. An example of a pipelined converter is the MAX1449, 105MHz, 10-bit ADC. For a given resolution, pipelined ADCs are around 10 times slower than flash converters of similar resolution.

Pipelined converters are possibly the optimal architecture for ADCs that need to sample at rates up to around 100Msps with resolution at 10 bits and above. For resolutions up to 10 bits and conversion rates above a few hundred Msps, flash ADCs dominate.

Interestingly, there are some situations where flash ADCs are hidden inside a converter employing another architecture to increase its speed.

### 7.3. Flash Vs Integrating ADCs:

Single, dual, and multislope ADCs achieve high resolutions of 16 bits or more, are relatively inexpensive, and dissipate materially less power. These devices support very low conversion rates, typically less than a few hundred samples per second. Most applications are for monitoring DC signals in the instrumentation and industrial markets. This architecture competes with sigma-delta converters.

### 7.4. Flash Vs Sigma-Delta ADCs:

Flash ADCs do not compete with a sigma-delta architecture because currently the achievable conversion rates differ by up to two orders of magnitude. The sigma-delta architecture is suitable for applications with much lower bandwidth, typically less than 1MHz, and with resolutions in the 12- to 24-bit range. Sigma-delta converters are capable of the highest resolution possible in ADCs. They require simpler anti-alias filters (if needed) to bandlimit the signal prior to conversion.

Sigma-delta ADCs trade speed for resolution by oversampling, followed by filtering to reduce noise. However, these devices are not always efficient for multichannel applications. This architecture can be implemented by using sampled data filters, also known as modulators, or continuous-time filters. For higher frequency conversion rates the continuous-time architecture is potentially capable of reaching conversion rates in the hundreds of Msps range with low resolution of 6 to 8 bits.

This approach is still in the early research and development stage and offers competition to flash alternatives in the lower conversion rate range. Another interesting use of a flash ADC is as a building block inside a sigma-delta circuit to increase the conversion rate of the ADC.

### 7.5. Subranging ADCs:

When higher resolution converters or smaller die size and power for a given resolution are needed, multistage conversion is employed. This architecture is known as a subranging converter, also sometimes referred to as a multistep or half-flash converter. This approach combines ideas from successive approximation and flash architectures.

Subranging ADCs reduce the number of bits to be converted into smaller groups, which are then run through a lower-resolution flash converter. This approach reduces the number of comparators and reduces the logic complexity compared to a flash converter (Figure 4). The trade-off results in a slower conversion speed compared to flash.

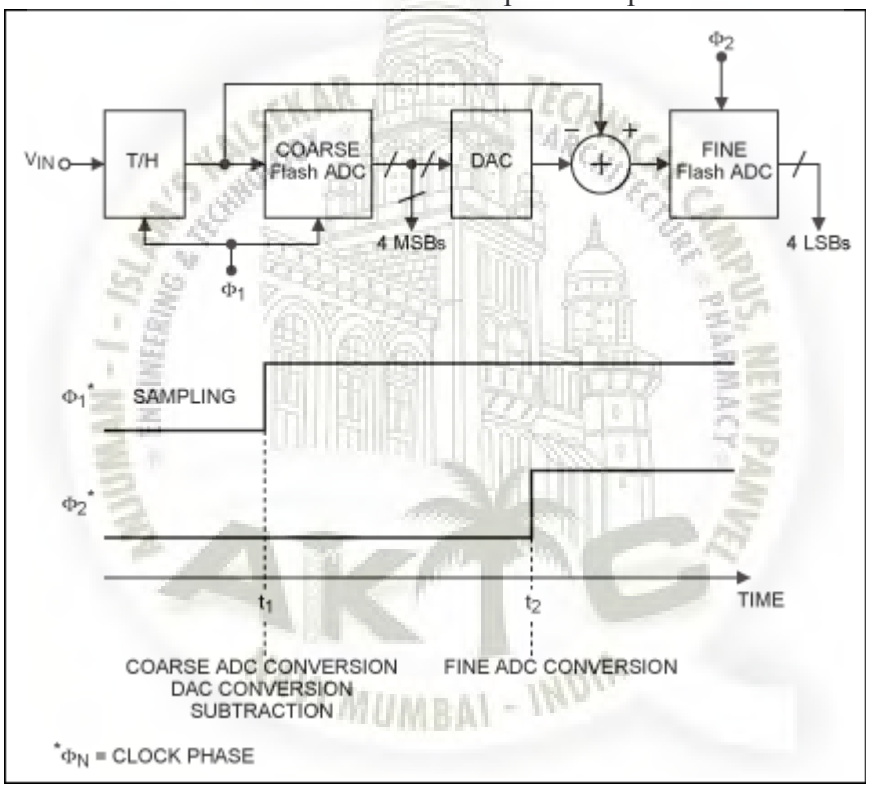



**Figure 4. Subranging ADC Architecture.**

The MAX153 is an 8-bit, 1Msps ADC implemented with a subranging architecture. This circuit employs a two-step technique. First, a conversion is completed with a 4-bit converter. A residue is created, where an 8-bit accurate DAC converts the result of the 4-bit conversion back to an analog signal. The analog signal is subtracted from the input signal. Second, this residue is again

converted by the 4-bit ADC and the results of the first and second pass are combined to provide the 8-bit digital output.

## Process Technology:

Flash converter speeds are currently in excess of 1Gsps. The 2.2Gbps MAX109 is fabricated with an advanced SiGE process. The MAX108 (1.5Gsps), MAX104 (1Gsps), and MAX106 (600Msps) 8-bit ADCs are manufactured with Maxim's proprietary, advanced GST-2 bipolar process ("giga"-speed silicon bipolar process).

CMOS flash converters are available at lower speed with resolutions compared to bipolar technology offerings. These ADCs are typically intended for integration into a larger CMOS circuit. CMOS, BiCMOS, and bipolar technologies will continue to improve, yielding increasingly higher conversion rates.

## Related Parts:

| | |
|---|---|
| MAX104 | ±5V, 1Gsps, 8-Bit ADC with On-Chip 2.2GHz Track/Hold Amplifier |
| MAX105 | Dual, 6-Bit, 800Msps ADC with On-Chip, Wideband Input Amplifier |
| MAX106 | ±5V, 600Msps, 8-Bit ADC with On-Chip 2.2GHz Bandwidth Track/Hold Amplifier |
| MAX108 | ±5V, 1.5Gsps, 8-Bit, Ultra High-Speed, A to D Converter with On-Chip 2.2GHz Track/Hold Amplifier |
| MAX109 | 8-Bit, 2.2Gsps ADC with Track/Hold Amplifier and 1:4 Demultiplexed LVDS Outputs |
| MAX1106 | Single-Supply, Low-Power, Serial 8-Bit ADCs |
| MAX1132 | 16-Bit ADC, 200ksps, 5V Single-Supply with Reference |
| | |
| MAX1449 | 10-Bit, 105Msps, Single +3.3V, Low-Power ADC with Internal Reference |
| MAX153 | 1Msps, µP Compatible, 8-Bit ADC with 1µA Power Down |
| MAX196 | 6-Channel, Multirange, 5V, 12-Bit DAS with 12-Bit Bus Interface and Fault Protection |

## ADC Input Capacitance:

$$\sigma^2(V_{th}) = \frac{A_{Vth}^2}{WL} \qquad C_g = 10\ fF/\mu m^2$$

- N = 6 bits → 63 comparators
- $V_{FS}$ = 1 V → 1 LSB = 16 mV
- σ = LSB/4 → σ = 4 mV
- $A_{VT0}$ = 10 mV·µm → L = 0.24 µm, W = 26 µm

| N (bits) | # of comp. | $C_{in}$ (pF) |
|---|---|---|
| 6 | 63 | 3.9 |
| 8 | 255 | 250 |
| 10 | 1023 | ??! |

Small Vos leads to large device sizes, hence large area and power.

Large comparator leads to large input capacitance, difficult to drive and difficult to achieve sufficient tracking bandwidth.

## Flash ADC Design Considerations:

•Use a dedicated S/H (or T/H) for better dynamic performance
Can be avoided when using the A/D inside a ΔΣloop

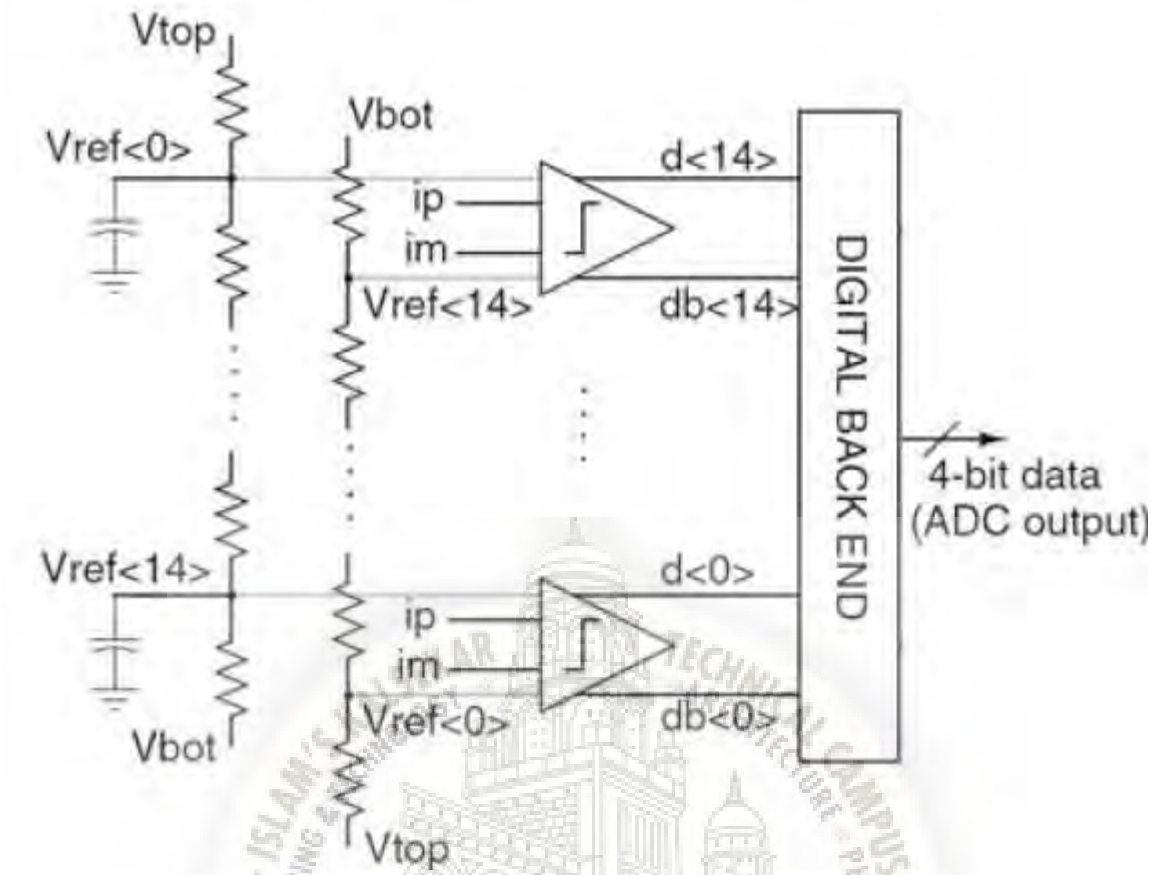
•Large input range for the quantizer has several benefits
Increased step-size (VLSB) relaxes offset requirements on the comparators

Reduced matching requirements result in small input cap to the S/H, easier to drive

Reduced input cap results in smaller clock routing parasitics–power savings in clock drivers

•Comparator Design

**Reference Ladder:**




**Differential Reference Ladder:**

•Decaps on the reference taps

large *RC*time-constant will not allow reference restoration after kickback noise

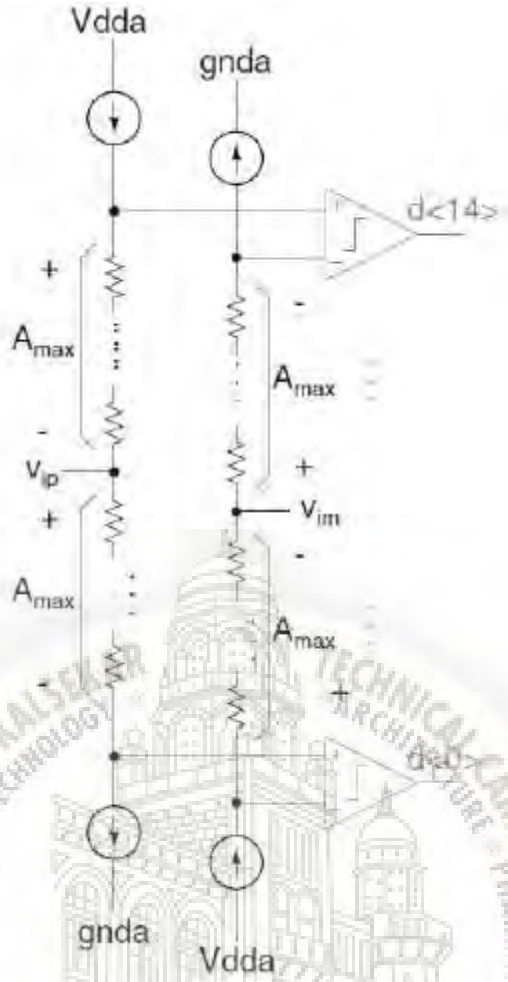
Small *R*will lead to power dissipation

Optimize *RC* time-constant value

•Subtract references from the input in a differential manner several topologies are possible

•Several architectures for the digital backend may need to pipeline digital logic at high sampling rates >500 MS/s

**Reference Substraction: Scheme I**

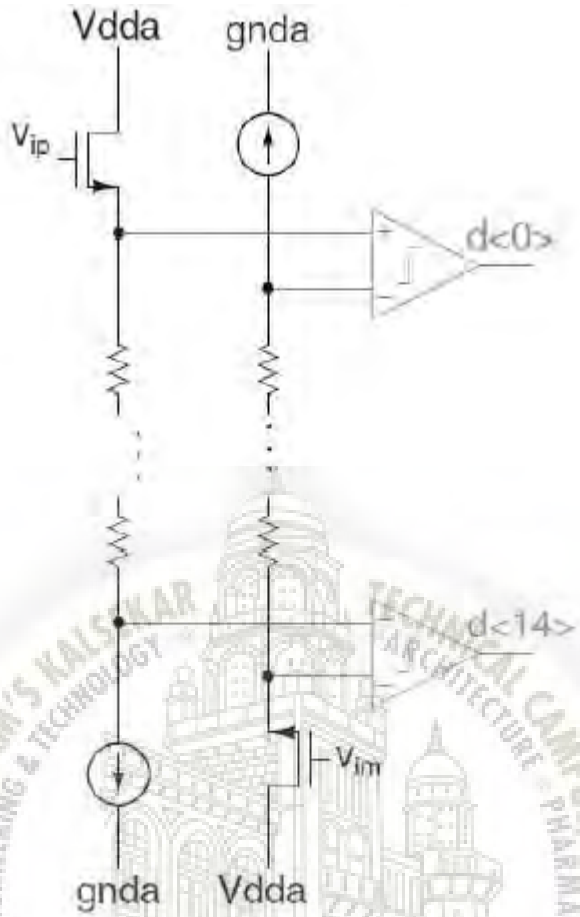



•Employ reference ladder for subtraction.

•Choose current (*I*) such that differential voltage drop across R = 1 *V*LSB

•Ladder is part of the signal path: Comparator input cap load the resistor taps, excess delay.

**Reference Substraction: Scheme II**

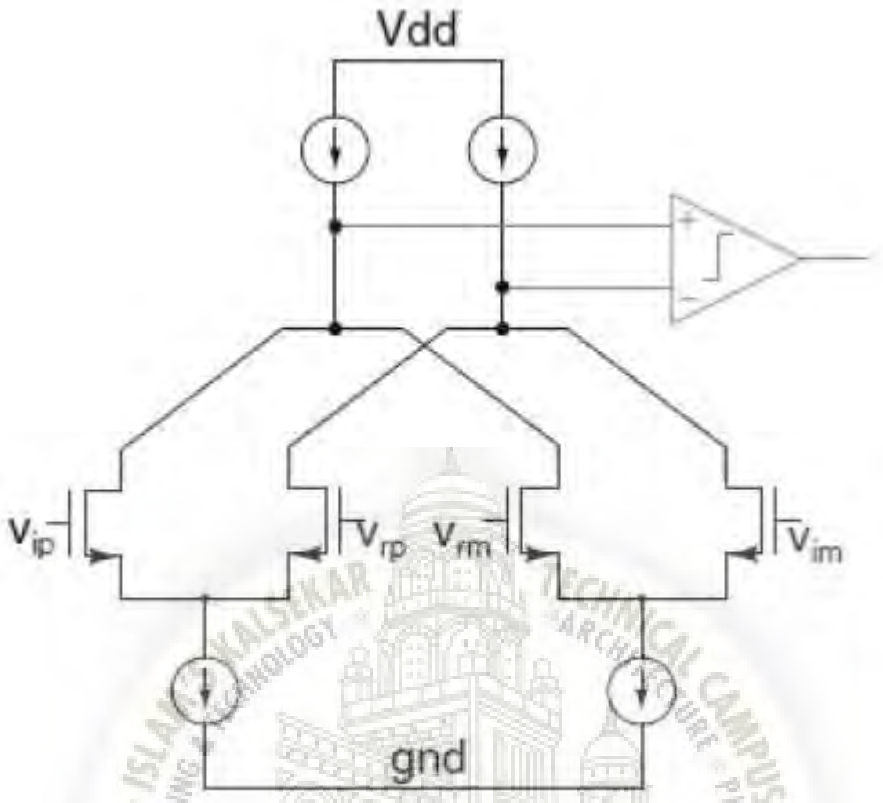



•Source followers to buffer vin
–reduced swing, varies with PVT

•Ladder is part of the signal path
–Comparator input cap load the resistor taps

–Excess delay

**Reference Substraction: Scheme III**



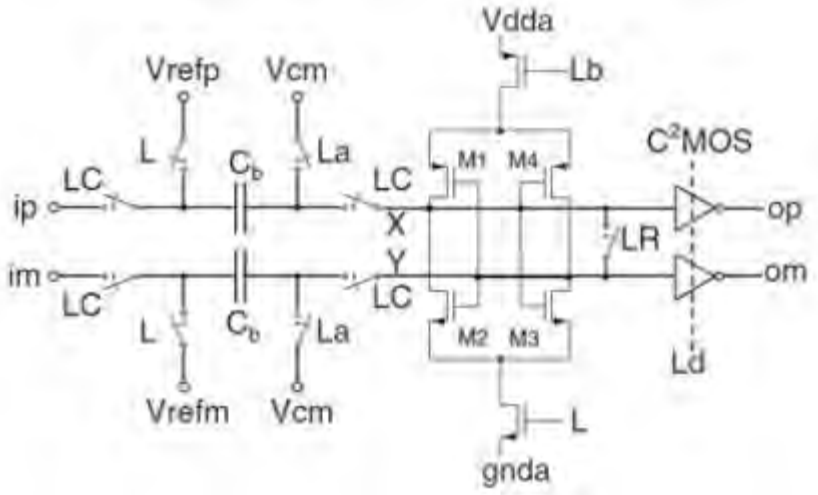

•Differential difference amplifier for subtracting the reference
–followed by a zero crossing detector

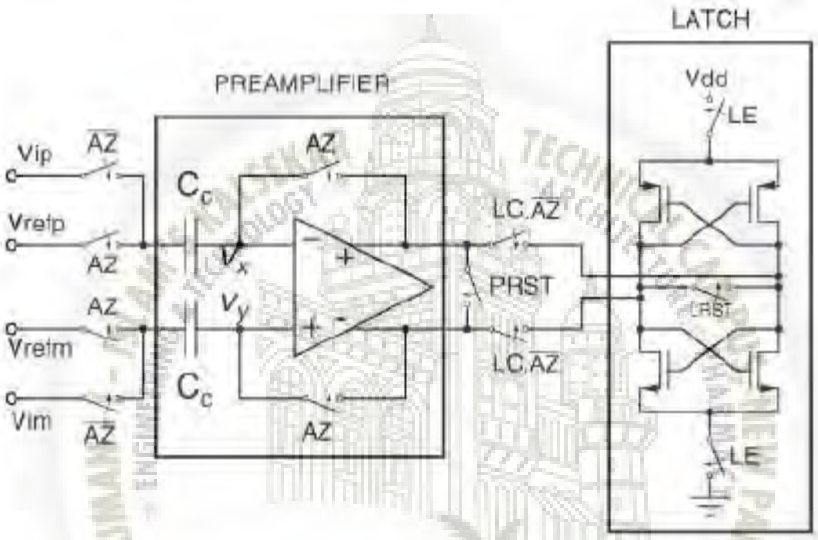
•Relaxes the impedance requirements on the ladder

•Mismatch in differential pairs and tail current sources results in comparator offset
–current trimming (see the reference below)

•Finite BW of the amplifier causes excess delay

**Reference Substraction: Scheme IV**




•Switched-capacitor reference subtraction.

–Pay attention to charge injection.

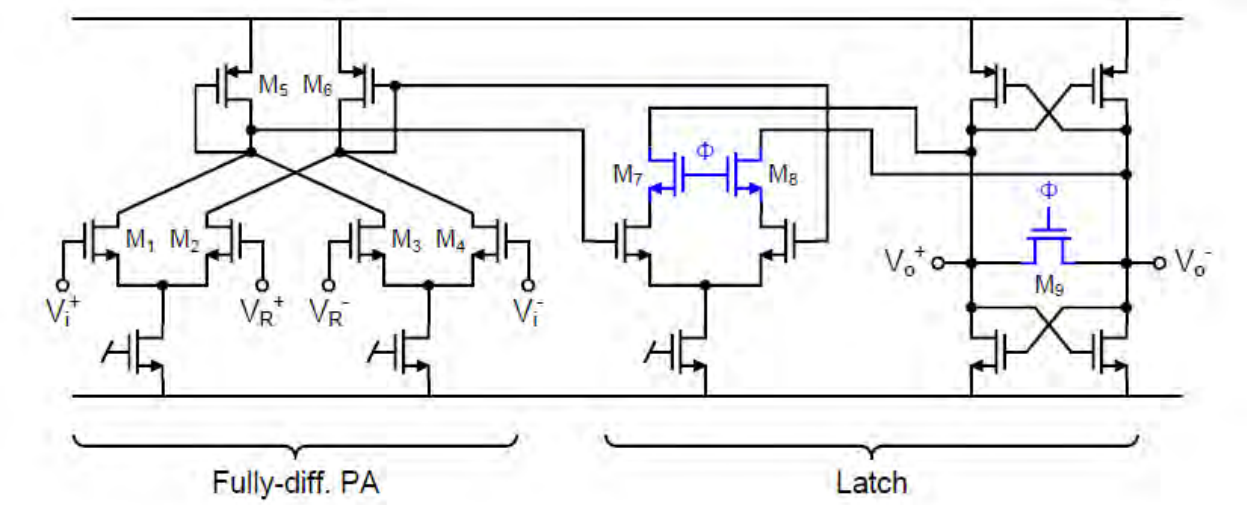
•ADC can handle large input swing.

•Slow when auto-zeroing preamp is used.

–Large settling time constant.

–Reference subtraction in background.

## Fully - Differential Comparator:




•Double-balanced, fully-differential preamp.

•Switches (M7, M8) added to stop input propagation during regeneration.

•Active pull-up PMOS added to the latch.

## Proposed Extra Bit Generation Idea:

A Flash ADC requires 2N-1 comparators to quantize the input voltage. Digitizing the data with one more bit of resolution will cost eight times more power consumption. Comparators have an integral role in decision making process and the output timing, given by (1), has valuable

information. Therefore, extra bits can be generated from time domain analysis of comparators, as shown in Fig. 2.

$$t = \tau \times \ln^{\left(\frac{V_{in(diff)}}{A_{pre}V_o}\right)}$$

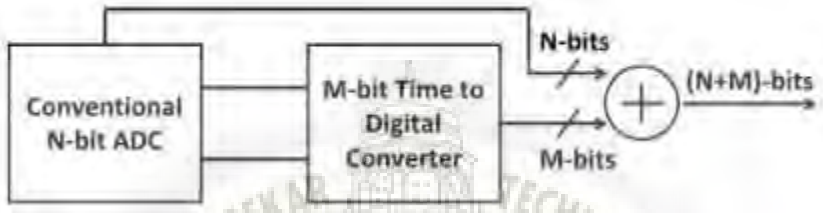



**Fig. 2. Time analysis on the conventional ADCs.**

In equation (1), τ, A □□□, V □□(□□□□), and V□ are latch time constant, preamplifier gain, input differential voltage, and output voltage, respectively. The time needed for decision making highly depends on the input differential voltage measured between input analog signal and the reference voltage, preamplifier gain and the latch time constant. As the input differential voltage becomes smaller, the comparator output voltage changes slower and hence more time is required for the final decision to be reached. This time can be utilized to do more comparison, as shown in Fig. 3.

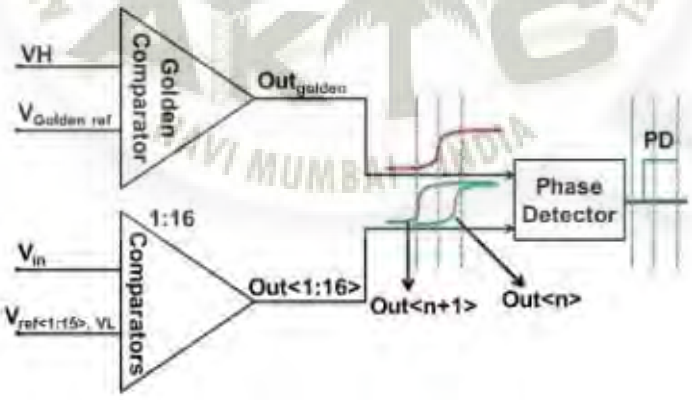



**Fig. 3. Proposed concept of generating extra bit.**

From (1), the delay is maximum for the closest comparator to the reference voltage. Therefore, the comparators delay can be compared to a reference comparator delay, called golden comparator, through a phase detector. Hence, the higher LSB and lower LSB can be

distinguished by the time analysis as shown in Figure. 4. The golden reference is generated from half of each LSB on resistor ladder.

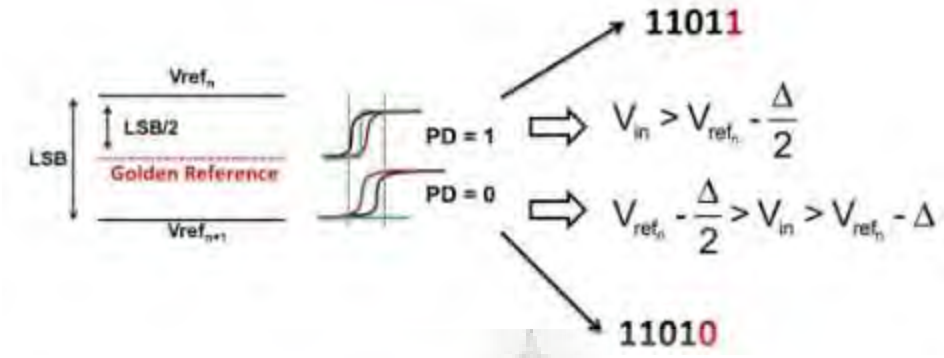



**Fig. 4. Comparison process with phase detector.**

Each LSB is divided by two which means the input is converted by half LSB. So, the proposed analog to digital converter generates an additional bit by only using 2N-1+1 comparators which is less than 2N-1 number of comparators used in conventional designs. It is worth mentioning that our design uses one more comparator for the last edge detection.

# CHAPTER 8
# ADVANTAGES, DISADVANTAGES & APPLICATONS

## Advantages:

1. It is very fast compared to other ADC's.

2. A flash converter is also quite simple, apart from the analog comparators.

3. Requires only logic for the final conversion to binary.

4. Accuracy is very high.

## Disadvantages:

1. Complex circuit.

2. A flash converter requires a huge number of comparators compared to other ADCs.

3. A flash converter requires c2^n-1comparators for an *n*-bit conversion.

4. The size, power consumption and cost of all those comparators makes flash converters generally impractical for precisions much greater than 8 bits (255 comparators).

## Applications:

The very high sample rate of this type of ADC enables high-frequency applications (typically in a few GHz range) like

1. Radar detection.
2. Wideband radio receivers.
3. Electronic test equipment.
4. Optical communication links.
5. The flash ADC is embedded in a large IC containing many digital decoding functions.
6. Also a small flash ADC circuit may be present inside a delta-sigma modulation loop.
7. Flash ADCs are also used in NAND flash memory, where up to 3 bits are stored per cell as 8 voltages level on floating gates.

## Conclusion:

The design of Flash ADC includes the design of comparator, decoder and digital to analog convertor. The performance of ADC depends on the choice of comparator. Decoder architecture consists of a Multiplexer Based decoder, which will reduce the complexity. With the help of Resistive Ladder Network the DAC architecture is implemented. The Static characteristics like Differential Non Linearity error (DNL) and Integral Non Linearity error (INL) are found in the range of +0.059/-0.00325 LSB and +0.0032/-1.5 LSB and Dynamic characteristics like SNR, SFDR, DR and ENOB are found as 25.05 dB, 22.33 dB, 26.66 dB and 3.86 bit. The Flash ADC

and DAC is implemented and characterized in the following ways: The Multiplexer based Decoder is used due to which the hardware requirement Reduces. No need of sample and hold circuit which will cause the increment in speed.

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