AIKTC/KRRC/SoET/ACKN/QUES/2018-19/ **Date:** _____

School: SoET-CBSGS **Branch:** EXTC **SEM:** VI

To,
Exam Controller,
AIKTC, New Panvel.

Dear Sir/Madam,

Received with thanks the following **Semester/Unit Test-I/Unit Test-II (Reg./ATKT)** question papers from your exam cell:

Sr. No.	Subject Name	Subject Code	Format		No. of Copies
			SC	HC	
1	Digital Communication	ETC601		✓	02
2	Discrete Time Signal Processing	ETC602			
3	Computer Communication & Telecom Networks	ETC603		✓	02
4	Television Engg.	ETC604		✓	02
5	Operating System	ETC605		✓	02
6	VLSI Design	ETC606		✓	02

Note: SC – Softcopy, HC - Hardcopy

(Shaheen Ansari)
Librarian, AIKTC

TE-sem-V – EXTC – CBSGS

Paper/Subject Code: 37001 / DIGITAL COMMUNICATION

10/5/19

Q. P. Code : 38834

(3 Hours) (Total Marks : 80

N.B. 1. Question No 1 is compulsory.
2. Attempt any three questions out of remaining five.
3. All questions carry equal marks
4. Assume Suitable data, if required and state it clearly.

1 Attempt any FOUR [20]

1 With a relevant block diagram, explain duobinary signalling scheme. Why is it called correlative coding? Write the output for bitstream 001100.

2 Compare offset and non-offset QPSK.

3 Derive the condition for maximum entropy of the source.

4 What are the different parameters which need to be examined before choosing a PCM waveform for a particular application?

5 Define code rate, Hamming distance and Hamming Weight in the context of linear block codes. Also explain the properties of generator polynomial in cyclic code.

2 a A discrete memory less source emits eight messages S_0-S_7 with probabilities 0.35, 0.3, 0.15, 0.08, 0.05, 0.03, 0.03 and 0.01 respectively. [10]

i. Create a Huffman Tree for Huffman source coding Technique using minimum variance method.
ii. Tabulate the codeword and length of codewords for each source symbol
iii. Determine the average code word length and entropy
iv. Comment on the results obtained
v. Find Information rate if source emits messages at the rate of 4000 messages per second.

b Consider (3,1,2) convolution code with $g^{(1)}=101$, $g^{(2)}=110$ and $g^{(3)}=011$ [10]

i. Draw the encoder for this code
ii. Draw the state transition diagram
iii. Using state transition diagram, find the codeword for the sequence 1101.
iv. Derive the code transfer function.

3 a Explain 16-ary PSK w.r.t. the following:- [10]

1. Modulator and
2. Demodulator
3. Power spectral density
4. Bandwidth,
5. Euclidean distance.

b Consider a (7,4) cyclic code generated by $g(x)= 1 + x^2 + x^3$. [10]
Design an encoder for systematic cyclic code generation using shift registers
Using encoder implemented in (i) and not otherwise, find the code word for message (1001).
Suppose the received vector is R = (0 0 1 0 1 1 0), find the syndrome using syndrome circuit.
Find out the generator matrix for the above cyclic code.

TURN OVER

4 a Why MSK is called 'shaped QPSK'? For the bit sequence, 1011010, draw the MSK waveform (Consider m3) [10]

b Explain Direct sequence spread spectrum (DS-SS) with neat diagram. Explain processing gain and Jamming Margin with necessary expressions. [10]

5 a Consider a Systematic block code whose Parity check equations are: [10]

P1= m1+m2 + m3 P2= m1 + m2 + m4

P3= m1+m3 + m4 P4 = m2 + m3 + m4

where mi are message bits and Pi are parity check bits. In a codeword parity bits appear before message bits.

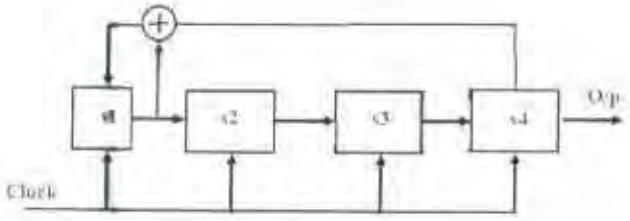
(i) Find Generator matrix (G) and Parity check matrix (H)

(ii) Find the codeword for the message vectors: 1001, 1101

(iii) How many errors can the code correct and detect?

(iv) If the received codeword is 10011101, decode the message.

b The following circuit is used to generate PN sequence with initial content (Seed) as 1011. **[10]**



i. Write down the PN sequence.

ii. Verify the balance property of PN Sequence.

iii. Verify the Auto-correlation property of the PN sequence.

6 a a. What do you mean by eye diagram? What is its purpose? Draw the ideal eye pattern. Mention the various parameters observed from the eye pattern. Explain with help of suitable illustration. [10]

b What is matched Filter? State and explain maximum likelihood decision rule. Explain the function of correlator receiver. [10]

(9) TE - sem-VI - CBSGS - CCTN - EXTC 22/5/19

Paper / Subject Code: 37003 / COMPUTER COMMUNICATION AND TELECOM NETWORKS

Duration: 3 hours **Max marks: 80**

Note the following instructions.

i) Question No.1 is compulsory (attempt any 4)
ii) Total 4 questions need to be solved
iii) Attempt any three questions from remaining five questions.

1.a	What is the difference between unicast and Multicast routing?	**[5]**
1.b	What are the types of timers used in TCP, Explain?	**[5]**
1.c	A company is granted the site address 201.70.64.0(Class).The Company needs six subnets .Design the subnets.	**[5]**
1.d	Explain Shortest path algorithm with suitable diagram.	**[5]**
1.e	Explain the difference between a connection oriented and connectionless service.	**[5]**
2.a	Explain Various network hardware devices in detail.	**[10]**
2.b	i. What is distance vector routing and link state routing.	**[5]**
	ii. Explain exterior and interior routing.	**[5]**
3.a	What are different types of ARQ? Explain GO BACK N ARQ	**[10]**
3.b	What is HDLC? What are HDLC frame types, Explain modes of operation in details.	**[10]**
4.a	Draw and explain TCP Header format.	**[10]**
4.b	Explain TCP congestion control policy.	**[10]**
5.a	What is carrier sensing? Explain CSMA/CD and CSMA/CA in detail.	**[10]**
5.b	What is ALOHA? What are the types of ALOHA? Compare them.	**[10]**
6	Write a short notes **(any two)**: a. ISO-OSI network model b. Transmission Media c. DNS	**[20]**

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Paper / Subject Code: 37004 / TELEVISION ENGINEERING

Q.P. Code :23610

[Time: Three Hours] **[Marks:80]**

Please check whether you have got the right question paper.

N.B:
1. Question.No.1 is compulsory.
2. Answer any Three out of remaining six questions.
3. Draw the neat diagrams wherever necessary.

Q.1	1	Answer the following	20
	a.	Draw and Explain of color difference signal circuit.	
	b.	Explain the specification of vertical sync pulse and need of serrations in it	
	c.	What is the function electron multiplier in image orthicon camera tube	
	d.	Explain EBU MAC system in brief.	
Q2	a)	What is NTSC? Draw and explain NTSC Decoder.	20
	b)	What is MUSE system? Explain its technical specifications, advantages and disadvantages.	
Q3	a)	Draw and Explain half line discrepancy. How can it be eliminated?	20
	b)	Explain: 1) Why (G-γ) signal is not selected for transmission? 2) Explain how effective number of lines is evolved.	
Q4	a)	Draw sync separator section in Television system and explain it in detail.	20
	b)	Draw and explain color television camera system and what the purpose of dichroic lance is.	
Q.5	a)	Draw and explain delta gun color picture tube.	20
	b)	Explain MAC signal its compression technique and scanning frequency.	
Q.6		Write short notes on (any two)	20
	a)	Cancellation of phase error in PAL.	
	b)	Compatibility factors for monochrome and color television.	
	c)	DTH Television system.	

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TE-sem-VI - CBSGS - EXTC

Paper / Subject Code: 37005 / OPERATING SYSTEMS

3/6/19

(3 Hours) **[Total Marks : 80]**

N.B. (1) Question No. 1 is compulsory
(2)Assume suitable data if necessary
(3)Attempt any three questions from remaining questions

1
(a) Draw and explain process state transition diagram. (5)
(b) What is kernel of an Operating System? Explain different types of kernels. (5)
(c) Explain the concept of segmentation. (5)
(d) What are the characteristics of a Real Time OS? (5)

2 (a) Consider the following set of processes with CPU burst time given in milliseconds. (10)

Process	Burst time	Arrival time
P1	10	1
P2	4	2
P3	5	3
P4	3	4

Draw Gantt chart for FCFS and Shortest Remaining Time First (SRTF) and calculate average waiting time and average turnaround time.

(b) Explain how logical address is translated into physical address using paging mechanism with the help of a diagram. (10)

3 (a) Explain Buddy algorithm in LINUX memory management. (10)
(b) Consider the following snapshot (10)

Process	Allocation			Max			Available		
	A	B	C	A	B	C	A	B	C
P0	1	3	5	0	6	5	1	3	5
P1	1	0	0	2	1	3			
P2	2	0	1	3	4	6			
P3	4	1	1	1	5	7			
P4	5	4	3	0	0	1			

Answer the following using Banker's algorithm.
(i) What is the content of matrix Need?
(ii) Is the system in the safe state?
(iii) If the request from process P1 arrives for (0, 4, 2, 0) can request be granted immediately?

4 (a) Explain the working of EDF and RMA real time scheduling algorithms. (10)

(b) Calculate page hit and page miss for the following string using page replacement policies FIFO and LRU. Page frame size is 3. (10)

1,2,3,2,1,5,2,1,6,2,5,6,3,1,3,6,1,2,4,3

5 (a) Explain Disk Arm Scheduling algorithms. (10)

(b) What is semaphore? Give an implementation of bounded buffer producer consumer problem using semaphore. (10)

6 (a) What are system calls? Explain any five system calls. (10)

(b) Explain how UNIX performs file management using I-nodes. (10)

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TE-sem-V - CBSGS - EXTC

Paper / Subject Code: 37006 / VLSI DESIGN

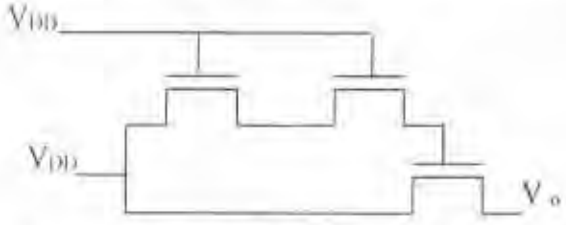
10/6/19

Time: 3 Hours **Marks: 80**

1] Question no.**1** is **compulsory**
2] Attempt any **three** questions out of remaining questions
3] Assume **suitable data** if **required**
4] **Figures** to the **right** indicate marks.

Q. No. 1) Solve the following [20]

a) Calculate the voltage at the output node V_o if V_{DD}=5V and V_{tn}=1.5V



b) Draw and Explain Clocked SR latch using static CMOS design style.
c) Draw layout diagram of static CMOS inverter based on lambda design rules.
d) Draw VTC of static CMOS inverter and show operating regions of nMOS and pMOS transistors on it.
e) Explain short channel effects (any two).

Q. No. 2)

a) Explain in detail the fabrication process steps for a CMOS inverter using n- well process with the help of cross sectional view for each step. [10]

b) Implement a two input XOR gate using
(i) static CMOS logic
(ii) Dynamic logic
(iii) Transmission gate
(iv) Pseudo NMOS logic [10]

Q. No. 3)

a) Derive an expression for the inverter threshold voltage (switching voltage) of a CMOS inverter. Calculate the (W/L) ratios of the NMOS and PMOS transistor in the CMOS inverter circuit with the following parameters:
V_{DD} = 3V $V_{t0,n}$= 0.6V $V_{t0,p}$ = -0.8V V_{TH}=1.5V
$\mu_n C_{OX}$=60μA/V² $\mu_P C_{OX}$ =20μA/V² [10]

b) Draw schematic diagram of six transistor SRAM cell and explain its Read and Write operations. [10]

Q. No. 4)

a) What is scaling. Compare constant field scaling with constant voltage scaling and state advantages and limitations in both the methods. [10]

b) Design a 4- bit CLA adder using dynamic NMOS logic. Compare delay of this circuit with respect to a 4 bit ripple carry adder. [10]

Q. No. 5)

a) Draw the CMOS circuit for $Y = \overline{A + BC(D + E) + F}$ and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs. assuming that $(W/L) = 15$ for all pMOS transistors and $(W/L) = 10$ for all nMOS transistors. [10]

b) Explain in detail static and dynamic power dissipation. What are the main components which make power dissipation in CMOS circuit? [10]

Q. No.6) Explain any 2 of the following [20]

a. 4 bit Array Multiplier
b. Interconnect Delay model
c. 3-T DRAM

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