SE-ET. SemIII (cold) DLD.

(OLD COURSE)

02/12/2014

QP Code:12289

[Total Marks: 100 (3 Hours) N.B.: (1) Question No. 1 is compulsory. (2) Attempt any four from remaining six questions. (3) Figures to the right indicate full marks. 1. (a) Convert (154.25)₁₀ into binary, octal and hexadecimal number systems. 5 (b) Design one bit digital comparator. (c) Design a full adder using 8:1 MUX. 5 (d) Simplify the following using Boolean laws. $f = \overline{A} \overline{B} \overline{C} + A \overline{B} \overline{C} + BC + \overline{A} \overline{B} C + A \overline{B} C$ (a) Simplify using k-map and realize using NAND gates only. 10 $f(A, B, C, D) = \sum m(1,3,7,11,15) + d(0,2,5)$ (b) Using Boolean laws prove that NAND and NOR gates as universal gates. 10 10 3. (a) Design a BCD to 7 segment code converter. 10 (b) Draw a 3 bit binary up-down counter using JK-FF. (a) What is a race around condition? How it is overcome in Master Slave J-K 10 Flip-Flop. (b) Design a 3 bit Binary to Gray code converter ad implement. 10 (a) Draw a 4 bit universal shift register and explain its operation as shift left and 10 right. (b) Draw a 2 input TTL NAND gate and explain its operation. 10 6. (a) Simplify using Quine McClusky Method. 10 $f(A,B,C,D) = \sum m(0,1,2,3,4,6,8,9,10,11)$ (b) Implement the following expression using basic logic gates. 10 $f(A, B, C, D) = \sum m(0, 1, 3, 5, 7, 9, 10, 15)$ 20 Write short notes on any two :--(a) Priority Encoder (b) TTL Vs CMOS logic family (c) PAL and PLA (d) FPGA and CPLD.