

SE-ET
Sem III (CBSGS)
Digital Electronics

02/12/2014

QP Code :14614

(3 Hours)

[Total Marks :80

- N.B. : (1) Question no 1 is **compulsory**.
(2) Out of remaining questions, attempt any **three** questions.
(3) **Assume** suitable additional data if required.
(4) Fig. in brackets on **right** hand side indicates **full** marks.

1. (a) Compare Moore and Mealy machines models. 5
(b) Design a 4:1 multiplexer using only NAND gates. 5
(c) Write a VHDL code for full adder. 5
(d) Convert SR F/F to D F/F. 5
2. (a) Implement the following Boolean function with 8:1 multiplexer. 10
 $F(A,B,C,D) = \pi m(0,3,5,6,8,9,10,12,14)$
(b) State truth table of 3 bit Gray to Binary conversion then design it using 3:8 decoder and additional gates. 10
3. (a) Use the quine-Mc-Cluskey method of minimization and find the expression for the function. 10
 $F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,9,11,14)$
(b) Define the following in terms of Logic families 10
(i) Propagation delay
(ii) Fanout
(iii) Power Dissipation
(iv) Figures of Merit
(v) Noise margin
4. (a) Design ripple counter using JK flip flop for the state. 10
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- (b) (i) Give the advantage and disadvantage of CMOS family. 10
(ii) Implement a full-subtractor using two-Half-Subtractors.
5. (a) Design an even parity generator with 3 data bits. 10
(b) Explain any one shift register in detail. 10
6. (a) Draw and explain the block diagram of architecture of XC9500 CPLD family. 10
(b) Explain Johnson counter or twisted ring counter. 10