VLSI D : VI SEM ET : CBSGS

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09/06/2015

QP Code : 5141

(3 Hours) [Total Marks : 80

N.B. : (1) Question no. 1 is compusory.
(2) Answer any three questions out of remaining questions.
(3) Assume suitable data if required.

1. Solve any five :- 20
   (a) Draw layout of 2 input CMOS NOR gate using lambda (λ) rules.
   (b) Implement Master Slave D Flip Flop using C²MOS logic style.
   (c) Explain various sources of power dissipation in CMOS Inverter.
   (d) Implement NOR based 2:4 decoder.
   (e) State various short channel effects and explain one of them.
   (f) Draw static CMOS NAND and NOR gates. Size all transistors in NAND and NOR gate to provide worst case equal rise and fall delay for both gates. Assume mobility of electron is two times higer than that of holes. Magnitude of threshold voltage for all transistor is same.

2. (a) Draw six transistor CMOS SRAM cell. Describe various constraints that should be imposed on the devices for guaranteeing safe read and write operation. Derive the equation that would help to size the transistors and also based on derived equations, discuss qualitatively relative sizing of transisters in the cell. 10

   (b) Implement $Y = \overline{AB + C(D+E)}$ using 10
   (i) Static CMOS logic.
   (ii) Dynamic logic with pull up network.
   (iii) Dynamic logic with pull down network.
   (iv) Pesudo NMOS logic.

3. (a) With the help of neat cross sections and appropriate masks, give the process flow of N-well CMOS technology. 10

   (b) For CMOS Inverter with following parameters. 10

$$V_{TO,n} = 0.6\ V \qquad \mu_n C_{ox} = 60\mu A/V^2, \left(\frac{W}{L}\right)_n = 8$$

$$V_{TO,p} = -0.7\ V \qquad \mu_p C_{ox} = 20\mu A/V^2, \left(\frac{W}{L}\right)_p = 12$$

Calculate noise margins and the switching threshold of the inverter. The power supply voltage $V_{DD} = 3.3$ V.

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4. (a) Design clocked CMOS JK latch to implement the truth table shown below. 10

Clk	J	K	Q_{n+1}
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\overline{Q}_n$ (toggle)

(b) Explain 4 × 4 bit array muiltiplier with the help of necessary hardware for the generation and addition of partial product. 10

5. (a) In two input CMOS NAND gate , $\mu_n C_{ox} = 20\mu A/V^2$, $\mu_n C_{ox} = 10\mu A/V^2$, and all PMOS have $\left(\frac{W}{L}\right)_n = 20$, $V_{TO,n} = 1$ V and $V_{TO,p} = -1$ V. If one of the input is held permenantly at V_{DD} and other is switched from zero volts to V_{DD} with zero rise time for a duration grater than fall delay of NAND gate and then switched back to zero volts with zero fall time, then calculate t_{pHL} and t_{pLH}. Asume V_{DD} = 5V and total load capacitance which is independent of MOSFET sizes is equal to 2PF. 10

(b) With the help of suitable diagrams explain how clock is generated and stabilized in VLSI chip. 5

(c) Explain with help of neat diagrams importance of power distribution network in VLSI chip. 5

6. Write short notes on any **four** :- 20

(a) Flash memory
b) Carry look ahead adder
(c) ESD protection circuit
(d) Barrel Shifter
(e) Interconnect scalling.

Course: T.E.(SEM VI)(CBSGS)(E&TC)(prog 585 TO 598)

Q.P Code: 5141

Correction:

Q.no.(5)(a) (check following image)

Que 5(a)

(i) read $\mu_n C_{ox} = 10 \mu A/V^2$

as $\mu_p C_{ox} = 10 \mu A/V^2$

(ii) read , and all PMOS have $\left(\frac{W}{L}\right) = 20$

as , and all NMOS and PMOS have $\left(\frac{W}{L}\right) = 20$

(~~Rest~~ No change in remaing part of Q.5(a))

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Note: Take printouts and distribute them to concerned students