Q.P. Code : **4836**

(3 Hours) [Total Marks : 80

N.B. : (1) Question No. **1** is **compulsory**.
(2) **Assume** suitable data if **necessary**.
(3) Attempt any **three** questions out of the remaining **five**.

1. (a) Convert $(121.2)_3$ into base 10. 2
   (b) Represent $(52)_{10}$ into Excess - 3 code and Gray code. 2
   (c) Find the one's complement and two's complement of $(57)_{10}$. 2
   (d) Realize $y = AB + \overline{AB}$ using NAND gates only. 2
   (e) Obtain hamming code for 1011. 2
   (f) Convert $(126)_{10}$ to Octal, Hexcode. 2
   (g) State demorgans law. 2
   (h) Convert $(214.32)_{10}$ to binary. 2
   (i) Perform binary subtraction using 2's complement for $(62)_{10}$ and $(99)_{10}$ 4

2. (a) Minimize the logic function using Quine-McCIuskey method.
   $f (A,B,C,D) = \Sigma m \ (1,3,7,9,10,11,13,15)$ 12
   (b) Implement the following expression using single 4:1 Mux.
   $f = (A,B,C,D) = \Sigma m \ (0,1,2,4,6,9,12,14)$ 8

3. (a) Design a 4-input (A,B,C,D) digital circuit that will give at its output (X) a logic 1 only if the binary number formed at the input is between 2 and 9 (including). 10
   (b) Simplify $Y = \overline{\left(A + \overline{A} B\right) \left(C + \overline{D}\right)}$ 5
   (c) Design 1 bit comparator using logic gates. 5

4. (a) Given the logic expression
   $$A + \overline{B}\overline{C} + AB\overline{D} + ABCD$$ 12
      (i) Express in standard SOP
      (ii) Draw K-map for the equation.
      (iii) Minimize and realize using NAND gates only.
   (b) Design 8 bit BCD adder. 8

5. (a) Design a mod 5 synchronous up counter using JK FF. 10
   (b) Convert SR FF to TFF and JK FF. 10

6. Write short note on (**any three**) 20
      (a) VHDL
      (b) Multivibrators
      (c) Gray code & Excess-3code
      (d) Johnson Ring Counter

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