SE - sem - III - old - EXTC

PLD

26/5/15

QP Code : **4683**

**(OLD COURSE)**

**(3 Hours)** **[ Total Marks : 100**

**N.B.** (1) Question No. **1** is **compulsory**.

(2) Solve any **four** out of remaining **six** questions.

(3) **Each** question carries **20** marks. **Equal** marks for the subquestions.

(4) Assume **suitable** data if **required**.

1. (a) Perform the following operations –

(i) $(1101{\cdot}0)_2 \times (110.1)_2$

(ii) $(57)_8 - (47)_8$

(iii) $(75)_{10} - (55)_{10}$ using 2's complement method.

(iv) $(111010{\cdot}110)_2 \div (1010)_2$

(b) (i) Explain minterm and Maxterm

(ii) Justify, NAND & NOR gates are Universal gates.

(iii) Find M if $(193)_M = (623)_8$

(iv) Differentiate between synchronous and Asynchronous counter.

2. (a) Prove the following using boolean algebraic theorems

(i) $\overline{(\overline{AB} + \overline{A} + AB)} = 0$

(ii) $AB + \overline{AC} + A\overline{B}C\,(AB + C) = 1$

(b) State and prove DeMorgan's theorems.

3. (a) Simplity the following boolean function by using Quine Mc Cluskey method.

$F(A,B,C,D) = \Sigma m\,(0, 2, 3, 6, 7, 8, 10, 12, 13)$

(b) Minimize the following logical equation using K-map and design the minimized equation using logic gates.

$F(A,B,C,D) = \Pi M\,(0, 2, 3, 8, 9, 12, 13, 15)$

4. (a) Design the logic ckt for 1-bit comparator using NAND gates only.

(b) Draw and explain the working of clocked S-R Flip Flop with preset and clear using NAND gates only.

5. (a) Design the logic ckt for Mod-6 Ripple counter using MS-JK FFs.
   (b) Design the logic ckt for 3-bit SIPO Register using MS-D-FFs.

6. (a) Design the logic ckt for Full Subtractor using 3:8 Decoder.
   (b) Design and implement the given logical equation using 16:1 Multiplexer.
   $Y = \Sigma m\ (1, 3, 4, 8, 10, 11, 12, 14, 15)$

7. (a) Explain TTL and ECL Logic Families.
   (b) Explain PAL and PLA.

---