BE-sem-VII – CBGS- EXTC

VLSI

17/12/15

QP Code : 6202

(3 Hours) **[Total Marks : 80**

N.B.: (1) **Question No. 1** is compulsory and solve any three from the remaining five questions.
(2) Figures to right indicate full marks.
(3) Assume suitable data if required and mention the same in the answer sheet.

1. Solve **any four** from the following **20**
   a) Explain various problems associated with MOSFET switch.
   b) What are advantages and disadvantages of cascode current mirror over two transistor simple current mirror. How to overcome disadvantages associated with cascode current mirror.
   c) Find voltage gain and maximum output voltage swing for common source amplifier with resistive load of 2K. Assume MOSFET with $V_{TN} = 1V$, $(W/L) = 10$, $\mu nCox = 100\mu A/V^2$, $V_{DD} = 5V$ and DC bias at Gate is 2V .
   d) Explain various performance parameters of CMOS operational Amplifier.
   e) Explain various issues associated with mixed signal circuit layout.

2. a) With the help of neat circuit diagram explain working common source amplifier with diode connected PMOS load. Derive expression for its voltage gain and output resistance. What happens to the performance of the amplifier if diode connected PMOS load is replaced by diode connected NMOS load. **10**
   b) Draw circuit diagram of resistive load differential amplifier with constant current source as tail current. Explain its working with the help of voltage transfer characteristics and derive expression for differential voltage gain using superposistion theorem. **10**

3. a) Design two stage Operational Transconductance Amplifier (OTA) to satisfy following specifications with phase margin of 60^0. Assume for all transistors $L = 1\mu m$ **15**
   i) $Av \geq 3000$ V/V
   ii) Slew rate ≥ 5 V/μs
   iii) Gain Bandwidth = 5MHz
   iv) Power dissipation ≤ 2mW
   v) Input common Mode Range (ICMR) = -0.5V to 1.5V

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vi) Output swing = ± 1.5V
Assume V_{DD} = 2.0V and V_{SS} = -2.0V .
Load Capacitance C_L = 5PF. Use NMOS transistors with V_{TN} = 0.5V, μnCox = 120 μA/V², λn = 0.02V⁻¹ and PMOS transistors with V_{TP} = -0.5V, μpCox = 60 μA/V², λp = 0.03V⁻¹.
Calculate expected voltage gain and power dissipation for designed circuit.

b) Why frequency compensation is necessary for operational amplifiers. Explain Miller's compensation techinque with respect to two stage OTA. 5

4. a) Explain in detail working of switched capacitor integrator. 10

b) Explain different types of noise sources present in MOS circuits. Derive expression for the total noise voltage of the single stage common-source amplifier with resistive load. 10

5. a) Consider a 3-bit D/A converter in which Vref = 4V, with the following measured values. 10
{0.011 : 0.507 : 1.002 : 1.501 : 1.996 : 2.495 : 2.996 : 3.491}
Find the INL and DNL errors in units of LSB.

b) With the help of neat diagram, explain in detail working of charge scaling DAC. What are limitations of charge scaling DAC architecture and how to overcome the same. 10

6. Write short notes on **any four** 20
i) Two step flash ADC
ii) CMOS comparator
iii) Band gap voltage reference
iv) Common mode response of differential pair
v) Cyclic DAC
