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QP Code : 5401

(3 hours)   Total marks: 80

N.B   1) Question no 1 is compulsory

2) Attempt any three questions from remaining five questions

3) Assume suitable data if required

4) Draw neat diagram wherever necessary.

1. Solve any four each question carries 5 marks

a) Explain role of different registers like IR, PC,SP,AC,MAR and MDR used in Von Neumann
model.   [5]
b) Differentiate between Computer Organization and Computer Architecture.   [5]

c) List different memory organization characteristics   [5]

d) What is virtual memory?   [5]

e) Show IEEE 754 standards for Binary Floating Point Representation for 32 bit single format and
64 bit double format.   [5]

2.   (a) I) Draw the flow chart for Booth's Algorithm for twos complement multiplication.   [4]

II) Using Booth's algorithm show the multiplication of -3 * -7.   [6]

(b) What are differences between RISC and CISC processor?   [10]

3.   (a)Describe hardwire control unit and specify its advantages.   [10]

(b) Explain six stage instruction pipeline with suitable diagram.   [10]

4.   (a) Calculate the hit and miss using various page replacement policies LRU,OPT,FIFO for
following sequence (page frame size 3) 4,7,3,0,1,7,3,8,5,4,5,3,4,7 . State which one is best for
above example?   [10]

(b) What is TLB? Explain working of TLB   [10]

5.   (a) compare interrupt driven I/O and DMA   [10]

(b) Explain Flynn's classification   [10]

6.   (a) explain set associative and associative cache mapping techniques   [10]

(b) What is bus arbitration? Explain any two techniques of bus arbitration.   [10]

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