Q.P. Code : **1255**

(3 Hours) [Total Marks :100

N.B. : (1) Question no. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Figures on the right indicate full marks.
(4) Assume suitable data, wherever necessary.

1. (a) Explain Booth's algorithm with the help of a flowchart and hence multiply 10
-13×7
(b) Explain with diagram the different cases of Flynn's classification. 10

2. (a) Explain Von-neumann model. 10
(b) List various methods of Hardwired control unit and explain any one in 10
detail

3. (a) Explain with examples the IEEE 754 standards of floating point format. 10
(b) Explain the programmed I/O, Interrupt driven I/O and DMA methods of I/O 10
access.

4. (a) Explain with neat diagram Wilkie's micro programmed control unit. 10
(b) Compare RISC and CISC. 5
(c) Compare SRAM and DRAM. 5

5. (a) Explain different cache mapping techniques. 10
(b) Explain six stage pipelining with block diagram. 10

6. (a) What is the need of bus hierarchy. Explain with diagram the concept of 10
bus hierarchy.
(b) Explain with the help of flowchart non-restoring method of division and 10
hence divide 10 ÷ 3

7. Write short notes on:- (**any four**) 20
(a) Characteristics of two level memory.
(b) Systolic array architecture.
(c) Demand paging.
(d) USB
(e) PCI
(f) Static and Dynamic data flow model.

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QP-Con. 12204-15.