SE - sem-III - old - computer

DLDA

9/12/15

Q.P. Code : **1189**

(3 Hours) **[Total Marks : 100**

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions from question no. **2** to 7.
(3) Assume **suitable** data if **necessary**.

1. (a) State and verify De-Morgan's Theorem. **20**
   (b) Verify that 'A universal gate can perform 'AND' and 'OR' operation.
   (c) Discuss any three characteristics of TTL logic family.
   (d) Difference between Synchronous and Asynchronous Circuits.

2. (a) Represent $(-27)_{10}$ in (i) Sign Magnitude representation **5**
   (ii) One's Complement form (iii) Two's Complement form
   (b) Simplify $\overline{\overline{A\overline{B}} + ABC + A(B + \overline{A}B)}$ **5**
   (c) Perform without conversion to any other base. **4**
   (i) $(61)_8 * (36)_8$ (ii) $(A\ B\ C\ D)_H - (2A\ FF)_H$
   (d) Convert $(86.2)_{10}$ into octal, binary and hexadecimal number system. **6**

3. (a) Simplify using K-map and realize the SOP equation using only NAND gates. **10**
   $F(A, B, C, D) = \Sigma m(0, 2, 3, 7, 9, 12, 13) + d(1)$
   (b) Design Mod-10 Synchronous counter using 'T' flipflops. Avoid Lock out condition. Draw the state diagram. **10**

4. (a) Design a FULL adder using half adders and gates. **10**
   (b) Design 2-bit Asynchronous up/down counter. Draw neat waveforms. **10**

5. (a) Design a 3 bit bidirectional shift register using JK FlipFlops. **10**
   (b) Simplify using Quine Mc Cluskey method the following logic function. **10**
   $F(A, B, C, D, E) = \Sigma m(0, 1, 2, 6, 8, 10, 11, 14, 15, 16, 17, 20, 21, 24, 30) + \Sigma d(13, 18)$

6. (a) Convert 'D' FlipFlop to JK FlipFlop and 'T' FlipFlop.. **10**
   (b) Explain transfer characteristics of TTL NAND gate along with Voltage parameters. **10**

7. Write notes on following :- **20**
   (a) Twisted Ring Counter
   (b) TTL and CMOS Logic Families
   (c) Error detecting and Correcting Codes
   (d) Arithmetic Logic Unit
   (e) Master Slave JK FlipFlop.
