SE-sem-II-old-EXTC

3/12/15

DLD

QP Code : **1163**

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**
(2) Solve **any four** out of remaining **six** questions
(3) Each question carries **20 marks.** Equal marks for the subquestions.
(4) Assume suitable data if required.

1. (a) Obtain Gray code and Excess-3 code for $(9599)_{10}$
   (b) Obtain equivalant Binary, octal, Hexadecimal nos. for $(8588)_{10}$
   (c) Do the followings using 2'S complement method
      (i) $(54)_{10} - (45)_{10}$
      (ii) $(56)_{10} - (65)_{10}$
   (d) Design 2-I/P AND operation using 2-I/P NOR gates only

2. (a) State and prove Demorgan's theorems.
   (b) Design the logic ckt for following logical eqⁿ using NAND gates only.
   $$Y = (A + \overline{B}).(A + \overline{B} + C)$$

3. (a) Design the logic ckt for Full Adder using logic gates.
   (b) Minimize the following logical eqn using k-map & design the minimized eqⁿ using logic gates.
   $$Y = \sum m\,(1,3,7,11,15) + d(0,2,5)$$

4. (a) Design and Explain the logic ckt for 4:1 MUX using logic gates.
   (b) Design the logic ckt for Full ADDER using only one 3:8 Decoder (use some necessary gates if required)

5. (a) Explain the following terms related to flipfiops
      (i) Set (ii) Reset
      (iii) Preset (iv) Clear
   (b) Design the logic ckt for conversion of T-FF into D-FF

6. (a) Design and explain the logic ckt for 3-bit synchronous counter using MS-JK FFs
   (b) Design and explain the logic ckt for 3-bit SISO register (With O/p waveforms) using MS-JK FFs.

7. Write short notes on any four :-
   (i) Weighted and Non-weighted codes
   (ii) Asynchronous counter
   (iii) ECL Logic family
   (iv) PAL & PLA
   (V) Quine Mc-cluskey method.

QP-Con. 9647-15.