SE/CO/Sem-IV CBSGS/COA

23/5/16

**Q.P. Code : 541501**

**(3 Hours)** **[ Total Marks : 80**

**N.B. :** (1) Q. **1** is **compulsory**.
(2) Attempt any **THREE** out of the remaining questions.
(3) Assume suitable **data** if necessary.

1. Attempt any **4** sub questions.
   (a) Explain various pipeline hazards. **5**
   (b) Express $(35.25)_{10}$ in the IEEE single precision standard of floating point representation. **5**
   (c) Explain in brief the function of 8089 I/O processor. **5**
   (d) Compare RISC and CISC processors. **5**
   (e) Differentiate between Computer Architecture and Computer organization. **5**

2. (a) Explain Flynn's classification in detail. **10**
   (b) Explain the Interleaved memory. **10**

3. (a) Calculate number of page faults and page hits for the page replacement policies FIFO, Optimal & LRU for given reference string 7, 0, 1, 2, 0, 3, 0, 4, 2, 3, 0, 3, 2, 1, 2, 0, 1, 7, 0, 1 (assuming three frame size). **10**
   (b) What is the need of DMA? Explain its various techniques of data transfer. **10**

4. (a) What is Bus arbitration? Explain its techniques. **10**
   (b) Describe the register organization within the CPU. **10**

5. (a) What are the features of cache memory design? **10**
   (b) Multiply (-10) and (-4) using Booth's algorithm. **10**

6. Write notes on
   (a) Joysticks **6**
   (b) The characteristics of memory **8**
   (c) Microinstructions to execute an instruction MOV [RI], R2. **6**

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