Analog Electronics - I

An Introduction

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ANALOG ELECTRONICS- I

SR. NO.	NAME OF THE TOPIC
1.	Field Effect Transistor
2.	Biasing of BJT'S
3.	Biasing of FET'S and MOSFET'S
4.	Small Signal Analysis Of BJTS
5.	Small Signal Analysis of FETS
6.	High Frequency Response of FETS and BJTS

Topic 1 FIELD EFFECT TRANSISTORS

1.1 INTRODUCTION

The field-effect transistor (FET) is a three-terminal device used for a variety of applications that match, to a large extent. Although there are important differences between the two types of devices, there are also many similarities.

The primary difference between the two types of transistors is the fact that the BJT transistor is a *current-controlled* device as depicted in Fig. 1.1(a), while the JFET transistor is a *voltage-controlled* device as shown in Fig. 1.1(b). In other words, the current I_C in Fig. 1.1(a) is a direct function of the level of I_B. For the FET the current I will be a function of the voltage V_{GS} applied to the input circuit as shown in Fig. 1.1(b).

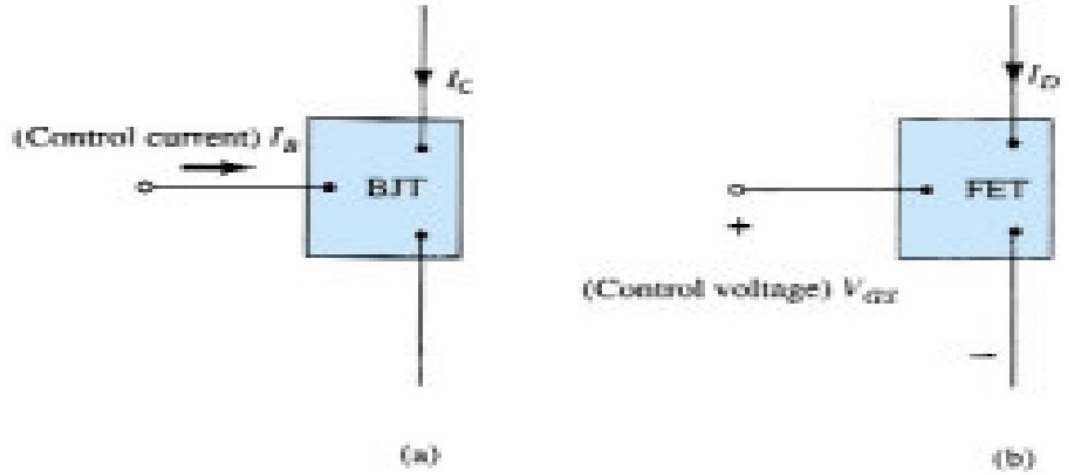


Fig. 1.1 (a) Current-controlled and (b) voltage-controlled amplifiers

In each case the current of the output circuit is being controlled by a parameter of the input circuit—in one case a current level and in the other an applied voltage. Just as there are*npn* and*pnp* bipolar transistors, there are *n-channel* and *p-channel* field-effect transistors. However, it is important to keep in mind that the BJT transistor is a *bipolar* device—the prefix *bi-* revealing that the conduction level is a function of two charge carriers, electrons and holes. The FET is a *unipolar* device depending solely on either electron (*n*-channel) or hole (*p*-channel) conduction.

The term field-effect in the chosen name deserves some explanation. For the FET an *electric field* is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

One of the most important characteristics of the FET is its *high input impedance.* At a level of 1 to several hundred mega ohms it far exceeds the typical input resistance levels of the BJT transistor configurations—a very important characteristic in the design of linear ac amplifier systems. On the other hand, the BJT transistor has a much higher sensitivity to changes in the applied signal. In other words, the variation in output current is typically a great deal more for BJTs than FETs for the same change in applied voltage. For this reason, typical ac voltage gains for BJT amplifiers are a great deal more than for FETs. In general, FETs are more temperature stable than BJTs, and FETs are usually smaller in construction than BJTs, making them particularly useful in *integrated-circuit (IC)* chips. The construction characteristics of some FETs, however, can make them more sensitive to handling than BJTs.

Two types of FETs are there: the *junction field-effect transistor* (JFET) and the *metal-oxide-semiconductor field-effect transistor (MOSFET).*
The MOSFET category is further broken down into depletion and enhancement types. The MOSFET transistor has become one of the most important devices used in the design and construction of integrated circuits for digital computers. Its thermal stability and other general characteristics make it extremely popular in computer circuit design.

1.2 CONSTRUCTION AND CHARACTERISTICS OF JFETs

The JFET is a three-terminal device with one terminal capable of controlling the current between the other two.
The basic construction of the *n*-channel JFET is shown in Fig. 1.2. Note that the major part of the structure is the *n*-type material that forms the channel between the embedded layers of *p*-type material. The top of the *n*-type channel is connected through an ohmic contact to a terminal referred to as the *drain (D),* while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the *source (S).* The two *p*-type materials are connected together and to the *gate (G)* terminal. In essence, therefore, the drain and source are connected to the ends of the *n*-type channel and the gate to the two layers of *p*-type material. In the absence of any applied potentials the JFET has two *p-n* junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig. 1.2 that resembles the same region of a diode under no-bias conditions. A depletion region is that region void of free carriers and therefore unable to support conduction through the region. The drain and source terminals are at opposite ends of the *n*-channel as introduced in Fig. 1.2 because the terminology is defined for electron flow.

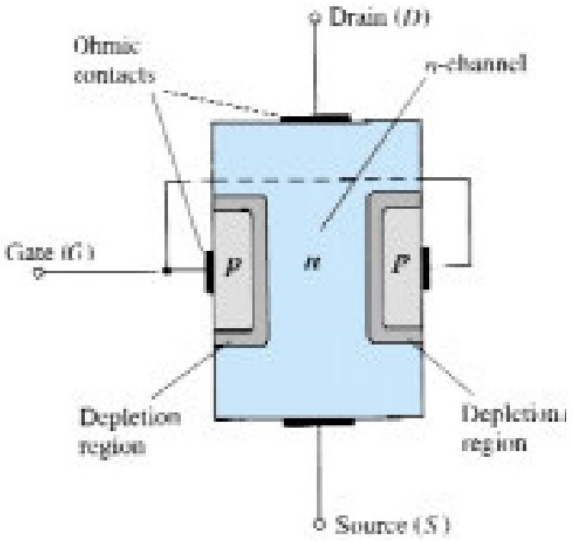


Fig 1.2 Junction field-effect transistor (JFET)

V_{GS} = 0 V, V_{DS} Some Positive Value

In Fig. 1.3, a positive voltage V_{DS} has been applied across the channel and the gate has been connected directly to the source to establish the condition V_{GS} = 0 V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each *p*-material similar to the distribution of the no-bias conditions of Fig. 1.2. The instant the voltage V_{DD} (= V_{DS}) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current I_D with the defined direction of Fig. 1.3. The path of charge flow clearly reveals that the drain and source currents are equivalent ($I_D = I_S$). Under the conditions appearing in Fig. 1.3, the flow of charge is relatively uninhibited and limited solely by the resistance of the *n*-channel between drain and source.

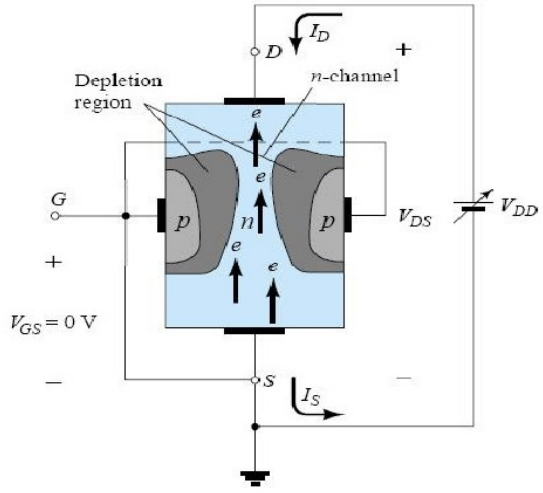


Fig 1.3 JFET in the V_{GS} = 0 V and V_{DS}> 0 V

As the voltage V_{DS} is increased from 0 to a few volts, the current will increase as determined by Ohm's law and the plot of I_D versus V_{DS} will appear as shown in Fig. 1.4. The relative straightness of the plot reveals that for the region of low values of V_{DS}, the resistance is essentially constant. As V_{DS} increases and approaches a level referred to as V_P in Fig. 1.4, the depletion regions of Fig. 1.3 will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph of Fig. 1.4 to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching "infinite" ohms in the horizontal region.

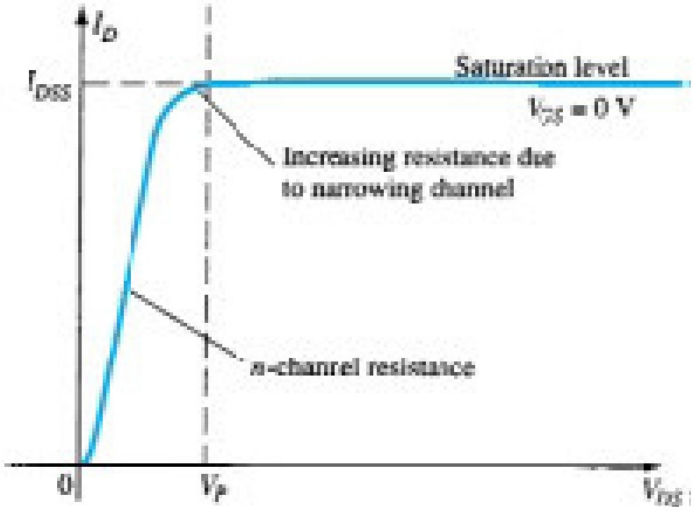


Fig 1.4 I_D versus V_{DS} for V_{GS}=0 V

If V_{DS} is increased to a level where it appears that the two depletion regions would "touch" as shown in Fig. 1.5, a condition referred to as *pinch-off* will result. The level of V_{DS} that establishes this condition is referred to as the *pinch-off voltage* and is denoted by V_P as shown in Fig. 1.4. In actuality, the term *pinch-off* suggests the current I_D is pinched off and drops to 0 A. As shown in Fig. 1.4, I_D maintains a saturation level defined as I_{DSS}. In reality a very small channel still exists, with a current of very high density. The fact that I_D does not drop off at pinch-off and maintains the saturation level indicated in Fig. 1.4 is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the *n*-channel material to establish the varying levels of reverse bias along the *p-n* junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

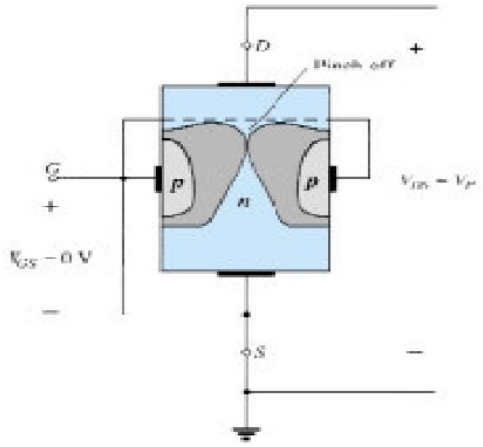


Fig 1.5 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$)

As V_{DS} is increased beyond V_P, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of I_D remains essentially the same. In essence, therefore, once $V_{DS} = V_P$ the JFET has the characteristics of a current source. As shown in Fig. 5.8, the current is fixed at $I_D = I_{DSS}$, but the voltage V_{DS} (for levels > V_P) is determined by the applied load.

I_{DSS} is the maximum drain current for a JFET and is defined by the conditions $V_{GS} = 0$ V and $V_{DS} > |V_P|$.

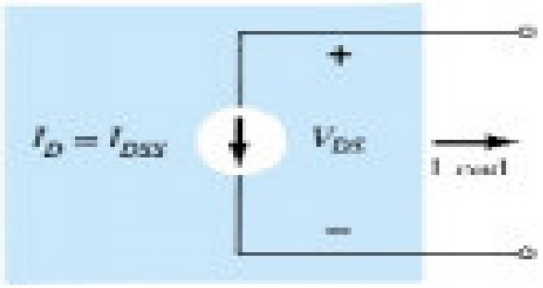


Fig 1.6 Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$

***VGS* = 0 V**

The voltage from gate to source, denoted V_{GS}, is the controlling voltage of the JFET. Just as various curves for I_C versus V_{CE} were established for different levels of I_B for the BJT transistor, curves of I_D versus V_{DS} for various levels of V_{GS} can be developed for the JFET. For the *n*-channel device the controlling voltage V_{GS} is made more and more negative from its $V_{GS} = 0$ V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source.

In Fig. 1.7 a negative voltage of -1 V has been applied between the gate and source terminals for a low level of V_{DS}. The effect of the applied negative-bias

V_{GS} is to establish depletion regions similar to those obtained with $V_{GS} = 0$ V but at lower levels of V_{DS}. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of V_{DS} as shown in Fig. 1.8 for $V_{GS} = -1$ V.

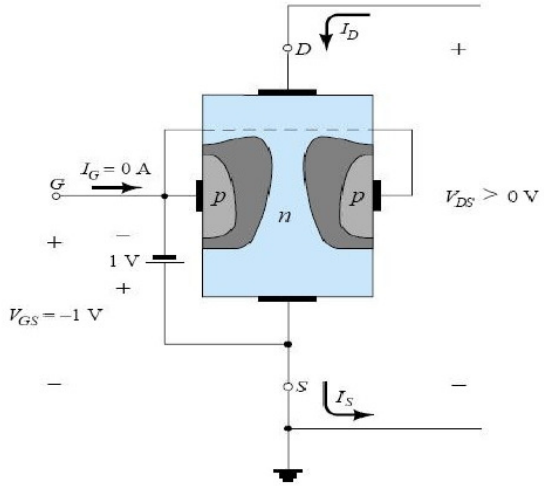


Fig 1.7 Application of a negative voltage to the gate of a JFET

The resulting saturation level for I_D has been reduced and in fact will continue to decrease as V_{GS} is made more and more negative. Note also on Fig. 1.8 how the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative. Eventually, V_{GS} when $V_{GS} = -V_P$ will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been "turned off."

In summary:

The level of V_{GS} that results in $I_D = 0$ mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

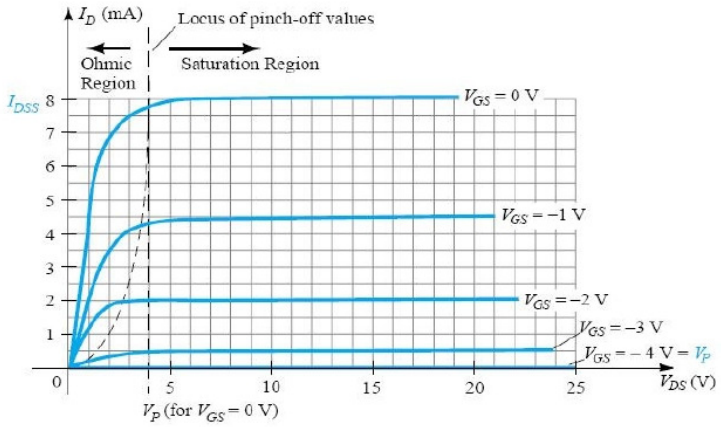


Fig 1.8 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = 4$ V

The region to the right of the pinch-off locus of Fig. 1.8 is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the *constant-current, saturation,* or *linear amplification region.*

Voltage-Controlled Resistor

The region to the left of the pinch-off locus of Fig. 1.8 is referred to as the *ohmic* or *voltage-controlled resistance region.* In this region the JFET can actually be employed as a variable resistor (possibly for an automatic gain control system) whose resistance is controlled by the applied gate-to-source voltage. Note in Fig. 1.8 that the slope of each curve and therefore the resistance of the device between drain and source for $V_{DS} = V_P$ is a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative, the slope of each curve becomes more and more horizontal, corresponding with an increasing resistance level.

$$\mathbf{r_d = r_0 / [1- (V_{GS}/V_P)^2]} \text{ ---------- (5.1)}$$

where r_o is the resistance with V_{GS} = 0 V and r_d the resistance at a particular level of V_{GS}.

P-Channel Devices

The *p*-channel JFET is constructed in exactly the same manner as the *n*-channel device of Fig. 1.2, but with a reversal of the *p*- and *n*- type materials as shown in Fig. 1.9.

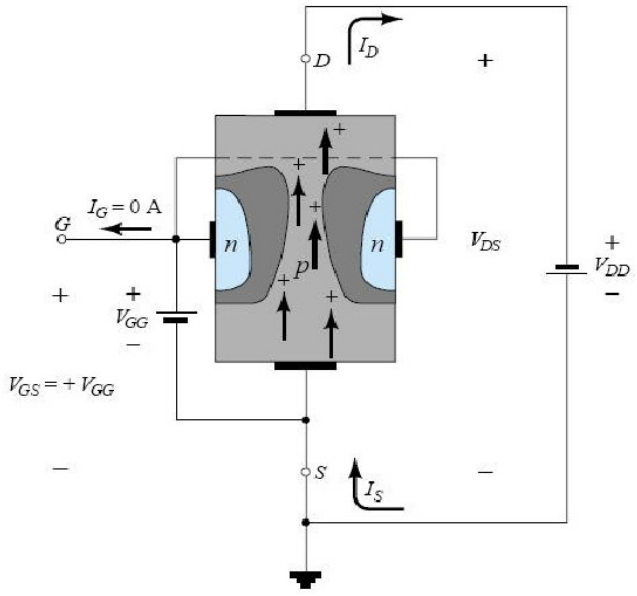


Fig 1.9 *p*-Channel JFET

The defined current directions are reversed, as are the actual polarities for the voltages V_{GS} and V_{DS}. For the *p*-channel device, the channel will be constricted by increasing positive voltages from gate to source and the double-subscript notation for V_{DS} will result in negative voltages for V_{DS} on the characteristics of Fig. 1.10, which has an I_{DSS} of 6 mA and a pinch-off voltage of V_{GS} = +6 V. Do not let the minus signs for V_{DS} confuse you. They simply indicate that the source is at a higher potential than the drain.

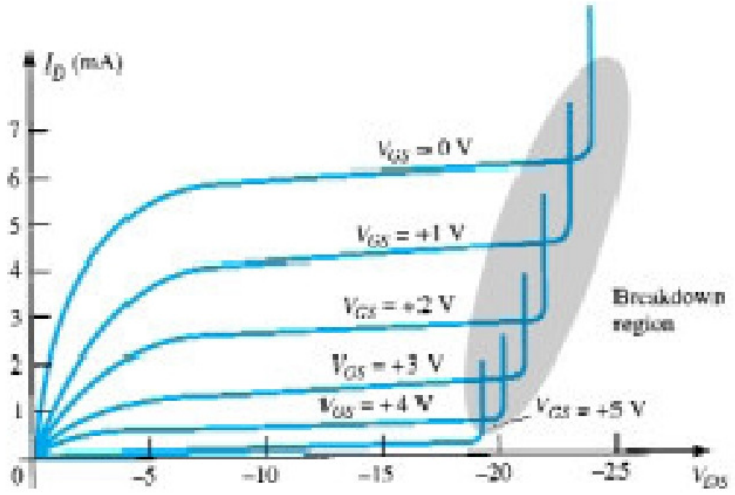


Fig 1.10 *p*-Channel JFET characteristics with I_{DSS} = 6 mA and V_P = +6 V

Note at high levels of V_{DS} that the curves suddenly rise to levels that seem unbounded. The vertical rise is an indication that breakdown has occurred and the current through the channel (in the same direction as normally encountered) is now limited solely by the external circuit. Although not appearing in Fig. 1.8 for the *n*-channel device, they do occur for the *n*-channel device if sufficient voltage is applied. This region can be avoided if the level of $V_{DS\text{max}}$ is noted on the specification sheet and the design is such that the actual level of V_{DS} is less than this value for *all* values of V_{GS}.

Symbols

The graphic symbols for the *n*-channel and *p*-channel JFETs are provided in Fig. 1.11. Note that the arrow is pointing in for the *n*-channel device of Fig. 1.11(a) to represent the direction in which I_G would flow if the *p*-*n* junction were forward-biased. For the *p*-channel device (Fig. 1.11(b)) the only difference in the symbol is the direction of the arrow.

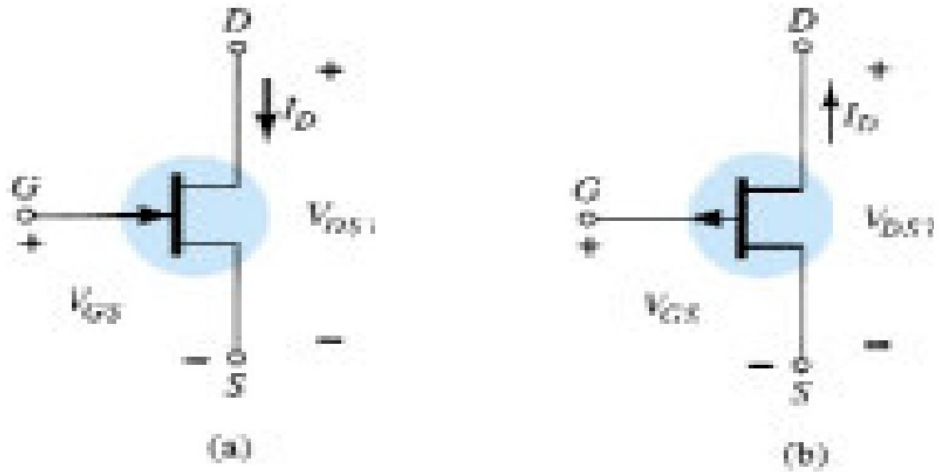
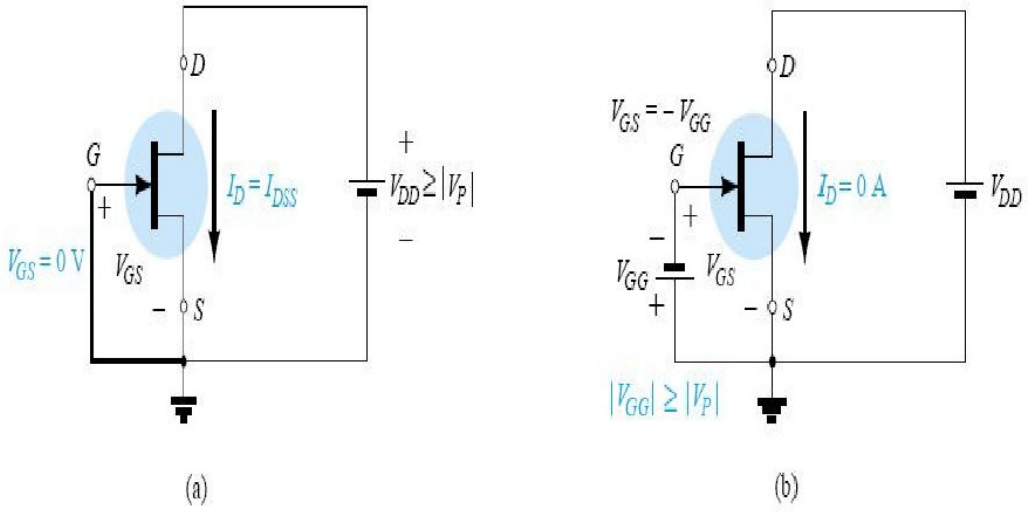
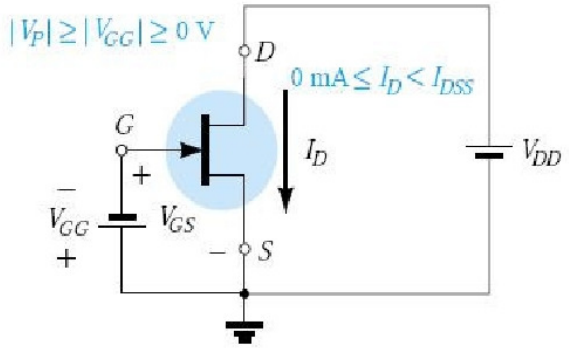


Fig 1.11 JFET symbols: (a) *n*-channel; (b) *p*-channel

Summary

- ***The maximum current is defined as I_{DSS} and occurs when V_{GS} = 0 V and VDS ≥\|VP\| as shown in Fig. 1.12(a).***
- ***For gate-to-source voltages V_{GS} less than (more negative than) the pinch-off level, the drain current is 0 A (I_D = 0 A) as appearing in Fig. 1.12(b).***
- ***For all levels of V_{GS} between 0 V and the pinch-off level, the current I_D will range between I_{DSS} and 0 A, respectively, as reviewed by Fig. 1.12(c).***
- ***For p-channel JFETs a similar list can be developed.***





(c)

Fig 1.12 (a) V_{GS} =0 V, $I_D = I_{DSS}$; (b) cutoff (I_D = 0 A) V_{GS} less than the pinch-off level; (c) I_D exists between 0 A and I_{DSS} for V_{GS} less than or equal to 0 V and greater than the pinch-off level.

1.3 TRANSFER CHARACTERISTICS

For the BJT transistor the output current I_C and input controlling current I_B were related by beta, which was considered constant for the analysis to be performed. In equation form,

$$I_C = f(I_B) = \beta I_B \text{ ----------(1.2)}$$

In Eq. (1.2) a linear relationship exists between I_C and I_B. Double the level of I_B and I_C will increase by a factor of two also.

Unfortunately, this linear relationship does not exist between the output and input quantities of a JFET. The relationship between I_D and V_{GS} is defined by ***Shockley's equation:***

$$\mathbf{I_D = I_{DSS}(1- V_{GS}/V_P)^2} \text{ ----------(1.3)}$$

The squared term of the equation will result in a nonlinear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

The graphical approach, however, will require a plot of Eq. (1.3) to represent the device and a plot of the network equation relating the same variables. The solution is defined by the point of intersection of the two curves. It is important to keep in mind when applying the graphical approach that the device characteristics will be *unaffected* by the network in which the device is employed. The network equation may change along with the intersection between the two curves, but the transfer curve defined by Eq. (1.3) is unaffected.

In general, therefore:

The transfer characteristics defined by Shockley's equation are unaffected by the network in which the device is employed.

The transfer curve can be obtained using Shockley's equation or from the output characteristics of Fig. 1.8. In Fig. 1.13 two graphs are provided, with the vertical scaling in milli amperes for each graph. One is a plot of I_D versus V_{DS}, while the other is I_D versus V_{GS}. Using the drain characteristics on the right of the "y" axis, a horizontal line can be drawn from the saturation region of the curve denoted $V_{GS} = 0$ V to the I_D axis. The resulting current level for both graphs is I_{DSS}. The point of intersection on the I_D versus V_{GS} curve will be as shown since the vertical axis is defined as $V_{GS} = 0$ V.

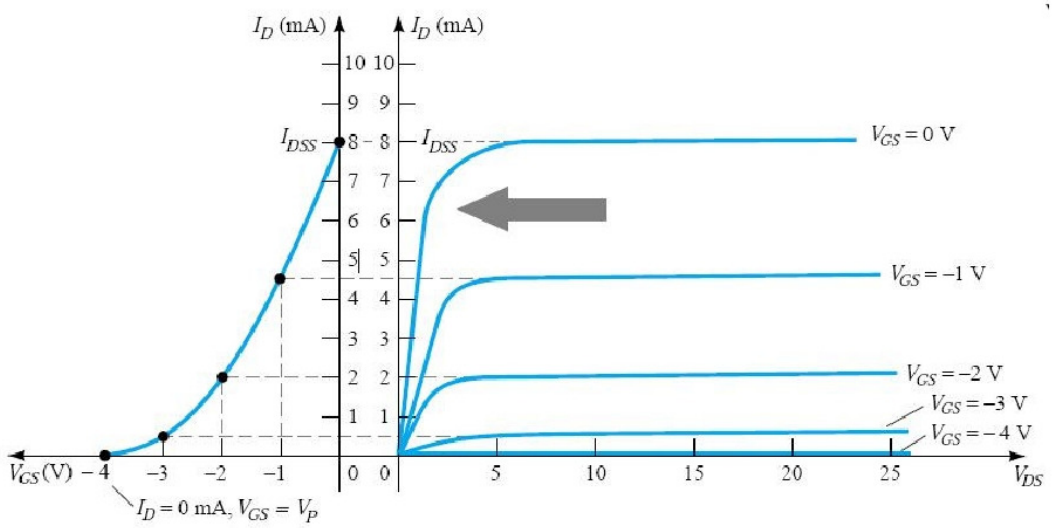


Fig 1.13 Obtaining the transfer curve from the drain characteristics

In review:
When $V_{GS} = 0$ V, $I_D = I_{DSS}$.

When $V_{GS} = V_P = -4$ V, the drain current is zero milli amperes, defining another point on the transfer curve. That is:
When $V_{GS} = V_P$, $I_D = 0$ mA.

The drain characteristics relate one output (or drain) quantity to another output (or drain) quantity—both axes are defined by variables in the same region of the device characteristics. The transfer characteristics are a plot of an output (or drain) current versus an input-controlling quantity. There is therefore a direct "transfer" from input to output variables when employing the curve to the left of Fig. 1.13. If the relationship were linear, the plot of I_D versus V_{GS} would result in a straight line between I_{DSS} and V_P. However, a parabolic curve will result because the vertical spacing between steps of V_{GS} on the drain characteristics of Fig. 1.13 decreases noticeably as V_{GS} becomes more and more negative. Compare the spacing between $V_{GS} = 0$ V and $V_{GS} = -1$ V to that between $V_{GS} = -3$ V and pinch-off. The change in V_{GS} is the same, but the resulting change in I_D is quite different.

Applying Shockley's Equation

The transfer curve of Fig. 1.13 can also be obtained directly from Shockley's equation (1.3) given simply the values of I_{DSS} and V_P. The levels of I_{DSS} and V_P define the limits of the curve on both axes and leave only the necessity of finding a few intermediate plot points.

Substituting $V_{GS} = 0$ V in equation 1.3 gives,

$$\mathbf{I_D = I_{DSS}|_{VGS = 0v}} \text{----------(1.4)}$$

Substituting $V_{GS} = V_P$ yields,

$$\mathbf{I_D = 0V|_{VGS = VP}} \text{----------(1.5)}$$

For the drain characteristics of Fig. 1.13, if we substitute $V_{GS} = -1$ V,

$$I_D = 4.5\text{mA}$$

as shown in Fig. 1.13. Note the care taken with the negative signs for V_{GS} and V_P in the calculations above. The loss of one sign would result in a totally erroneous result.

It should be obvious from the above that given I_{DSS} and V_P (as is normally provided on specification sheets) the level of I_D can be found for any level of V_{GS}. Conversely, an equation for the resulting level of V_{GS} for a given level of I_D

$$\mathbf{V_{GS} = V_P\left(1 - \frac{\quad}{\quad}\right)} \text{----------(1.6)}$$

Shorthand Method

$$I_D = I_{DSS}|_{VGS = VP/2} \text{----------(1.7)}$$

$$V_{GS} = 0.3V_P|_{ID = IDSS/2} \text{---------- (1.8)}$$

TABLE 5.1 V_{GS} versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
0.3 V_P	$I_{DSS}/2$
0.5 V_P	$I_{DSS}/4$
V_P	0 mA

1.4 IMPORTANT RELATIONSHIPS

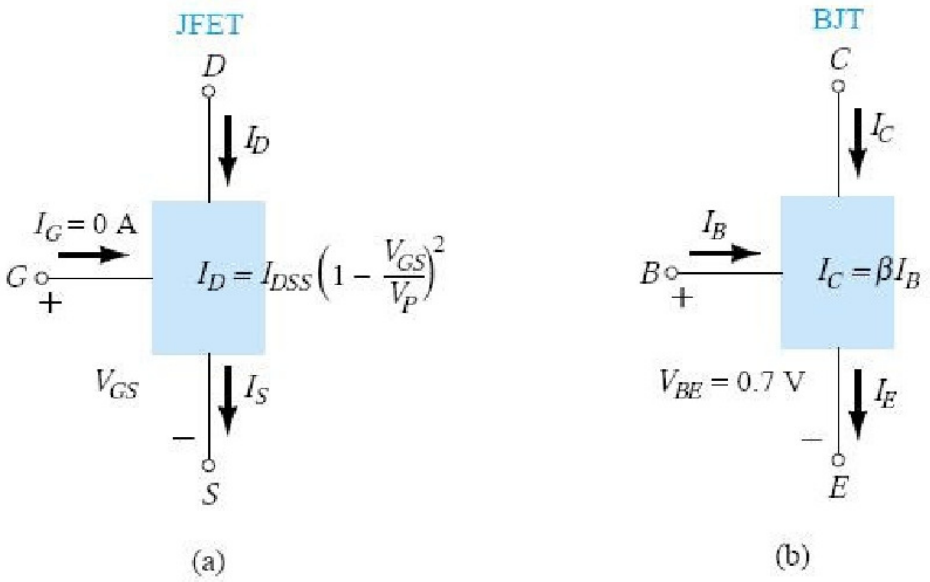


Fig 1.14 (a) JFET versus (b) BJT

JFET		*BJT*
$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$	$\Leftrightarrow$	$I_C = \beta I_B$
$I_D = I_S$	$\Leftrightarrow$	$I_C \cong I_E$
$I_G \cong 0$ A	$\Leftrightarrow$	$V_{BE} \cong 0.7$ V

A clear understanding of the impact of each of the equations above is sufficient background to approach the most complex of dc configurations. Recall that V_{BE} = 0.7 V was often the key to initiating an analysis of a BJT configuration. Similarly, the condition $I_G = 0$ A is often the starting point for the analysis of a JFET configuration.

For the BJT configuration, I_B is normally the first parameter to be determined. For the JFET, it is normally V_{GS}.

1.5 DEPLETION-TYPE MOSFET

There are two types of FETs: JFETs and MOSFETs. MOSFETs are further broken down into *depletion type* and *enhancement type.* The terms *depletion* and *enhancement* define their basic mode of operation, while the label MOSFET stands for *m*etal-*o*xide-*s*emiconductor-*f*ield-*e*ffect *t*ransistor. thedepletion-type MOSFET, which happens to have characteristics similar to those
of a JFET between cut-off and saturation at I_{DSS} but then has the added feature of characteristics that extend into the region of opposite polarity for V_{GS}.

Basic Construction

The basic construction of the *n*-channel depletion-type MOSFET is provided in Fig. 1.15. A slab of *p*-type material is formed from a silicon base and is referred to as the *substrate*. It is the foundation upon which the device will be constructed. In some cases the substrate is internally connected to the source terminal. However, many discrete devices provide an additional terminal labelled *SS*, resulting in a four-terminal device, such as that appearing in Fig. 1.15. The source and drain terminals are connected through metallic contacts to *n*-doped regions linked by an *n*-channel as shown in the figure. The gate is also connected to a metal contact surface but remains insulated from the *n*-channel by a very thin silicon dioxide (SiO_2) layer. SiO_2 is a particular type of insulator referred to as a *dielectric* that sets up opposing electric fields within the dielectric when exposed to an externally applied field.

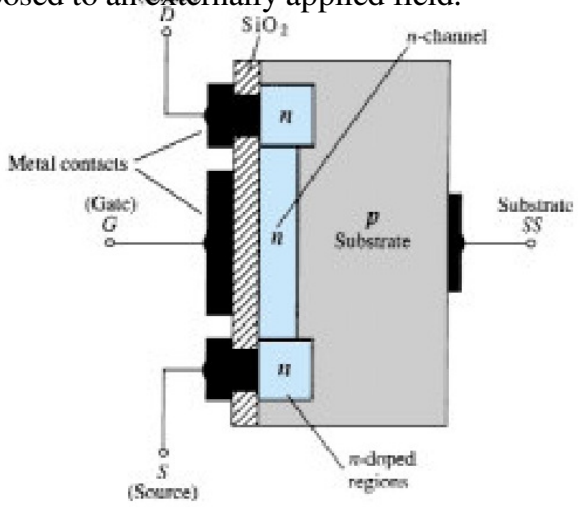


Fig 1.15 *n*-Channel depletion-type MOSFET

The fact that the SiO_2 layer is an insulating layer reveals the following fact: ***There is no direct electrical connection between the gate terminal and the channel of a MOSFET.***

In addition:

It is the insulating layer of SiO_2 in the MOSFET construction that accounts for the very desirable high input impedance of the device.

In fact, the input resistance of a MOSFET is often that of the typical JFET, even though the input impedance of most JFETs is sufficiently high for most applications. The very high input impedance continues to fully support the fact that the gate current (I_G) is essentially zero amperes for dc-biased configurations. The reason for the label metal-oxide-semiconductor FET is now fairly obvious: *metal* for the drain, source, and gate connections to the proper surface—in particular, the gate terminal and the control to be offered by the surface area of the contact, the *oxide* for the silicon dioxide insulating layer, and the *semiconductor* for the basic structure on which the *n*- and *p*-type regions are diffused. The insulating layer between the gate and channel has resulted in another name for the device: *insulated gate FET* or *IGFET,* although this label is used less and less in current literature.

Basic Operation and Characteristics

In Fig. 1.16 the gate-to-source voltage is set to zero volts by the direct connection from one terminal to the other, and a voltage V_{DS} is applied across the drain-to-source terminals. The result is an attraction for the positive potential at the drain by the *free* electrons of the *n*-channel and a current similar to that established through the channel of the JFET. In fact, the resulting current with *VGS* = 0 V continues to be labeled I_{DSS}, as shown in Fig. 1.17.

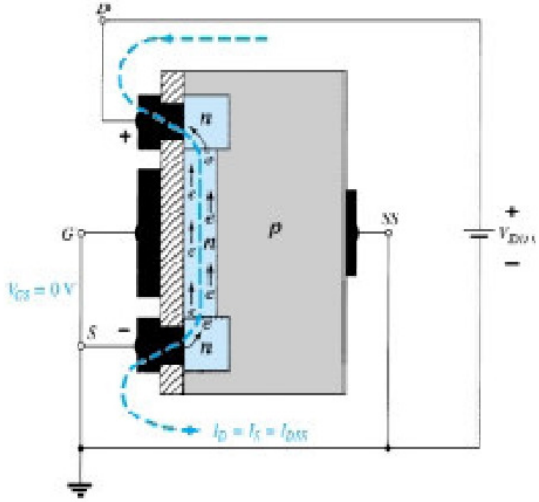


Fig 1.16 *n*-Channel depletion-type MOSFET with *VGS* = 0 V and an applied voltage V_{DD}

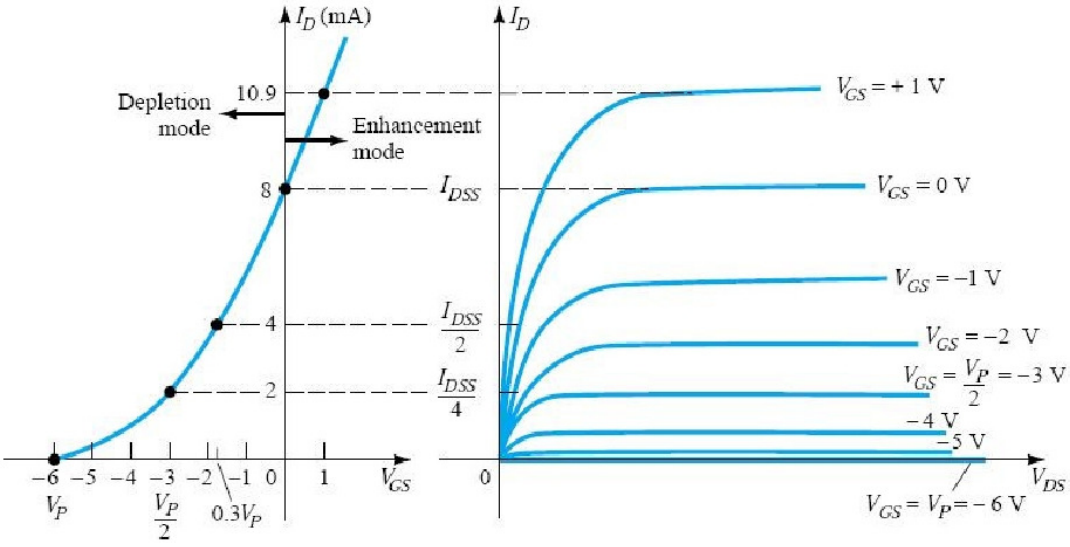


Fig 1.17 Drain and transfer characteristics for an *n*-channel depletion-type MOSFET

The region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region,* with the region between cut-off and the saturation level of I_{DSS} referred to as the *depletion region.* Shockley's equation is applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 1.15. There is an *n*-type substrate and a *p*-type channel, as shown in Fig. 1.18(a). The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 1.16 but with V_{DS} having negative values I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 1.18(c). The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 1.18(b). In other words, the drain current will increase from cut-off at $V_{GS} = V_P$ in the positive V_{GS} region to I_{DSS} and then continue to increase for increasingly negative values of V_{GS}. Shockley's equation is still applicable and requires simply placing the correct sign for both V_{GS} and V_P in the equation.

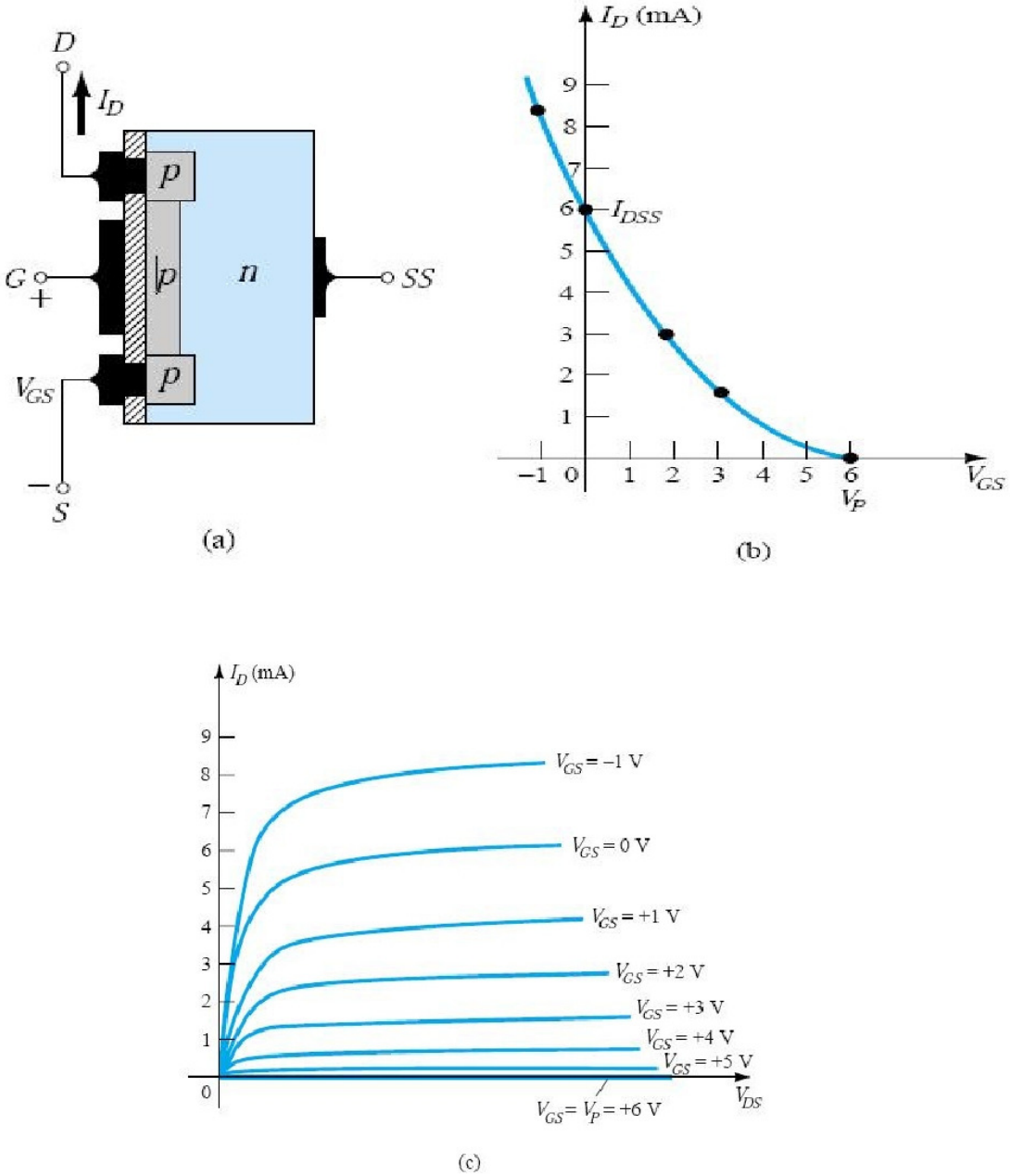


Fig 1.18 *p*-Channel depletion-type MOSFET with I_{DSS} = 6 mA and V_P = -6 V

Symbols

The graphic symbols for an *n*- and *p*-channel depletion-type MOSFET are provided in Fig. 1.19. The lack of a direct connection (due to the gate insulation) between the gate and channel is represented by a space between the gate and the other terminals of the symbol. The vertical line representing the channel is connected between the drain and source and is "supported" by the substrate. Two symbols are provided for each type of channel to reflect the fact that in some cases the substrate is externally available while in others it is not.

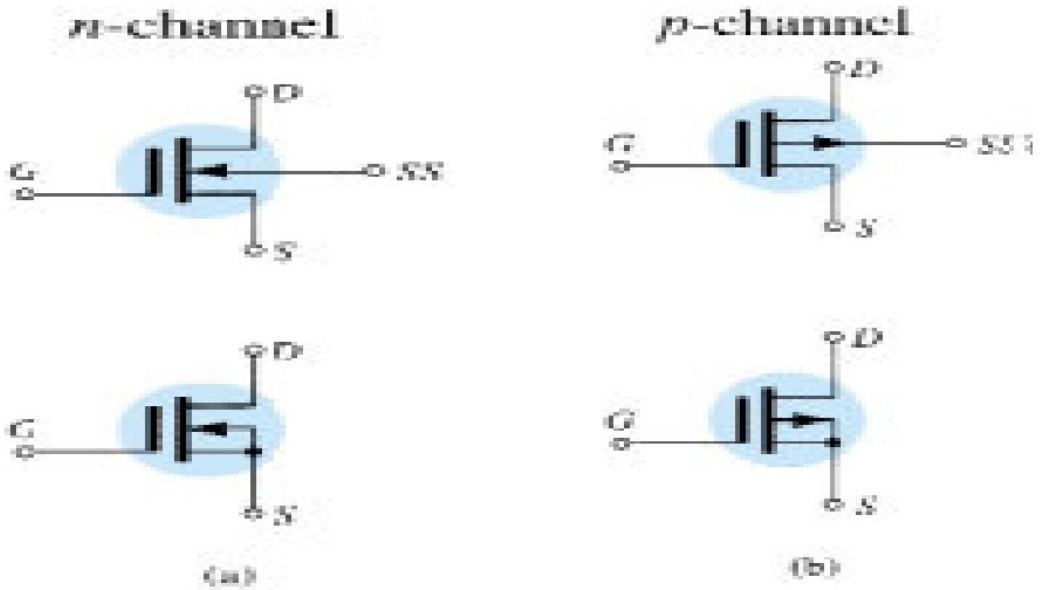


Fig 1.19 Graphic symbols for (a) *n*-channel depletion-type MOSFETs and (b) *p*- channel depletion-type MOSFETs

1.6 ENHANCEMENT-TYPE MOSFET

Although there are some similarities in construction and mode of operation between depletion-type and enhancement-type MOSFETs, the characteristics of the enhancement-type MOSFET are quite different from anything obtained thus far. The transfer curve is not defined by Shockley's equation, and the drain current is now cut off until the gate-to-source voltage reaches a specific magnitude. In particular, current control in an *n*-channel device is now effectedby a positive gate-to-source voltage rather than the range of negative voltages encountered for *n*-channel JFETs and *n*-channel depletion-type MOSFETs.

Basic Construction

The basic construction of the *n*-channel enhancement-type MOSFET is provided in Fig. 1.20. A slab of *p*-type material is formed from a silicon base and is again referred to as the substrate. As with the depletion-type MOSFET, the substrate is sometimes internally connected to the source terminal, while in other cases a fourth lead is made available for external control of its potential level. The source and drain terminals are again connected through metallic contacts to *n*-doped regions, but note in Fig. 1.20 the absence of a channel between the two *n*-doped regions. This is the primary difference between the construction of depletion-type and enhancement-type MOSFETs—the absence of a channel as a constructed component of the device. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the *p*-type material.

In summary, therefore, the *construction of an enhancement-type MOSFET is quite similar to that of the depletion-type MOSFET, except for the absence of a channel between the drain and source terminals.*

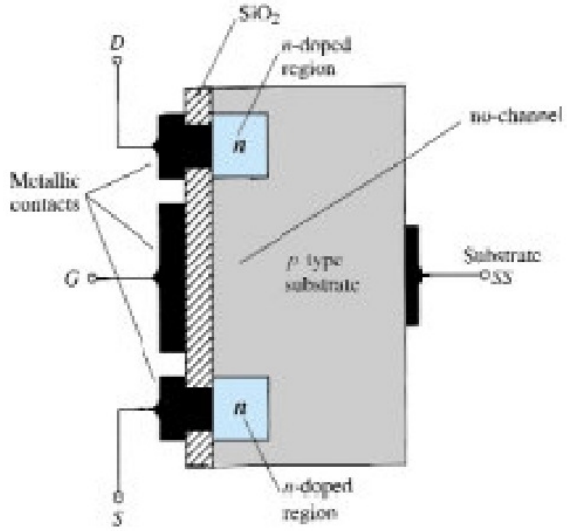


Fig 1.20 *n*-Channel enhancement-type MOSFET

Basic Operation and Characteristics

If V_{GS} is set at 0 V and a voltage applied between the drain and source of the device of Fig. 1.20, the absence of an *n*-channel (with its generous number of free carriers) will result in a current of effectively zero amperes—quite different from the depletion-type MOSFET and JFET where $I_D = I_{DSS}$. It is not sufficient to have a large accumulation of carriers (electrons) at the drain and source (due to the *n*-doped regions) if a path fails to exist between the two. With V_{DS} some positive voltage, V_{GS} at 0 V, and terminal *SS* directly connected to the source, there are in fact two reverse-biased *p*-*n* junctions between the *n*-doped regions and the *p*-substrate to oppose any significant flow between drain and source.
In Fig. 1.21 both V_{DS} and V_{GS} have been set at some positive voltage greater than 0 V, establishing the drain and gate at a positive potential with respect to the source. The positive potential at the gate will pressure the holes (since like charges repel) in the *p*-substrate along the edge of the SiO_2 layer to leave the area and enter deeper regions of the *p*-substrate, as shown in the figure. The result is a depletion region near the SiO_2 insulating layer void of holes. However, the electrons in the *p*-substrate (the minority carriers of the material) will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer. The SiO_2 layer and its insulating qualities will prevent the negative carriers from being absorbed at the gate terminal. As V_{GS} increases in magnitude, the concentration of electrons near the SiO_2 surface increases until eventually the induced *n*-type region can support a measurable flow between drain and source. The level of V_{GS} that results in the significant

increase in drain current is called the *threshold voltage* and is given the symbol V_T. On specification sheets it is referred to as $V_{GS(Th)}$, although V_T is less unwieldy and will be used in the analysis to follow. Since the channel is nonexistent with $V_{GS} = 0$ V and "enhanced" by the application of a positive gate-to-source voltage, this type of MOSFET is called an *enhancement-type MOSFET*. Both depletion- and enhancement-type MOSFETs have enhancement-type regions, but the label was applied to the latter since it is its only mode of operation.

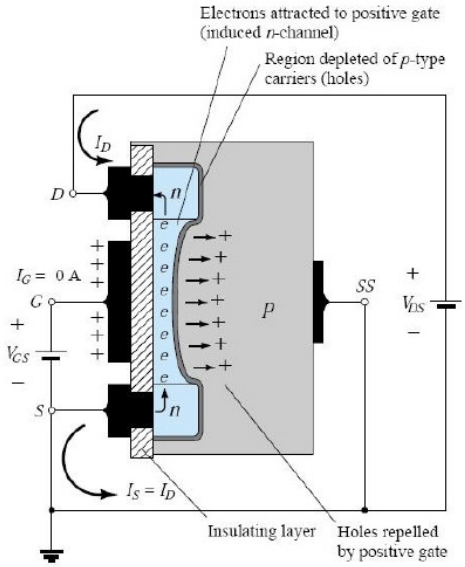


Fig 1.21 Channel formation in the *n*-channel enhancement-type MOSFET

As V_{GS} is increased beyond the threshold level, the density of free carriers in the induced channel will increase, resulting in an increased level of drain current. However, if we hold V_{GS} constant and increase the level of V_{DS}, the drain current will eventually reach a saturation level as occurred for the JFET and depletion-type MOSFET. The leveling off of I_D is due to a pinching-off process depicted by the narrower channel at the drain end of the induced channel as shown in Fig. 1.22. Applying Kirchhoff's voltage law to the terminal voltages of the MOSFET of Fig. 1.23, we find that

$$V_{DG} = V_{DS} - V_{GS} \text{---------- (1.9)}$$

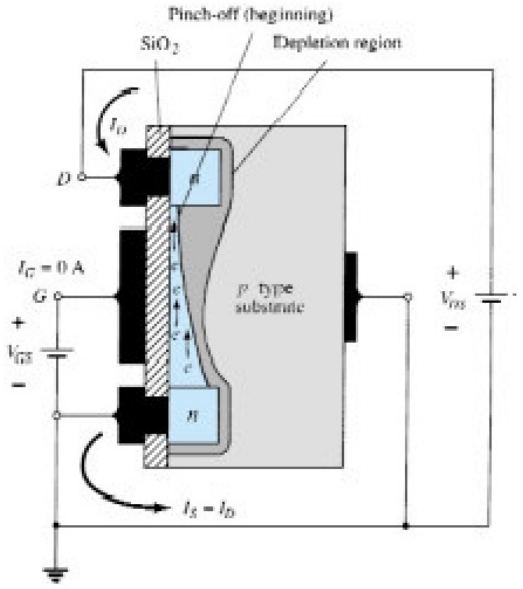


Fig 1.22 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

If V_{GS} is held fixed at some value such as 8 V and V_{DS} is increased from 2 to 5 V, the voltage V_{DG} [by Eq. (1.9)] will drop from -6 to -3 V and the gate will become less and less positive with respect to the drain. This reduction in gate-to-drain voltage will in turn reduce the attractive forces for free carriers (electrons) in this region of the induced channel, causing a reduction in the effective channel width. Eventually, the channel will be reduced to the point of pinch-off and a saturation condition will be established as described earlier for the JFET and depletion-type MOSFET.
In other words, any further increase in V_{DS} at the fixed value of V_{GS} will not affect the saturation level of I_D until breakdown conditions are encountered.
The drain characteristics of Fig. 1.23 reveal that for the device of Fig. 1.22 with $V_{GS} = 8$ V, saturation occurred at a level of $V_{DS} = 6$ V. In fact, the saturation level for V_{DS} is related to the level of applied V_{GS} by

$$\mathbf{V_{DSsat} = V_{GS} - V_T} \text{----------(1.10)}$$

Therefore, for a fixed value of V_T, then the higher the level of V_{GS}, the more the saturation level for V_{DS}, as shown in Fig. 1.22 by the locus of saturation levels. For the characteristics of Fig. 1.22 the level of V_T is 2 V, as revealed by the fact that the drain current has dropped to 0 mA.

In general, therefore:
For values of V_{GS} less than the threshold level, the drain current of an enhancement-type MOSFET is 0 mA.

Fig 1.23 clearly reveals that as the level of V_{GS} increased from V_T to 8 V, the resulting saturation level for I_D also increased from a level of 0 to 10 mA. In addition, it is quite noticeable that the spacing between the levels of V_{GS} increased as the magnitude of V_{GS} increased, resulting in ever-increasing increments in drain current.

For levels of $V_{GS} > V_T$, the drain current is related to the applied gate-to-source voltage by the following nonlinear relationship:

$$\mathbf{I_D = k(V_{GS} - V_T)} \text{ ----------(1.11)}$$

Again, it is the squared term that results in the nonlinear (curved) relationship between I_D and V_{GS}. The k term is a constant that is a function of the construction of the device. The value of k can be determined from the following equation [derived from Eq. (1.11)] where I_D(on) and V_{GS}(on) are the values for each at a particular point on the characteristics of the device.

$$\mathbf{k = I_D(on)/[V_{GS}(on) - V_T]} \text{ ----------(1.12)}$$

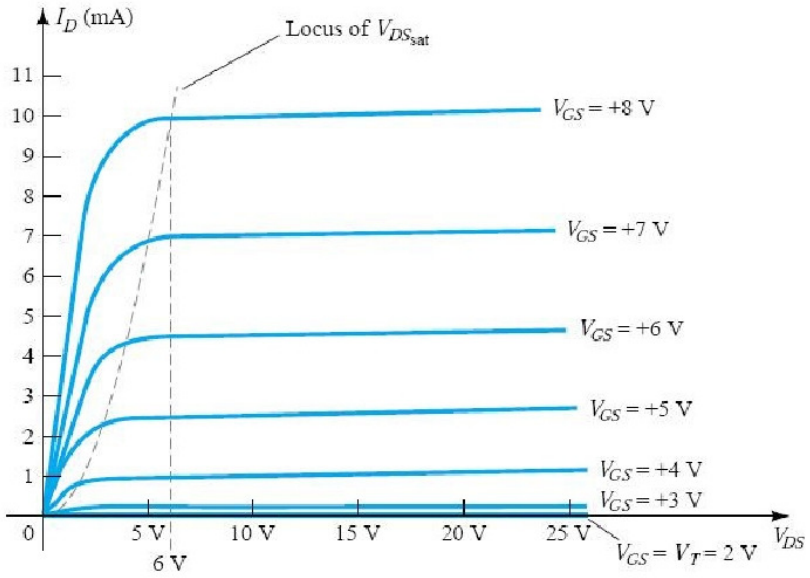


Fig 1.23 Drain characteristics of an *n*-channel enhancement-type MOSFET with V_T = 2 V and k = 0.278x10 A/V

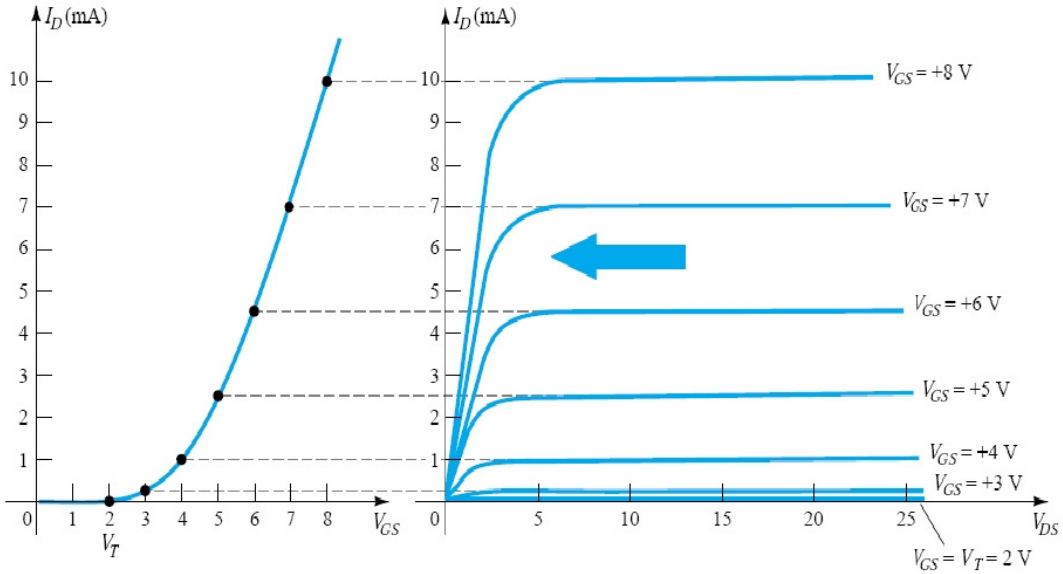
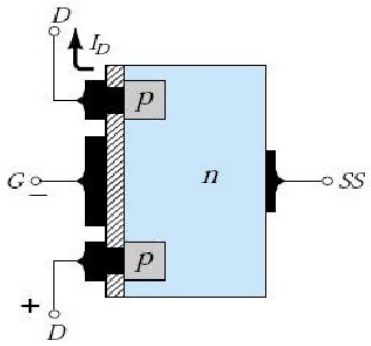


Fig 1.24 Transfer characteristics for an *n*-channel enhancement-type MOSFET from the drain characteristics

p-Channel Enhancement-Type MOSFETs

The construction of a *p*-channel enhancement-type MOSFET is exactly the reverse of that appearing in Fig. 1.20, as shown in Fig. 1.25(a). There is now an *n*-type substrate and *p*-doped regions under the drain and source connections. The terminals remain as identified, but all the voltage polarities and the current directions are reversed. The drain characteristics will appear as shown in Fig. 1.25(c), with increasing levels of current resulting from increasingly negative values of V_{GS}. The transfer characteristics will be the mirror image (about the I_D axis) of the transfer curve of Fig. 1.24, with I_D increasing with increasingly negative values of V_{GS} beyond V_T, as shown in Fig. 1.25(b). Equations (1.9) through (1.12) are equally applicable to *p*-channel devices.



(a)

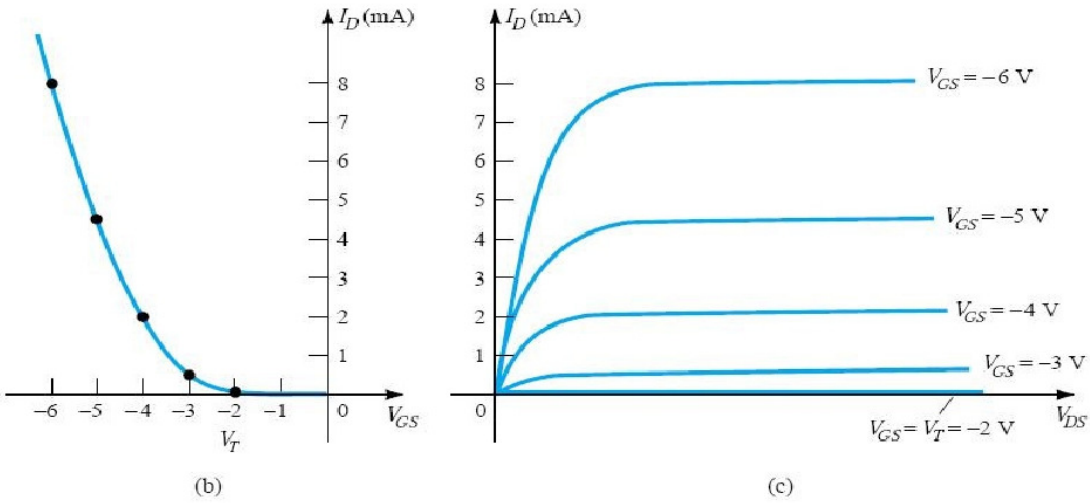


Fig 1.25 *p*-Channel enhancement-type MOSFET
with $V_T = 2$ V and $k = 0.5\text{x}10^3$ A/V^2

Symbols

The graphic symbols for the *n*- and *p*-channel enhancement-type MOSFETs are provided as Fig. 1.26. Again note how the symbols try to reflect the actual construction of the device. The dashed line between drain and source was chosen to reflect the fact that a channel does not exist between the two under no-bias conditions. It is, in fact, the only difference between the symbols for the depletion-type and enhancement-type MOSFETs.

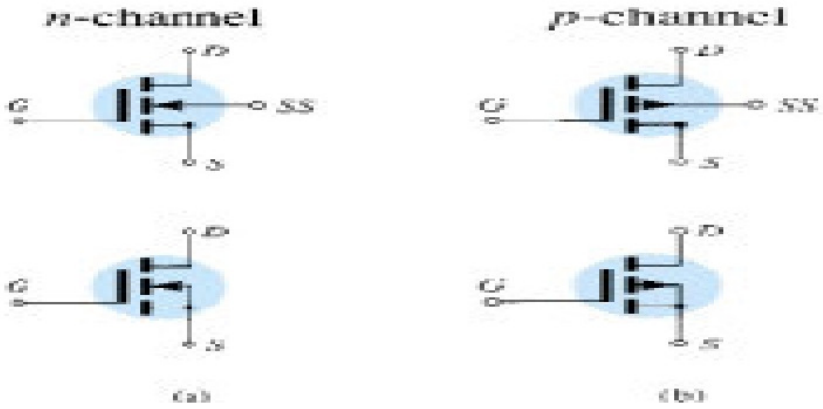


Fig 1.26 Symbols for (a) *n*-channel enhancement-type MOSFETs
(b) *p*-channel enhancement-type MOSFETs

Topic 2 BIASING OF BJT'S

2.1 INTRODUCTION

The analysis or design of a transistor amplifier requires knowledge of both the dc and ac response of the system. Too often it is assumed that the transistor is a magical device that can raise the level of the applied ac input without the assistance of an external energy source. In actuality, the improved output ac power level is the result of a transfer of energy from the applied dc supplies. The analysis or design of any electronic amplifier therefore has two components: the dc portion and the ac portion. Fortunately, the superposition theorem is applicable and the investigation of the dc conditions can be totally separated from the ac response. However, one must keep in mind that during the design or synthesis stage the choice of parameters for the required dc levels will affect the ac response, and vice versa.

The dc level of operation of a transistor is controlled by a number of factors, including the range of possible operating points on the device characteristics. Once the desired dc current and voltage levels have been defined, a network must be constructed that will establish the desired operating point. Each design will also determine the stability of the system, that is, how sensitive the system is to temperature variations.

Basic relationships for a transistor:

$$\mathbf{V_{BE} = 0.7V} \text{----------(2.1)}$$

$$\mathbf{I_E = (1+\beta)I_B = I_C} \text{----------(2.2)}$$

$$\mathbf{I_C = \beta I_B} \text{----------(2.3)}$$

In most instances the base current I_B is the first quantity to be determined. Once I_B is known, the relationships of Eqs. (2.1) through (2.3) can be applied to find the remaining quantities of interest.

2.2 OPERATING POINT

The term *biasing* appearing in the title of this chapter is an all-inclusive term for the application of dc voltages to establish a fixed level of current and voltage. For transistor amplifiers the resulting dc current and voltage establish an *operating point* on the characteristics that define the region that will be employed for amplification of the applied signal. Since the operating point is a fixed point on the characteristics, it is also called the *quiescent point* (abbreviated *Q*-point). By definition, *quiescent* means quiet, still, inactive. Figure 1.1 shows a general output device characteristic with four operating points indicated. The biasing circuit can be designed to set the device operation at any of these points or others within the *active region.* The maximum ratings are indicated on the characteristics of Fig. 1.1 by a horizontal line for the maximum collector current $I_{C\max}$ and a vertical line at the maximum collector-

to-emitter voltage V_{CE}max. The maximum power constraint is defined by the curve $P_{C\max}$ in the same figure. At the lower end of the scales is the cut-off region, defined by $I_B \leq 0\mu A$, and the *saturation region*, defined by $V_{CE} \leq V_{CE}$sat.

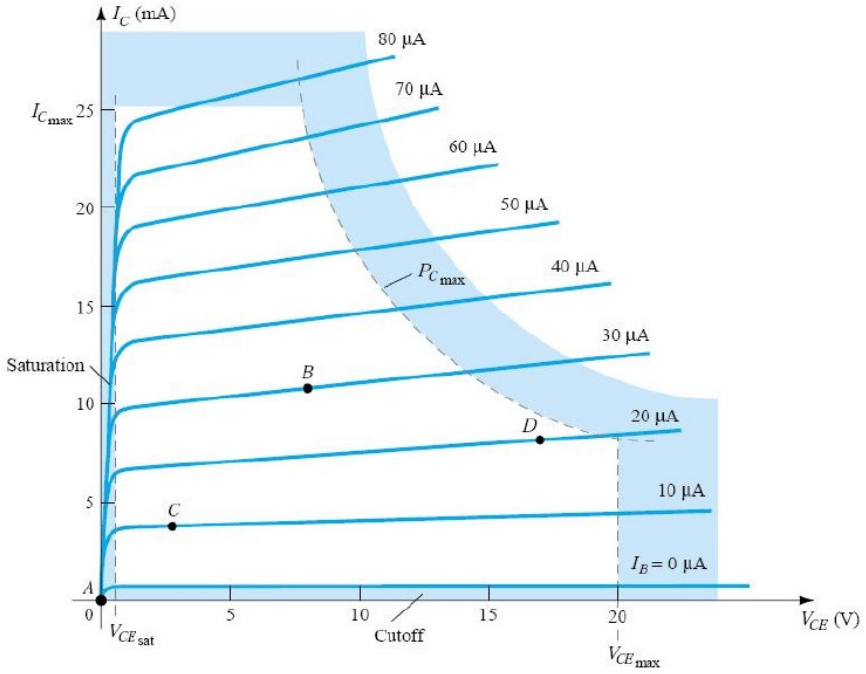


Fig 2.1 Various operating points within the limits of operation of a transistor

The BJT device could be biased to operate outside these maximum limits, but the result of such operation would be either a considerable shortening of the lifetime of the device or destruction of the device. Confining ourselves to the *active* region, one can select many different operating areas or points. The chosen *Q*-point often depends on the intended use of the circuit.

If no bias were used, the device would initially be completely off, resulting in a *Q*-point at *A*—namely, zero current through the device (and zero voltage across it). Since it is necessary to bias a device so that it can respond to the entire range of an input signal, point *A* would not be suitable. For point *B*, if a signal is applied to the circuit, the device will vary in current and voltage from operating point, allowing the device to react to (and possibly amplify) both the positive and negative excursions of the input signal. If the input signal is properly chosen, the voltage and current of the device will vary but not enough to drive the device into *cut-off* or *saturation*. Point *C* would allow some positive and negative variation of the output signal, but the peak-to-peak value would be limited by the proximity of $V_{CE} = 0\text{V}/I_C = 0$ mA. Operating at point *C* also raises some concern about the nonlinearities introduced by the fact that the spacing between I_B curves is rapidly changing in this region. In general, it is preferable

to operate where the gain of the device is fairly constant (or linear) to ensure that the amplification over the entire swing of input signal is the same. Point *B* is a region of more linear spacing and therefore more linear operation, as shown in Fig. 2.1. Point *D* sets the device operating point near the maximum voltage and power level. The output voltage swing in the positive direction is thus limited if the maximum voltage is not to be exceeded. Point *B* therefore seems the best operating point in terms of linear gain and largest possible voltage and current swing. This is usually the desired condition for small-signal amplifiers but not the case necessarily for power amplifiers.

One other very important biasing factor must be considered. Having selected and biased the BJT at a desired operating point, the effect of temperature must also be taken into account. Temperature causes the device parameters such as the transistor current gain (β_{ac}) and the transistor leakage current (I_{CEO}) to change. Higher temperatures result in increased leakage currents in the device, thereby changing the operating condition set by the biasing network. The result is that the network design must also provide a degree of *temperature stability* so that temperature changes result in minimum changes in the operating point. This maintenance of the operating point can be specified by a *stability factor*, *S*, which indicates the degree of change in operating point due to a temperature variation. A highly stable circuit is desirable, and the stability of a few basic bias circuits will be compared.

For the BJT to be biased in its linear or active operating region the following must be true:

1. The *base-emitter junction must be forward-biased* (*p*-region voltage more *p*ositive), with a resulting forward-bias voltage of about 0.6to 0.7 V.
2. The *base-collector junction must be reverse-biased* (*n*-region more *p*ositive), with the reverse-bias voltage being any value within the maximum limits of the device.

[Note that for forward bias the voltage across the *p-n* junction is *p-p*ositive, while for reverse bias it is opposite (reverse) with *n-p*ositive.]

Operation in the cut-off, saturation, and linear regions of the BJT characteristic are provided as follows:

1. *Linear-region operation:*
Base-emitter junction forward biased Base-collector junction reverse biased

2. *Cut-off-region operation:*
Base-emitter junction reverse biased

3. *Saturation-region operation:*
Base-emitter junction forward biased
Base-collector junction forward biased

2.3 FIXED-BIAS CIRCUIT

The fixed-bias circuit of Fig. 2.2 provides a relatively straightforward and simple introduction to transistor dc bias analysis. Even though the network employs an*npn* transistor, the equations and calculations apply equally well to a *pnp* transistor configuration merely by changing all current directions and voltage polarities. The current directions of Fig. 2.2 are the actual current directions, and the voltages are defined by the standard double-subscript notation. For the dc analysis the network can be isolated from the indicated ac levels by replacing the capacitors with an open circuit equivalent. In addition, the dc supply V_{CC} can be separated into two supplies (for analysis purposes only) as shown in Fig. 2.3 to permit a separation of input and output circuits. It also reduces the linkage between the two to the base current I_B. The separation is certainly valid, as we note in Fig. 2.3 that V_{CC} is connected directly to R_B and R_C just as in Fig. 2.2.

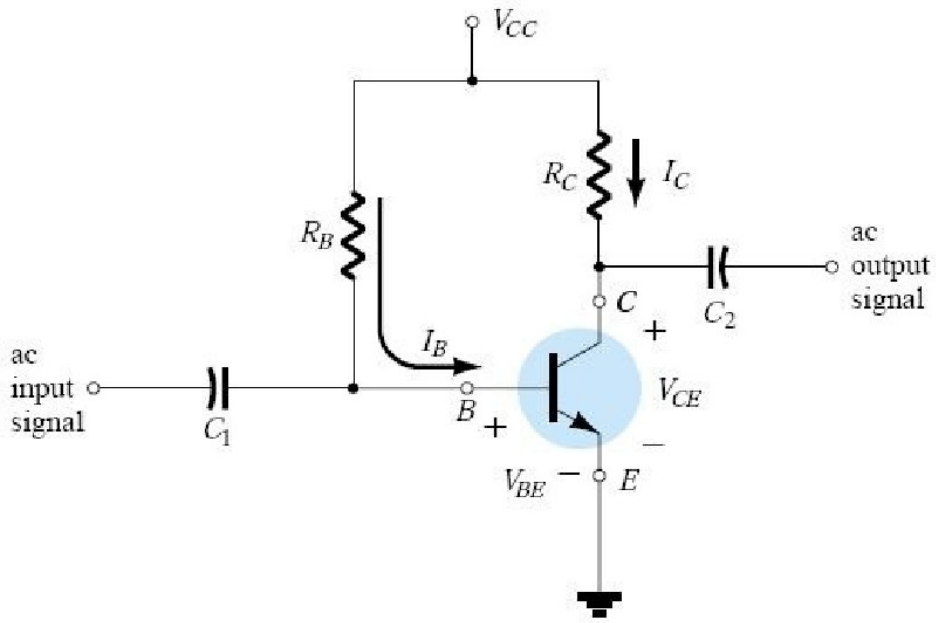


Fig 2.2 Fixed-bias circuit

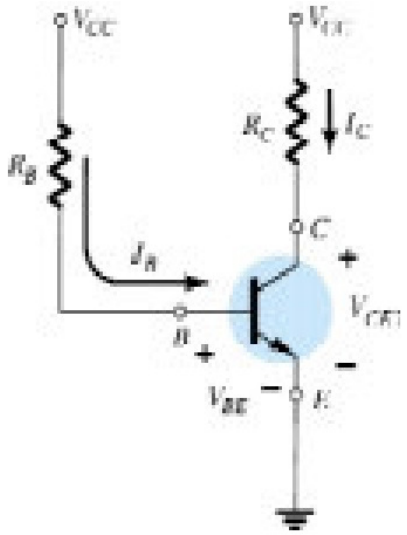


Fig 2.3 dc equivalent of Fig. 2.2

Base-Emitter Loop

Consider first the base-emitter circuit loop of Fig. 1.4. Writing Kirchhoff's voltage equation in the clockwise direction for the loop, we obtain

$+V_{CC} - I_B R_B - V_{BE} = 0$

Solving the equation for the current I_B will result in the following:

$$\mathbf{I_B = (V_{BE} - V_{CC})/R_B} \text{ ---------- (2.4)}$$

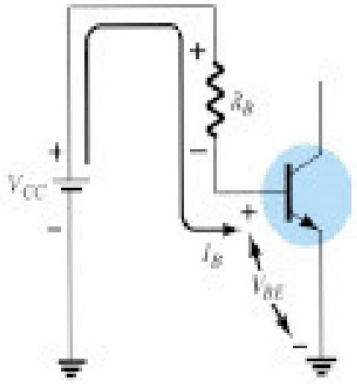


Fig 2.4 Base-emitter loop

Collector-Emitter Loop

Applying Kirchhoff's voltage law in the clockwise direction around the indicated collector - emitter closed loop of Fig. 2.5 will result in the following:

$V_{CE} + I_C R_C - V_{CC} = 0$

Solving the equation for the voltage V_{CE} will result in the following:

$$\mathbf{V_{CE} = V_{CC} - I_C R_C} \text{----------(2.5)}$$

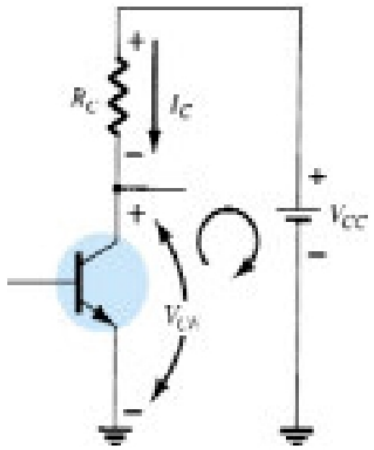


Fig 2.5 Collector-emitter loop

Keep in mind, $\mathbf{I_C = \beta I_B, V_{CE} = V_C - V_E, V_{BE} = V_B - V_E}$

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. For a transistor operating in the saturation region, the current is a maximum value *for the particular design.* Change the design and the corresponding saturation level may rise or drop. Of course, *the highest saturation level is defined by the maximum collector current as provided by the specification sheet.*
Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted.

The resulting saturation current for the fixed-bias configuration is

$$\mathbf{I_{Csat} = V_{CC}/R_C} \text{ ---------- (2.6)}$$

Once I_{Csat} is known, we have some idea of the maximum possible collector current for the chosen design and the level to stay below if we expect linear amplification.

Load-Line Analysis

The network of Fig. 2.6(a) establishes an output equation that relates the variables I_C and V_{CE} in the following manner:
$V_{CE} = V_{CC} - I_C R_C$----------(2.7)

The output characteristics of the transistor also relate the same two variables I_C and V_{CE} as shown in Fig. 2.6(b).

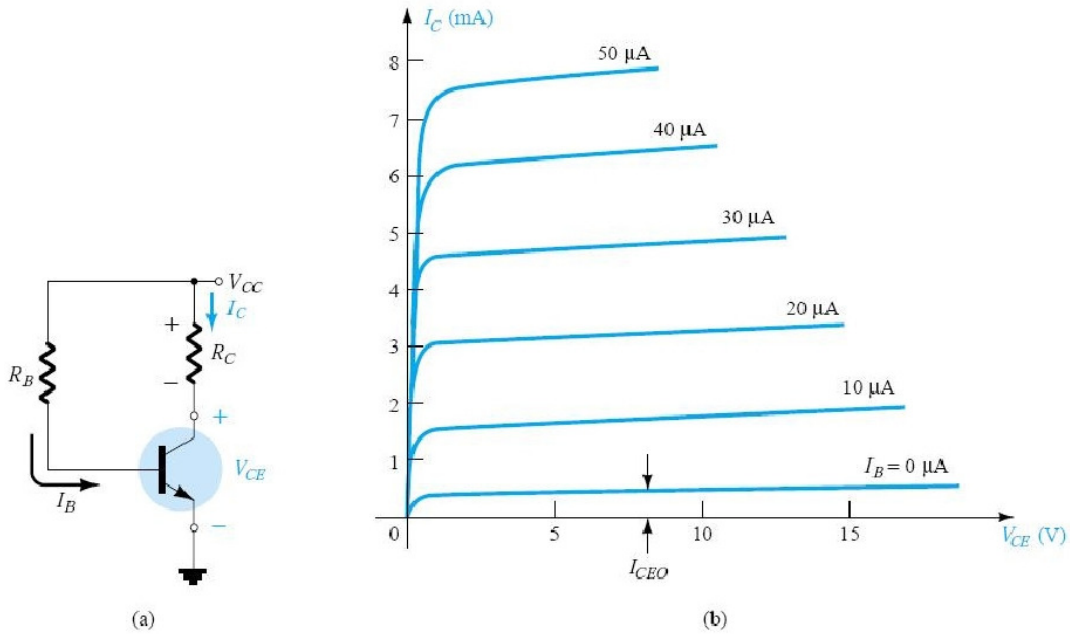


Fig 2.6 Load-line analysis: (a) the network; (b) the device characteristics

The common solution of the two occurs where the constraints established by each are satisfied simultaneously. In other words, this is similar to finding the solution of two simultaneous equations: one established by the network and the other by the device characteristics.
The device characteristics of I_C versus V_{CE} are provided in Fig. 2.6(b). We must now superimpose the straight line defined by Eq. (2.7) on the characteristics.
The most direct method of plotting Eq. (2.7) on the output characteristics is to use the fact that a straight line is defined by two points.

$$\mathbf{V_{CE} = V_{CC} | I_C = 0mA} \text{----------(2.8)}$$

$$\mathbf{I_C = (V_{CC}/R_C) | V_{CE} = 0V} \text{ ----------(2.9)}$$

By joining the two points defined by Eqs. (2.8) and (2.9), the straight line established by Eq. (2.8) can be drawn. The resulting line on the graph of Fig. 2.7 is called the *load line* since it is defined by the load resistor R_C. By solving for the resulting level of I_B, the actual Q-point can be established as shown in Fig. 2.7.

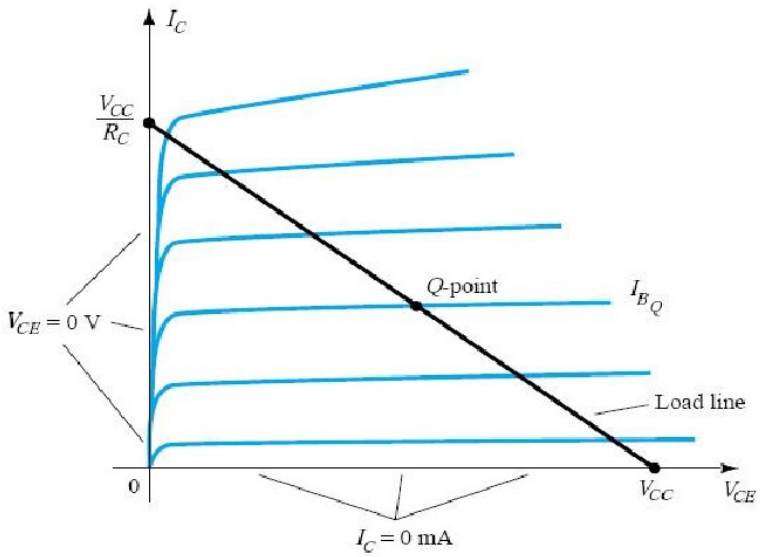


Fig 2.7 Fixed-bias load line

2.4 EMITTER-STABILIZED BIAS CIRCUIT

The dc bias network of Fig. 2.8 contains an emitter resistor to improve the stability level over that of the fixed-bias configuration.

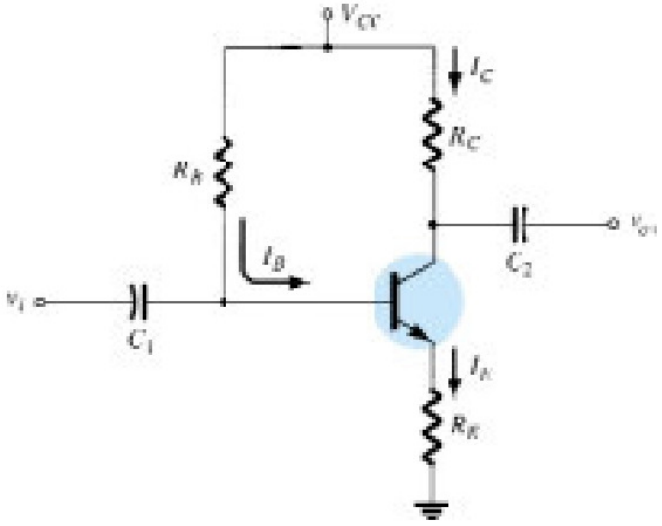


Fig 2.8 BJT bias circuit with emitter resistor

Base-Emitter Loop

The base-emitter loop of the network of Fig. 2.8 can be redrawn as shown in Fig.2.9. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in the following equation:

$+V_{CC} - I_BR_B - V_{BE} - I_ER_E = 0$ ----------(2.10)

Substituting for $I_E = (1+\beta)I_B$ in Eq. (2.10) and solving for I_B gives,

$$\mathbf{I_B = (V_{CC} - V_{BE})/[R_B + (1+\beta)R_E]} \text{ ----------(2.11)}$$

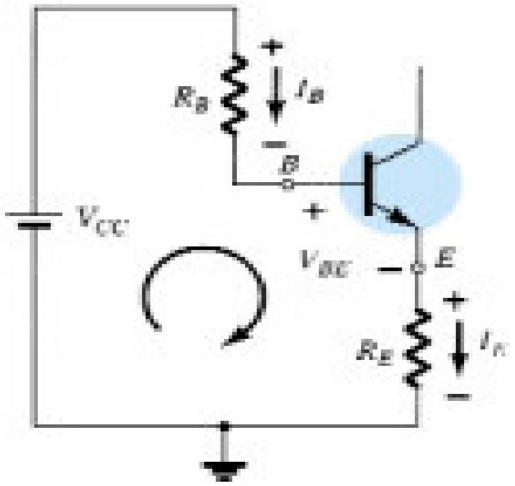


Fig 2.9 Base-emitter loop

***Note that**: The only difference between this equation for I_B and that obtained for the fixed-bias configuration is the term $(1+\beta)R_E$.*

Collector-Emitter Loop

The collector-emitter loop is redrawn. Writing Kirchhoff's voltage law for the indicated loop in the clockwise direction will result in:

$+I_ER_E + V_{CE} + I_CR_C - V_{CC} = 0$ ----------(2.11)

Substituting $I_E = I_C$ and grouping terms gives,

$$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)} \text{ ----------(2.12)}$$

Keep in mind,

$\mathbf{V_E = I_ER_E}$

$\mathbf{V_C = V_{CE} + V_E = V_{CC} - I_CR_C\ V_B =}$

$\mathbf{V_{BE} + V_E = V_{CC} - I_BR_B}$

Improved Bias Stability

The *addition of the emitter resistor to the dc bias of the BJT provides improved stability*, that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change.

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration:

$$\mathbf{I_{Csat} = V_{CC}/(R_C + R_E)} \text{----------(2.13)}$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration.
The collector-emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \text{ ----------(2.14)}$$

The most direct method of plotting Eq. (2.14) on the output characteristics is to use the fact that a straight line is defined by two points.

$$\mathbf{V_{CE} = V_{CC}|I_C = 0mA} \text{----------(2.15)}$$

$$\mathbf{I_C = V_{CC}/(R_C + R_E)|V_E = 0V} \text{ ----------(2.16)}$$

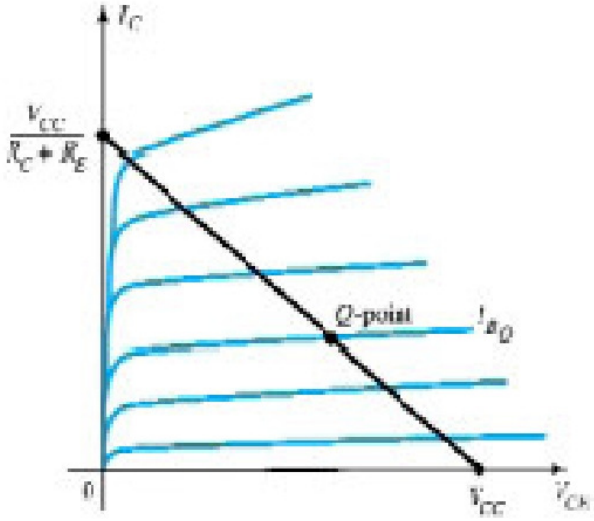


Fig 2.10 Load line for the emitter-bias configuration

2.5 VOLTAGE-DIVIDER BIAS

In the previous bias configurations the bias current I_{CQ} and voltage V_{CEQ} were a function of the current gain (β) of the transistor. However, since β is temperature sensitive, especially for silicon transistors, and the actual value of beta is usually not well defined, it would be desirable to develop a bias circuit that is less dependent, or in fact, independent of the transistor beta. The voltage-divider bias configuration of Fig. 2.11 is such a network. If analyzed on an exact basis the sensitivity to changes in beta is quite small. If the circuit parameters are properly chosen, the resulting levels of I_{CQ} and V_{CEQ} can be almost totally independent of beta.

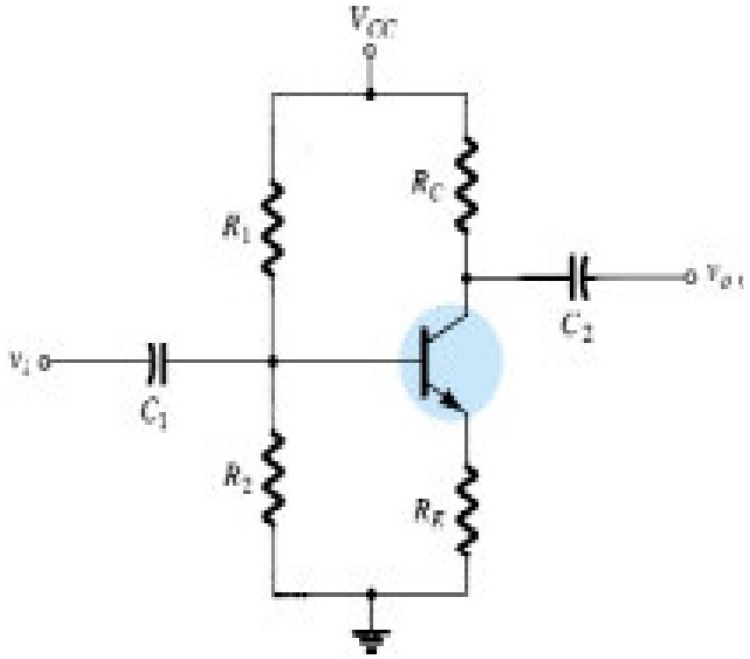


Fig 2.11 Voltage-divider bias configuration

There are two methods that can be applied to analyze the voltage-divider configuration. The first to be demonstrated is the *exact method* that can be applied to *any* voltage-divider configuration. The second is referred to as the *approximate method* and can be applied only if specific conditions are satisfied. The approximate approach permits a more direct analysis with a savings in time and energy.

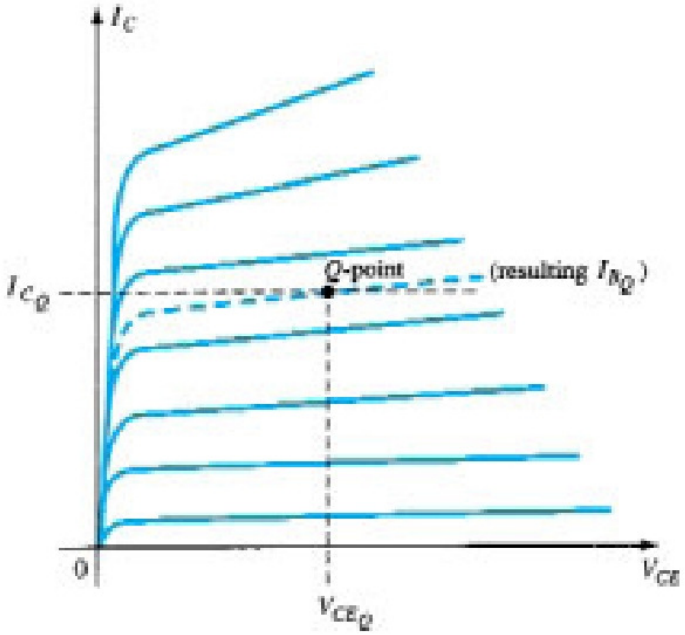


Fig 2.12 Defining the *Q*-point for the voltage-divider bias configuration

Exact Analysis

The input side of the network of Fig. 2.11 can be redrawn as shown in Fig. 2.13 for the dc analysis. The Thévenin equivalent network for the network to the left of the base terminal can then be found in the following manner:

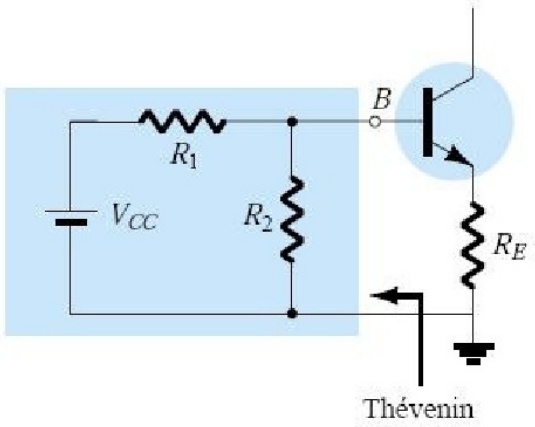


Fig 2.13 Redrawing the input side of the network of Fig. 2.11

$R_{th} = R_1 \| R_2$----------(2.17)

$E_{th} = V_{R2} = V_{CC}R_2/(R_1+R_2)$ ----------(2.18)

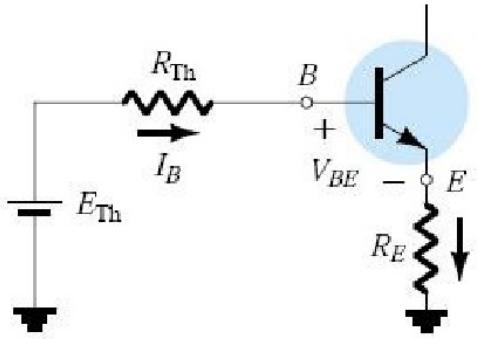


Fig 2.14 Inserting the Thévenin equivalent circuit

The Thévenin network is then redrawn as shown in Fig. 2.14, and I_{BQ} can be determined by first applying Kirchhoff's voltage law in the clockwise direction for the loop indicated:

$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$

i.e. $\mathbf{I_B = (E_{Th} - V_{BE})/R_{Th} + (1+\beta)R_E}$ --------(2.19)

Solving for V_{CE} in the collector-emitter loop,

$\mathbf{V_{CE} = V_{CC} - I_C(R_C+R_E)}$----------(2.20)

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 2.15. The resistanceR_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_E. The reflected resistance between base and emitter is defined by $R_i = (\beta+1)R_E$. IfR_i is much larger than the resistance R_2, the current I_B will be much smaller than I_2 (current always seeks the path of least resistance) and I_2 will be approximately equal to I_1. If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2, then $I_1 = I_2$ and R_1 and R_2 can be considered series elements.

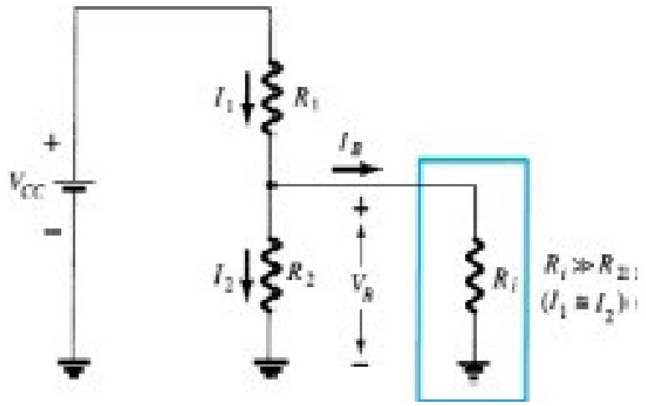


Fig 2.15 Partial-bias circuit for calculating the approximate base voltage V_B

The voltage across R_2, which is actually the base voltage, can be determined using the voltage-divider rule.

$$\mathbf{V_B = V_{CC}R_2/(R_1+R_2)} \text{----------(2.21)}$$

Since$Ri = (\beta+ 1)R_E = \beta R_E$ the condition that will define whether the approximate approach can be applied will be the following:

$$\mathbf{\beta R_E \geq 10R_2} \text{----------(2.22)}$$

In other words, if β times the value of R_E is at least 10 times the value of R_2, the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined,

$$\mathbf{V_E = V_B - V_{BE}} \text{----------(2.23)} \quad \mathbf{I_E}$$
$$\mathbf{= V_E/R_E} \text{----------(2.24)} \quad \mathbf{I_{CQ}}$$
$$\mathbf{= I_E} \text{----------(2.25)} \quad \mathbf{V_{CEQ}}$$
$$\mathbf{= V_{CC} - I_C(R_C+R_E)} \text{----------(2.26)}$$

Note in the sequence of calculations from Eq. (2.21) through Eq. (2.26) that β does not appear and I_B was not calculated. The Q-point (as determined by I_{CQ} and V_{CEQ}) is therefore independent of the value of β.

Transistor Saturation

The output collector-emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 2.4. The resulting equation for the saturation current is therefore the same as obtained for the emitter-biased configuration. That is,

$$\mathbf{I_{Csat} = I_{Cmax} = V_{CC}/(R_C + R_E)} \text{----------(2.28)}$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration.

$$\mathbf{I_C = V_{CC}/(R_C+R_E)|V_{CE}=0V} \text{----------(2.29)}$$
$$\mathbf{V_{CE} = V_{CC}|I_C=0mA} \text{----------(2.30)}$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

2.6 DC BIAS WITH VOLTAGE FEEDBACK

An improved level of stability can also be obtained by introducing a feedback path from collector to base as shown in Fig. 1.16. Although the *Q*-point is not totally independent of beta (even under approximate conditions), the sensitivity to changes in beta or temperature variations is normally less than encountered for the fixed-bias or emitter-biased configurations.

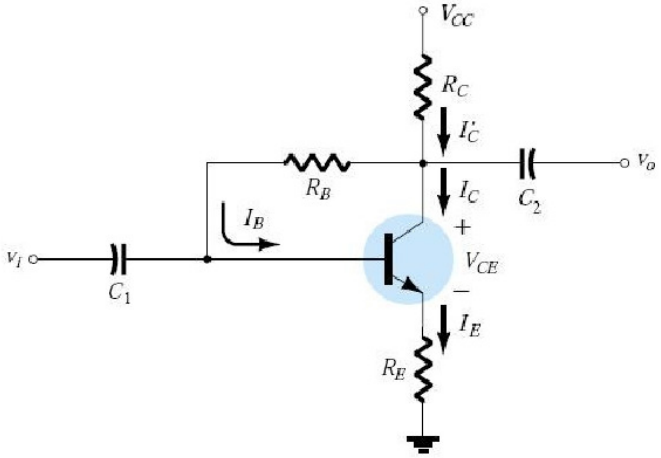


Fig 2.16 dc bias circuit with voltage feedback

Base-Emitter Loop

Fig 2.17 shows the base-emitter loop for the voltage feedback configuration. Writing Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$V_{CC} - I_{C'}R_C - I_BR_B - V_{BE} - I_ER_E = 0$

Putting $I_{C'} = \beta I_B$ and solving for I_B gives,

$$\mathbf{I_B = (V_{CC} - V_{BE})/[R_B + \beta(R_C+R_E)]} \text{ ----------(2.31)}$$

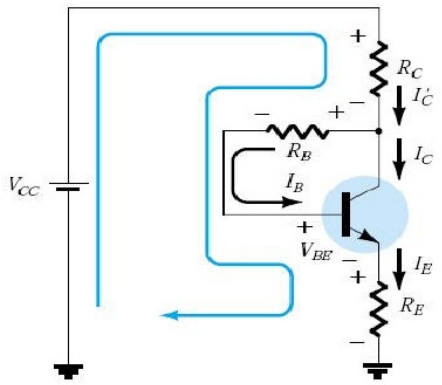


Fig 2.17 Base-emitter loop for the network of Fig. 2.16

Collector-Emitter Loop

The collector-emitter loop for the network of Fig. 2.16 is provided in Fig. 2.18. Applying Kirchhoff's voltage law around the indicated loop in the clockwise direction will result in

$I_E R_E + V_{CE} + I_C R_C - V_{CC} = 0$

Since $I_{C'} = I_C = I_E$ and solving for V_{CE} gives,

$$\mathbf{V_{CE} = V_{CC} - I_C(R_C + R_E)} \text{ ----------(2.32)}$$

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

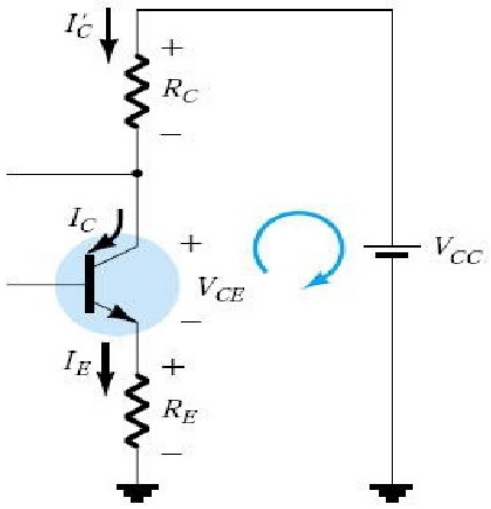


Fig 2.18 Collector-emitter loop for the network of Fig. 2.16

Saturation Conditions

Using the approximation $I'_C = I_C$, the equation for the saturation current is the same as obtained for the voltage-divider and emitter-bias configurations. That is,

$$\mathbf{I_{Csat} = I_{Cmax} = V_{CC}/(R_C + R_E)} \text{ ----------(2.33)}$$

Load-Line Analysis

Continuing with the approximation $I'_C = I_C$ will result in the same load line defined for the voltage-divider and emitter-biased configurations. The level of I_{BQ} will be defined by the chosen bias configuration.

2.7 BIAS STABILIZATION

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_C is sensitive to each of the following parameters:

β: increases with increase in temperature
$|V_{BE}|$: decreases about 7.5 mV per degree Celsius (°C) increase in temperature
I_{CO} (reverse saturation current): doubles in value for every 10°C increase in Temperature

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$

A stability factor, *S*, is defined for each of the parameters affecting bias stability as listed below:

$$\mathbf{S(I_{CO}) = \Delta I_C/\Delta I_{CO}} \text{ ----------(2.34)}$$

$$\mathbf{S(V_{BE}) = \Delta I_C/\Delta V_{BE}} \text{ ----------(2.35)}$$

$$\mathbf{S(\beta) = \Delta I_C/\beta} \text{ ----------(2.36)}$$

In each case, the delta symbol (Δ) signifies change in that quantity. The numerator of each equation is the change in collector current as established by the change in the quantity in the denominator. For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C/\Delta I_{CO}$ will be quite small. In other words:
Networks that are quite stable and relatively insensitive to temperature variations have low stability factors.
The higher the stability factor, the more sensitive the network to variations in that parameter.

$S(I_{CO})$: EMITTER-BIAS CONFIGURATION

For the emitter-bias configuration, an analysis of the network will result in

$$\mathbf{S(I_{CO}) = (1+\beta)[(1+ R_B/R_E) / \{(\beta+1) + R_B/R_E\}]} \text{ ----------(2.37)}$$

For $R_B/R_E >> (\beta+1)$, Eq. (1.37) will reduce to the following:

$$\mathbf{S(I_{CO}) = (1+\beta)} \text{ ----------(2.38)}$$

For $R_B/R_E << 1$,

$$\mathbf{S(I_{CO}) = 1} \text{ ----------(2.39)}$$

For the range where R_B/R_E ranges between 1 and (β+1),

$$\mathbf{S(I_{CO}) = R_B/R_E} \text{ ----------(2.40)}$$

The results reveal that the emitter-bias configuration is quite stable when the ratio R_B/R_E is as small as possible and the least stable when the same ratio approaches (β+1).

Fixed-Bias Configuration

$$\mathbf{S(I_{CO}) = (\beta+1)} \text{ ----------(2.41)}$$

The result is a configuration with a poor stability factor and a high sensitivity to variations in I_{CO}.

Voltage-Divider Bias Configuration

$$\mathbf{S(ICO) = (1+\beta)[(1+ R_{Th}/R_E) / \{(\beta+1) + R_{Th}/R_E\}]} \text{ ----------(2.42)}$$

Feedback-Bias Configuration

$$\mathbf{S(I_{CO}) = (1+\beta)[(1+ R_B/R_C) / \{(\beta+1) + R_B/R_C\}]} \text{ ----------(2.43)}$$

$S(V_{BE})$: EMITTER-BIAS CONFIGURATION

$$\mathbf{S(V_{BE}) = -\beta/[R_B + (1+\beta)R_E] = -(\beta/R_E)/[(R_B/R_E) + (1+\beta)]} \text{ ----------(2.44)}$$

Fixed-Bias Configuration ($R_E = 0\Omega$)

$$\mathbf{S(V_{BE}) = -\beta/R_B} \text{ ----------(2.45)}$$

For (1+β) >> RB/RE,

$$\mathbf{S(V_{BE}) = -1/R_E} \text{ ----------(2.46)}$$

revealing that the larger the resistance R_E, the lower the stability factor and the more stable the system.

S(β): EMITTER-BIAS CONFIGURATION

$$\mathbf{S(\beta) = [I_{C1}(1+R_B/R_E) / \{\beta_1(1+\beta_2+R_B/R_E)\}]} \text{ ----------(2.46)}$$

The notation I_{C_1} and β1 is used to define their values under one set of network conditions, while the notation β2 is used to define the new value of beta as established by such causes as temperature change, variation in β for the same transistor, or a change in transistors.

Fixed-Bias Configuration($R_E = 0\Omega$)

$$\mathbf{S(\beta) = [I_{C1}(R_B + R_C) / \beta_1\{R_B + R_C (1+\beta_2)\}]} \text{ ----------(2.47)}$$

Summary

Now that the three stability factors of importance have been introduced, the total effect on the collector current can be determined using the following equation:

$$\mathbf{\Delta I_C = S(I_{CO})\Delta I_{CO} + S(V_{BE})\Delta V_{BE} + S(\beta)\Delta\beta} \text{ ----------(2.48)}$$

The equation may initially appear quite complex, but take note that each component is simply a stability factor for the configuration multiplied by the resulting change in a parameter between the temperature limits of interest. In addition, the ΔI_C to be determined is simply the change in *IC* from the level at room temperature.

For instance, if we examine the fixed-bias configuration, Eq. (2.48) becomes the following:

$$\Delta I_C = (\beta+1)\Delta I_{CO} + (-\beta/R_B)\Delta V_{BE} + (I_{C1}/\beta_1)\Delta\beta$$

The effect of$S(I_{CO})$ in the design process is becoming a lesser concern because of improved manufacturing techniques that continue to lower the level of $I_{CO} = I_{CBO}$. It should also be mentioned that for a particular transistor the variation in levels of I_{CBO} and V_{BE} from one transistor to another in a lot is almost negligible compared to the variation in beta. In addition, the results of the analysis above support the fact that for a good stabilized design:

The ratio R_B/R_E or R_{Th}/R_E should be as small as possible with due consideration to all aspects of the design, including the ac response.

Topic 3 BIASING OF FETS AND MOSFETS

3.1 INTRODUCTION

For the *field-effect transistor (FET*), the relationship between input and output quantities is *nonlinear* due to the squared term in Shockley's equation. Linear relationships result in straight lines when plotted on a graph of one variable versus the other, while non-linear functions result in curves as obtained for the transfer characteristics of a JFET. The non-linear relationship between I_D and V_{GS} can complicate the mathematical approach to the dc analysis of FET configurations. A graphical approach may limit solutions to tenths-place accuracy, but it is a quicker method for most FET amplifiers.
Whereas in *bipolar junction transistor (BJT*), the biasing level can be obtained using the characteristic equations $V_{BE} = 0.7V$, $I_C = \beta I_B$, and $I_C = I_E$. The linkage between input and output variables is provided by β, which is assumed to be fixed in magnitude for the analysis to be performed. The fact that beta is a constant establishes a *linear* relationship between I_C and I_B. Doubling the value of I_B will double the level of I_C, and so on.

Another distinct difference between the analysis of BJT and FET transistors is that the input controlling variable for a BJT transistor is a current level, while for the FET a voltage is the controlling variable. In both cases, however, the controlled variable on the output side is a current level that also defines the important voltage levels of the output circuit.

The general relationships that can be applied to the dc analysis of all FET amplifiers are:

$$\mathbf{I_G = 0A} \text{----------(3.1)}$$
$$\mathbf{I_D = I_S} \text{----------(3.2)}$$

For JFETS and depletion-type MOSFETs, Shockley's equation is applied to relate the input and output quantities:

$$\mathbf{I_D = I_{DSS}(1-V_{GS}/V_P)^2} \text{ ----------(3.3)}$$

For enhancement-type MOSFETs, the following equation is applicable:

$$\mathbf{I_D = k(V_{GS} - V_T)^2} \text{ ----------(3.4)}$$

3.2 FIXED-BIAS CONFIGURATION

The simplest of biasing arrangements for the *n*-channel JFET appears in Fig. 3.1. The fixed-bias configuration is one of the few FET configurations that can be solved just as directly using either a mathematical or graphical approach.
The configuration of Fig. 3.1 includes the ac levels V_i and V_o and the coupling capacitors (C_1 and C_2). The coupling capacitors are "open circuits" for the dc analysis and low impedances (essentially short circuits) for the ac analysis. The resistor R_G is present to ensure that V_i appears at the input to the FET amplifier for the ac analysis.
For the dc analysis,
$I_G = 0A$ and $V_{RG} = I_G R_G = (0A)R_G = 0V$

The zero-volt drop across R_G permits replacing R_G by a short-circuit equivalent, as appearing in the network of Fig. 3.2 specifically redrawn for the dc analysis.

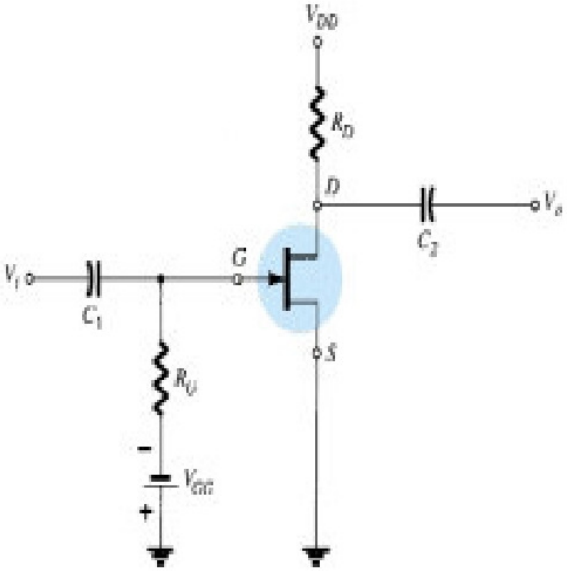


Fig 3.1 Fixed-bias configuration

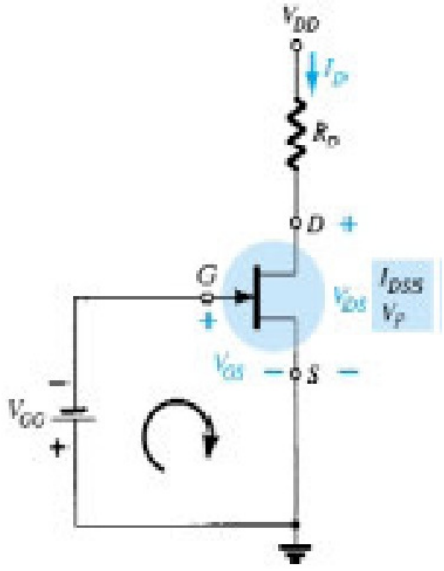


Fig 3.2 Network for dc analysis

The fact that the negative terminal of the battery is connected directly to the defined positive potential of V_{GS} clearly reveals that the polarity of V_{GS} is directly opposite to that of V_{GG}. Applying Kirchhoff's voltage law in the clockwise direction of the indicated loop of Fig. 3.2 will result in:

$$\mathbf{V_{GS} = -V_{GG}} \text{----------(3.5)}$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, resulting in the notation "fixed-bias configuration."

The resulting level of drain current I_D is now controlled by Shockley's equation:
$I_D = I_{DSS}(1-V_{GS}/V_P)^2$
Since V_{GS} is a fixed quantity for this configuration, its magnitude and sign can simply be substituted into Shockley's equation and the resulting level of I_D calculated.

A graphical analysis would require a plot of Shockley's equation as shown in Fig. 3.3. Choosing $V_{GS}= V_P/2$ will result in a drain current of $I_{DSS}/4$ when plotting the equation. For the analysis of this chapter, the three points defined by I_{DSS}, V_P, and the intersection just described will be sufficient for plotting the curve.

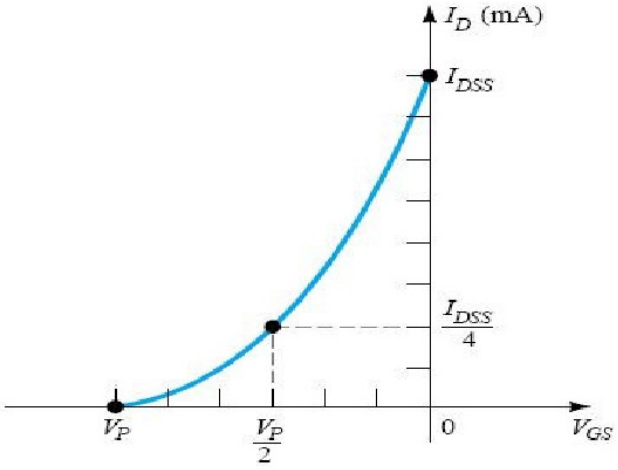


Fig 3.3 Plotting Shockley's equation

In Fig. 3.4, the fixed level of V_{GS} has been superimposed as a vertical line at $V_{GS} = -V_{GG}$. At any point on the vertical line, the level of V_{GS} is $-V_{GG}$—the level of I_D must simply be determined on this vertical line. The point where the two curves intersect is the common solution to the configuration—commonly referred to as the *quiescent* or *operating point or Q-point.*

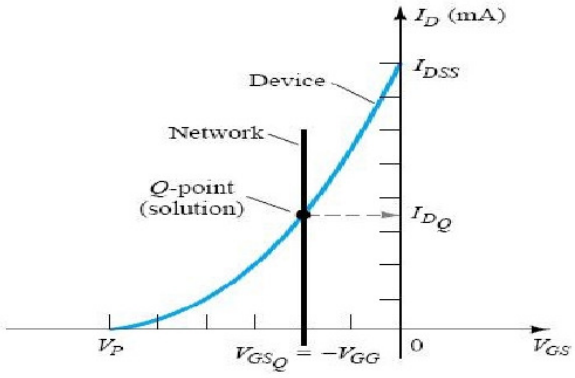


Fig 3.4 Finding the solution for the fixed-bias configuration

The drain-to-source voltage of the output section can be determined by applying Kirchhoff's voltage law as follows:

$+V_{DS} + I_D R_D - V_{DD} = 0$

Or, $\mathbf{V_{DS} = V_{DD} - I_D R_D}$----------(3.6)

Keep in mind, $\mathbf{V_S = 0V}$----------(3.7)

$\mathbf{V_D = V_{DS}}$----------(3.8) $\mathbf{V_G = V_{GS}}$ ----------(3.9)

Since the configuration requires two dc supplies, its use is limited.

3.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 3.5.

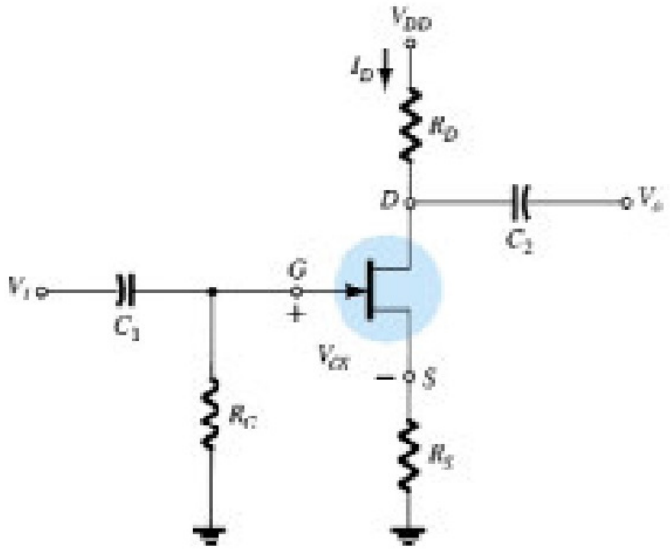


Fig 3.5 JFET self-bias configuration

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0$ A. The result is the network of Fig. 3.6 for the important dc analysis.

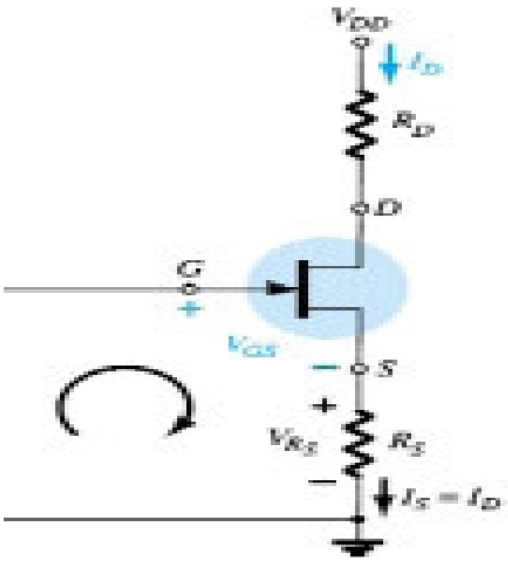


Fig 3.6 DC analysis of the self-bias configuration

For the indicated closed loop of Fig. 3.6, we find that

$V_{GS} = -I_D R_S$----------(3.10)

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

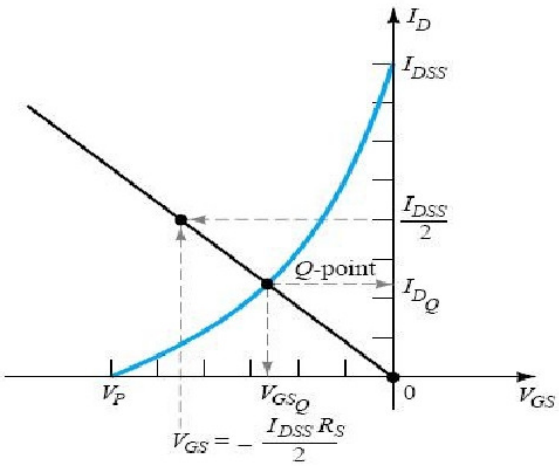


Fig 3.7 Sketching the self-bias line

The level of V_{DS} can be determined by applying Kirchhoff's voltage law to the output circuit, with the result that,

$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$

Or, $\mathbf{V_{DS} = V_{DD} - I_D(R_S - R_D)}$ ----------(3.11)

Keep in mind, $\mathbf{V_S = I_D R_S}$----------(3.12)

$\mathbf{V_G = 0V}$----------(3.13) $\mathbf{V_D = V_{DS} + V_S = V_{DD} - V_{RD}}$ ----------(3.14)

3.4 VOLTAGE-DIVIDER BIASING

The voltage-divider bias arrangement applied to BJT transistor amplifiers is also applied to FET amplifiers as demonstrated by Fig. 3.8. The basic construction is exactly the same, but the dc analysis of each is quite different. $I_G = 0$A for FET amplifiers, but the magnitude of I_B for common-emitter BJT amplifiers can affect the dc levels of current and voltage in both the input and output circuits. Recall that I_B provided the link between input and output circuits for the BJT voltage-divider configuration while V_{GS} will do the same for the FET configuration.

The network of Fig. 3.8 is redrawn as shown in Fig. 3.9 for the dc analysis. Note that all the capacitors, including the bypass capacitor C_S, have been replaced by an "open-circuit" equivalent. In addition, the source V_{DD} was separated into two equivalent sources to permit a further separation of the input and output regions of the network.

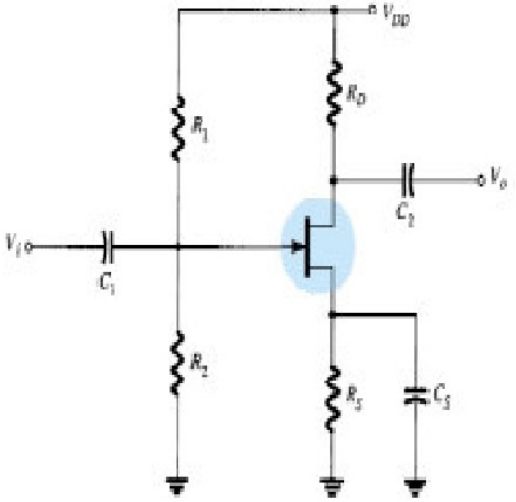


Fig 3.8 Voltage-divider bias arrangement

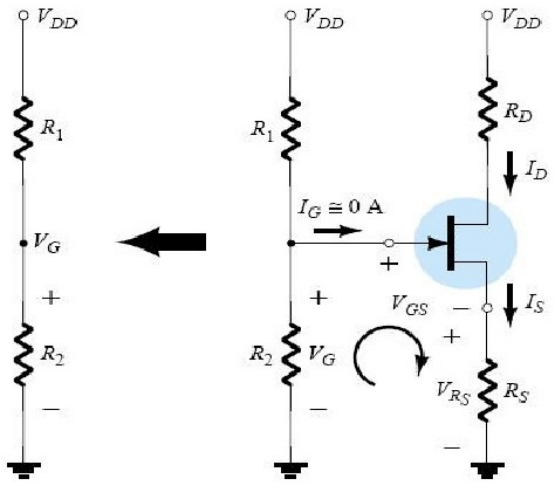


Fig 3.9 Redrawn network of Fig.3.8 for dc analysis

Since $I_G = 0$A, Kirchhoff's current law requires that $I_{R_1} = I_{R_2}$ and the series equivalent circuit appearing to the left of the figure can be used to find the level of V_G. The voltage V_G, equal to the voltage across R_2, can be found using the voltage-divider rule as follows:

$$\mathbf{V_G = V_{DD}R_2/R_1+R_2}\text{----------(3.15)}$$

Applying Kirchhoff's voltage law in the clockwise direction to the indicated loop of Fig. 3.9 will result in
$V_G - V_{GS} - V_{RS} = 0$
Substituting $V_{RS} = I_S R_S = I_D R_S$, we have

$$\mathbf{V_{GS} = V_G - I_D R_S}\text{----------(3.16)}$$

The result is an equation that continues to include the same two variables appearing in Shockley's equation: V_{GS} and I_D. The quantities V_G and R_S are fixed by the network construction. Equation (3.16) is still the equation for a straight line. The two points are:

$V_{GS} = V_G | I_D = 0\text{mA}$ ----------(3.17) $I_D = V_G/R_S | V_{GS} = 0\text{V}$ ----------(3.18)

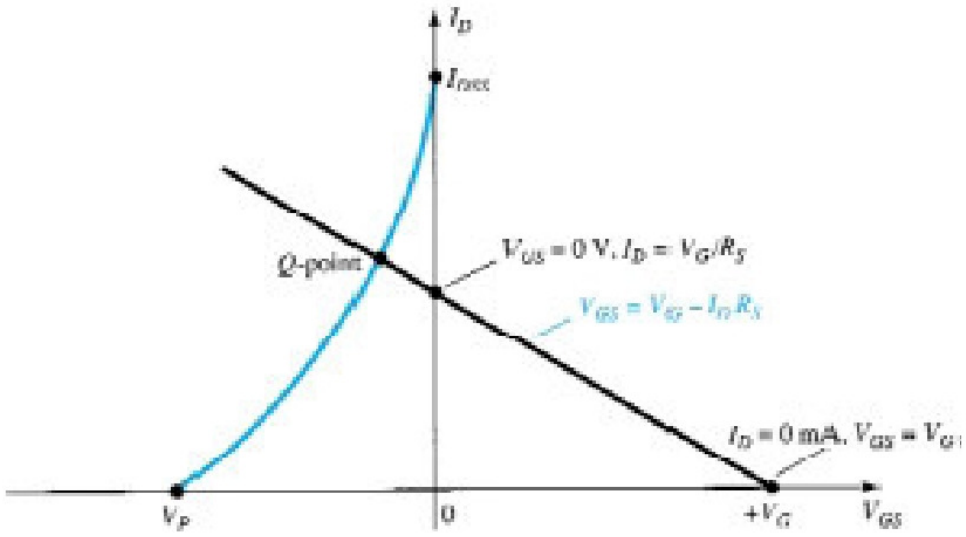


Fig 3.10 Sketching the network equation for the voltage-divider configuration

Increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.

Once the quiescent values of I_{DQ} and V_{GSQ} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$\mathbf{V_{DS} = V_{DD} - I_D(R_D + R_S)}\text{----------(3.19)}$$
$$\mathbf{V_D = V_{DD} - I_D R_D}\text{----------(3.20)}\ \mathbf{V_S = I_D R_S}\text{----------(3.21)}\ \mathbf{I_{R1} = I_{R2} = V_{DD}/R_1+R_2}\text{----------(3.22)}$$

3.5 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The *primary difference* between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceeds I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.
The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network.

3.6 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 3.11.

For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$\mathbf{I_D = k[V_{GS} - V_{GS(Th)}]} \text{ ----------(3.23)}$$

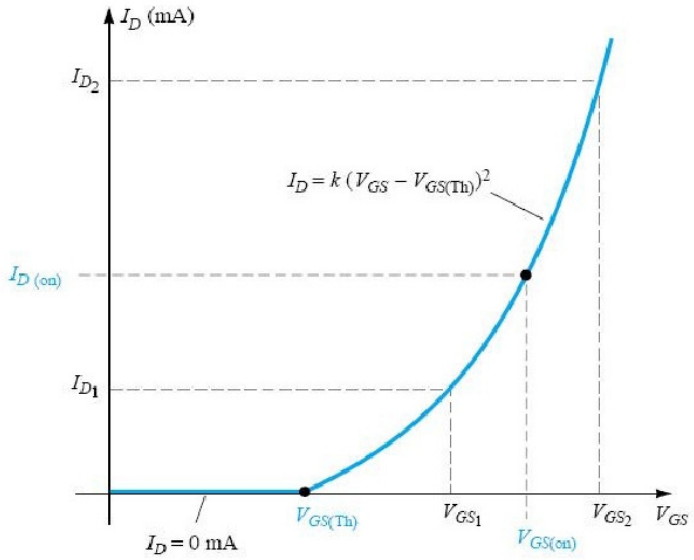


Fig 3.11 Transfer characteristics of an *n*-channel enhancement-type MOSFET

Since specification sheets typically provide the threshold voltage and a level of drain current (I_D(on)) and its corresponding level of V_{GS}(on), two points are defined immediately as shown in Fig. 3.11. To complete the curve, the constant *k* of Eq. (3.11) must be determined from the specification sheet data by substituting into Eq. (3.11) and solving for *k* as follows:

$I_D = k[V_{GS} - V_{GS(Th)}]^2$

Or, $I_{D(ON)} = k[V_{GS(ON)} - V_{GS(Th)}]^2$

$$\mathbf{k = I_{D(ON)} / [V_{GS(ON)} - V_{GS(Th)}]^2} \text{ ----------(3.24)}$$

Once *k* is defined, other levels of I_D can be determined for chosen values of V_{GS}. Typically, a point between $V_{GS(Th)}$ and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ will provide a sufficient number of points to plot Eq. (3.11).

FEEDBACK BIASING ARRANGEMENT

A popular biasing arrangement for enhancement-type MOSFETs is provided in Fig. 3.12. The resistor R_G brings a suitably large voltage to the gate to drive the MOSFET "on." Since I_G = 0 mA and V_{RG} = 0 V, the dc equivalent network appears as shown in Fig. 3.13.
A direct connection now exists between drain and gate, resulting in
$V_D = V_G$
and $\mathbf{V_{DS} = V_{GS}}$ ----------(3.25)

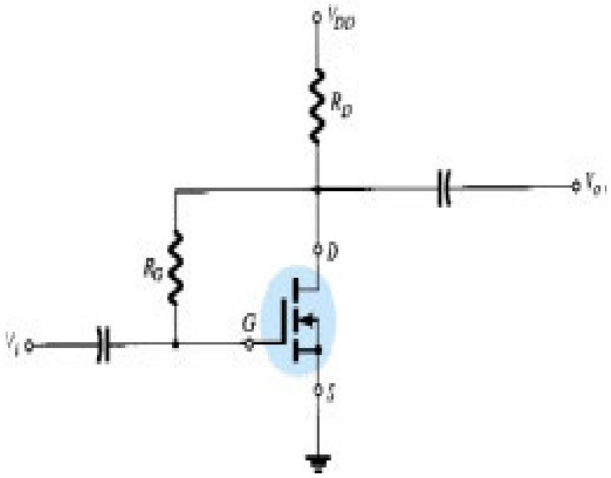


Fig 3.12 Feedback biasing arrangement

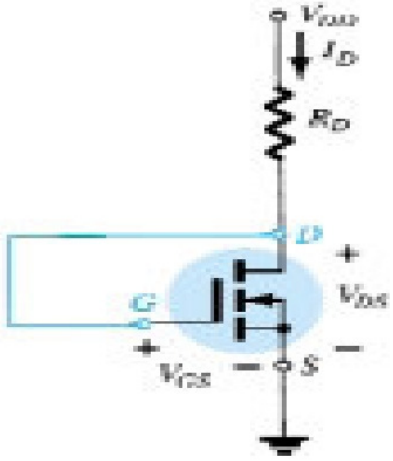


Fig 3.13 DC equivalent of the network of Fig. 3.12

For the output circuit,

$V_{DS} = V_{DD} - I_D R_D$

$$\mathbf{V_{GS} = V_{DD} - I_D R_D} \text{----------(3.26)}$$

The two points defining the Eq. (3.26) as a straight line,

$$\mathbf{V_{GS} = V_{DD} | I_{D=0mA}} \text{----------(3.27)}$$

$$\mathbf{I_D = V_{DD}/R_D | V_{GS=0V}} \text{----------(3.28)}$$

The plots defined by Eqs. (3.23) and (3.26) appear in Fig. 6.38 with the resulting operating point.

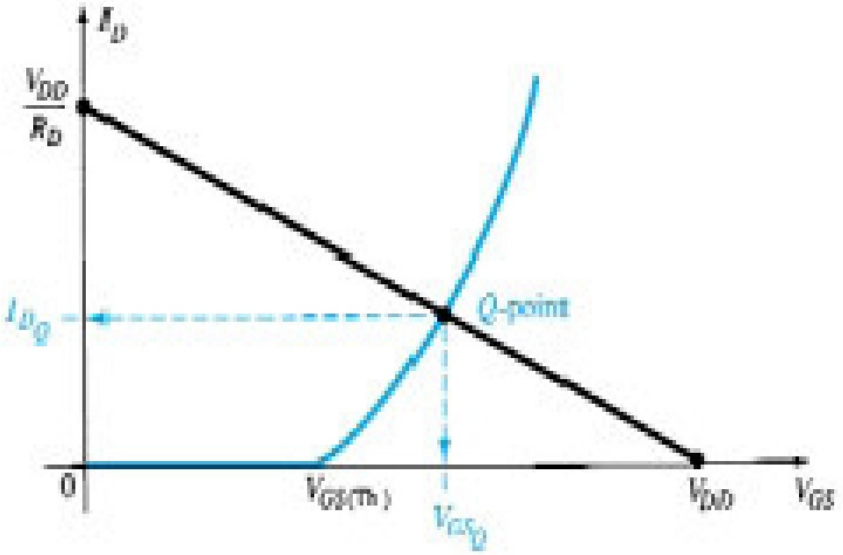


Fig 3.14 Determining the *Q*-point for the network of Fig. 3.12

VOLTAGE-DIVIDER BIASING ARRANGEMENT

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 3.15.

The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$\mathbf{V_G = V_{DD} R_2 / R_1 + R_2} \text{----------(3.29)}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 3.15 will result in,

$+V_G - V_{GS} - V_{RS} = 0$

Or, $$\mathbf{V_{GS} = V_G - I_D R_S} \text{----------(3.30)}$$

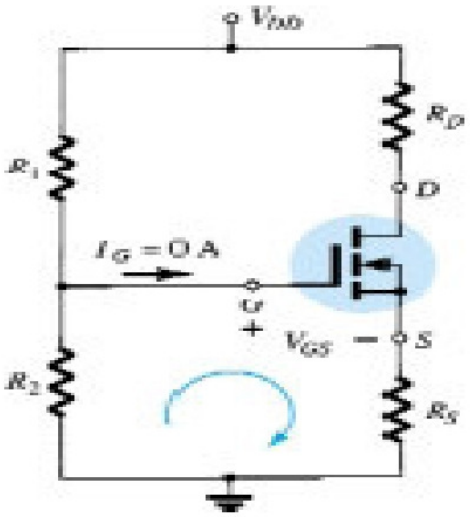


Fig 3.15 Voltage-divider biasing arrangement for an *n*-channel enhancement MOSFET

For the output section:

$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$

Or, $\mathbf{V_{DS} = V_{DD} - I_D(R_S + R_D)}$ ----------(3.31)

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (3.30) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{DQ} and V_{GSQ} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

Topic 4 SMALL SIGNAL ANALYSIS OF BJTS

4.1 INTRODUCTION

A model is the combination of circuit elements, properly chosen, that best approximates the actual behavior of a semiconductor device under specific operating conditions.

Once the ac equivalent circuit has been determined, the graphical symbol of the device can be replaced in the schematic by this circuit and the basic methods of accircuit analysis (mesh analysis, nodal analysis, and Thévenin's theorem) can be applied to determine the response of the circuit.

There are two models commonly used in the small-signal ac analysis of transistor networks: the r_e model and the hybrid equivalent model.

4.2 AC EQUIVALENT-CIRCUIT MODEL

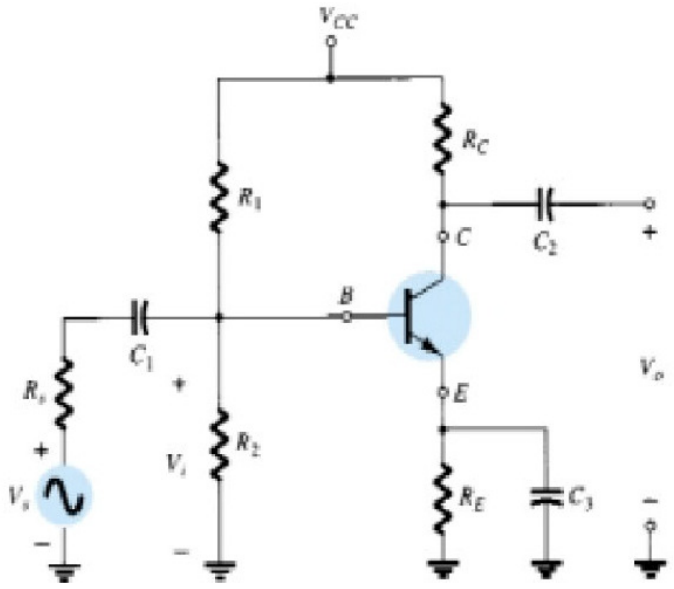


Fig 4.1 Transistor circuit

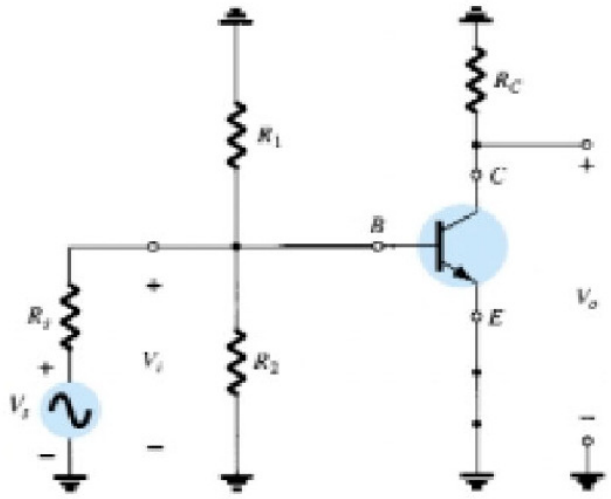


Fig 4.2 The network of Fig. 4.1 following removal of the dc supply and insertion of the short-circuit equivalent for the capacitors

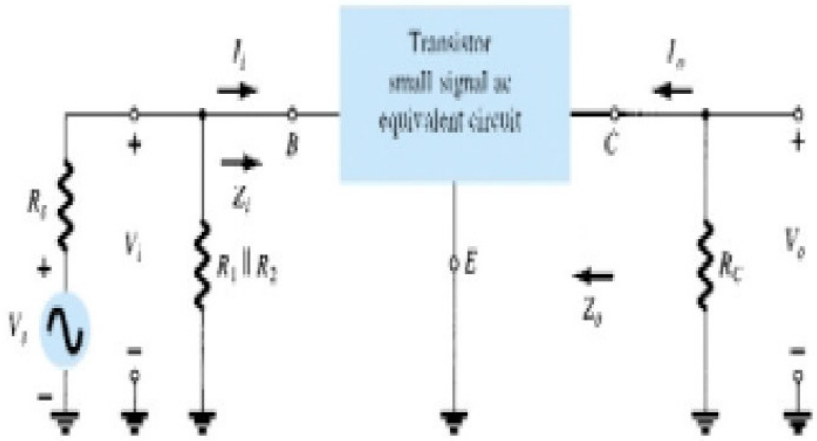


Fig 4.3 Circuit of Fig. 4.1 redrawn for small-signal ac analysis

In summary, the ac equivalent of a network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent
2. Replacing all capacitors by a short-circuit equivalent
3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2
4. Redrawing the network in a more convenient and logical form

4.3 THE IMPORTANT PARAMETERS: Z_i, Z_0, A_v, A_i

For the two-port (two pairs of terminals) system of Fig. 4.4, the input side (the side to which the signal is normally applied) is to the left and the output side (where the load is connected) is to the right.

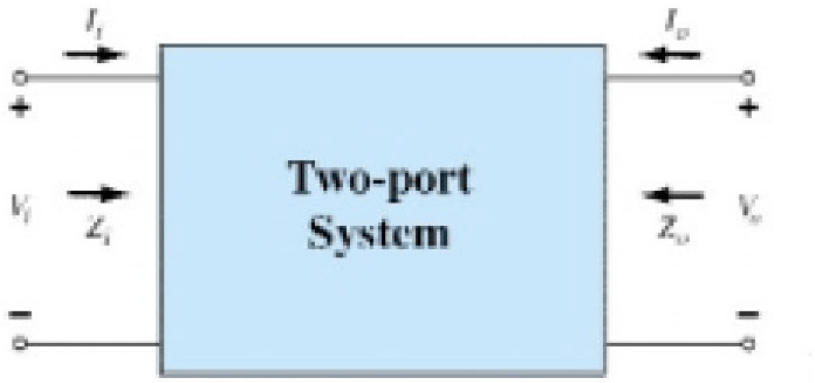


Fig 4.4 Two-port system

Input Impedance, Z_i

$Zi=V_i/Ii$

Output Impedance, Z_o

$Z_0=V_0/I_0$

Voltage Gain, A_v

$A_v = V_0/V_i$

Current Gain, A_i

$A_i = I_0/I_i$

4.4 THE *re* TRANSISTOR MODEL

The *re* model employs a diode and controlled current source to duplicate the behaviour of a transistor in the region of interest.

Common Base Configuration

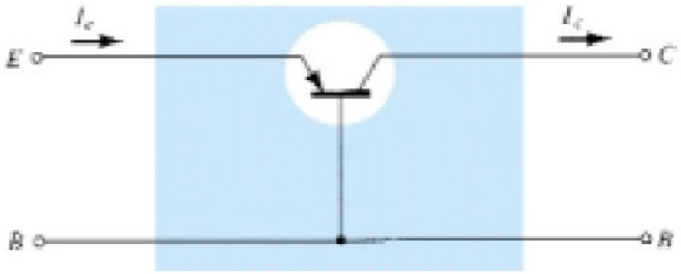


Fig 4.5 Common-base BJT transistor

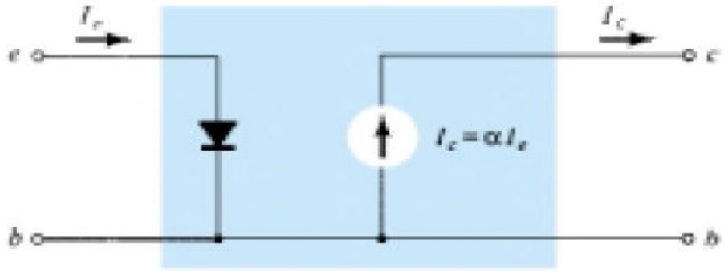


Fig 4.6 *re* model for the configuration

$$\mathbf{r_e = 26mV/I_E}$$

The subscript *e* of *re* was chosen to emphasize that it is the dc level of emitter current that determines the ac level of the resistance of the diode of Fig. 4.6. Substituting the resulting value of *re* in Fig. 4.6 will result in the very useful model of Fig. 4.7.

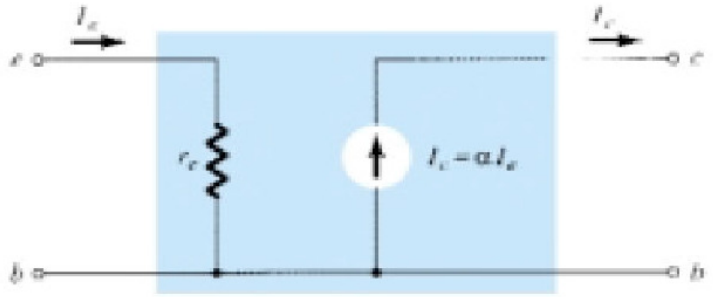


Fig. 4.7 Common Base r_e equivalent circuit

$$Z_i = r_e$$

$$Z_o = \infty \text{ ohm}$$

$$A_v = \alpha R_L/r_e = R_L/r_e$$

$$A_i = -\alpha = -1$$

Common Emitter Configuration

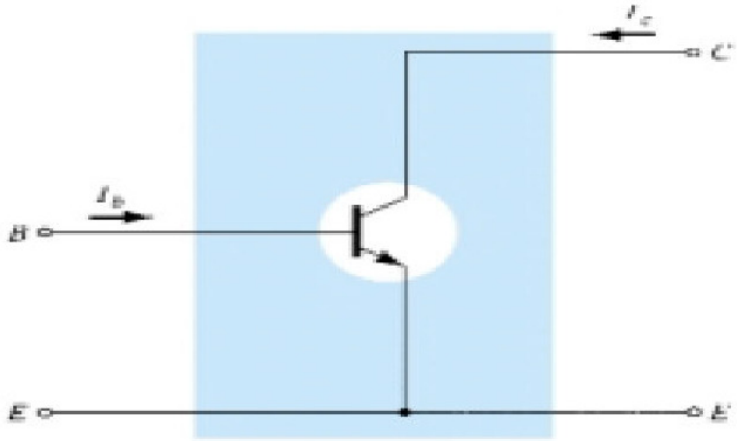


Fig 4.8 Common-emitter BJT transistor

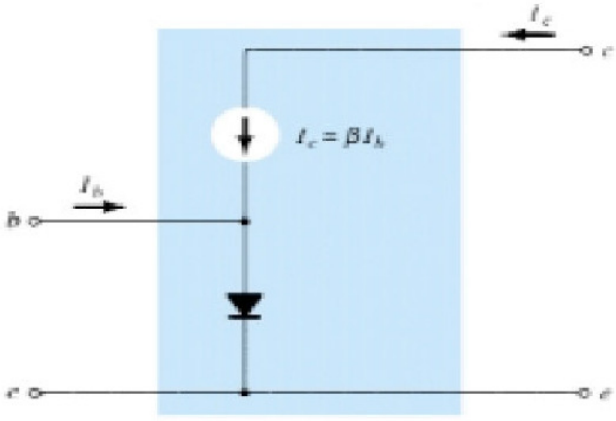


Fig 4.9 *re* model for the configuration

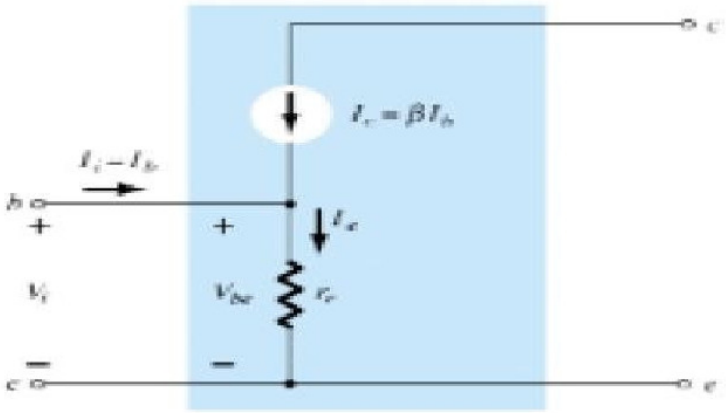


Fig 4.10 Common Emitter re equivalent circuit

$$Z_i = \beta R_E$$

$$Z_o = r_o$$

$$A_v = -R_L/r_e$$

$$A_i = \beta$$

4.5 THE HYBRID EQUIVALENT MODEL

The *re* model for a transistor is sensitive to the dc level of operation of the amplifier. The result is an input resistance that will vary with the dc operating point.

For the hybrid equivalent model, the parameters are defined at an operating point that may or may not reflect the actual operating conditions of the amplifier. This is due to the fact that specification sheets cannot provide parameters for an equivalent circuit at every possible operating point. They must choose operating conditions that they believe reflect the general characteristics of the device.

The quantities*hie*,*hre*,*hfe*, and *hoe* are called the *hybrid parameters* and are the components of a small-signal equivalent circuit.

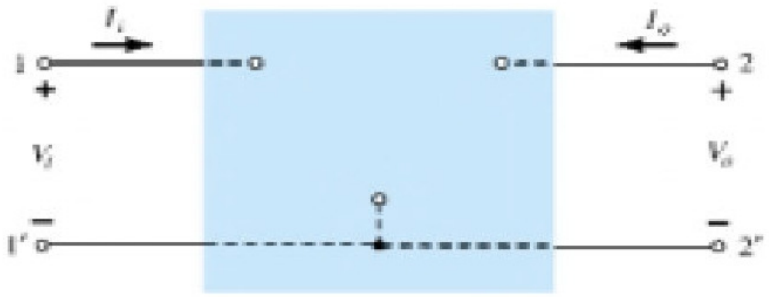


Fig 4.11 Two Port System

$V_i = h_{11}I_i + h_{12}Vo$
$I_o = h_{21}I_i + h_{22}V_o$

The parameters relating the four variables are called *h-parameters* from the word "hybrid." The term *hybrid* was chosen because the mixture of variables (*V* and*I*) in each equation results in a "hybrid" set of units of measurement for the *h*-parameters.

h_{11} = $V_i/I_i|_{Vo=0}$ = short-circuit input-impedance parameter

h_{12} = $V_i/V_o|_{Ii=0}$ = open-circuit reverse transfer voltage ratio parameter

h_{21} = $I_o/I_i|_{Vo=0}$ = short-circuit forward transfer current ratio parameter

h_{22} = $I_o/V_o|_{Io=0}$ = open-circuit output admittance parameter

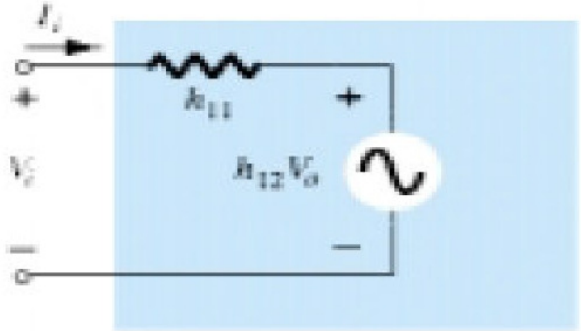


Fig 4.12 Hybrid Input equivalent circuit

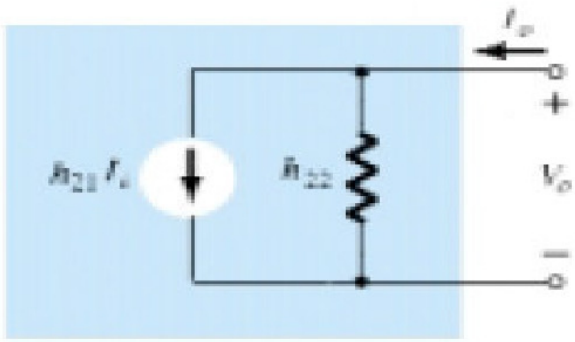


Fig 4.13 Hybrid Output equivalent circuit

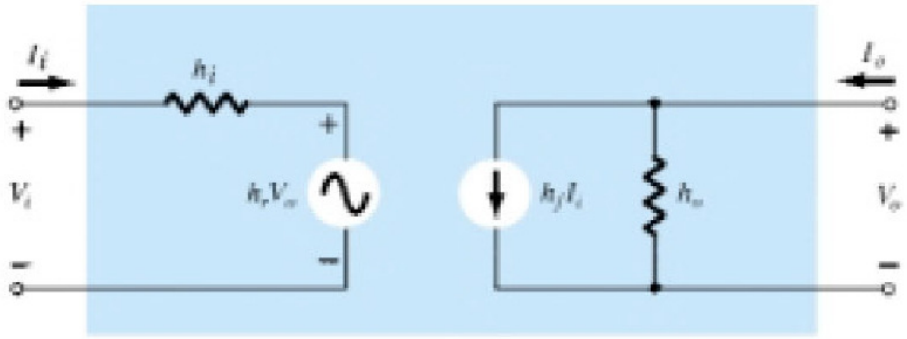


Fig 4.14 Complete Hybrid Equivalent Model

Where,

h_{11} = input resistance = h_i
h_{12} = reverse transfer voltage ratio = h_r
h_{21} = forward transfer current ratio = h_f
h_{22} = output conductance = h_o

Common Base Configuration

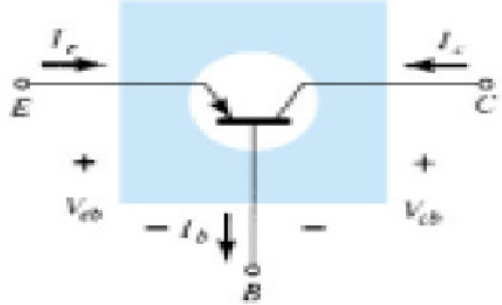


Fig 4.15 Graphical Symbol

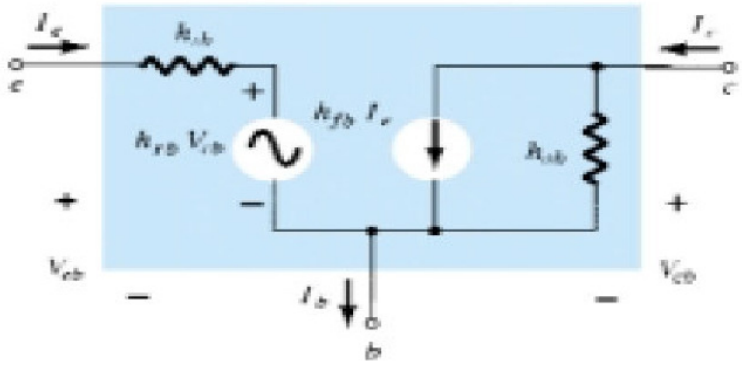


Fig 4.16 Hybrid equivalent circuit

Common Emitter Configuration

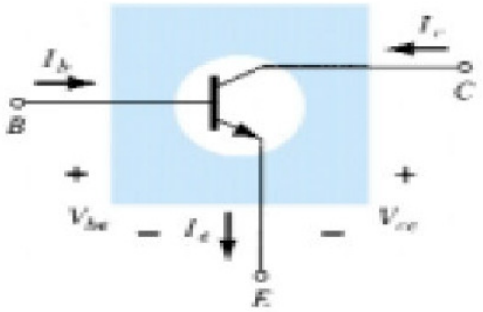


Fig 4.17 Graphical Symbol

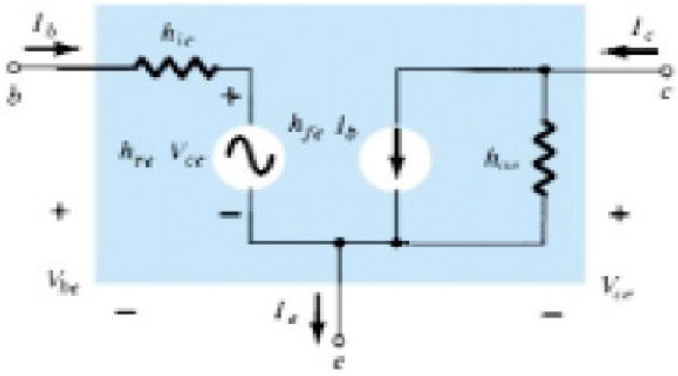
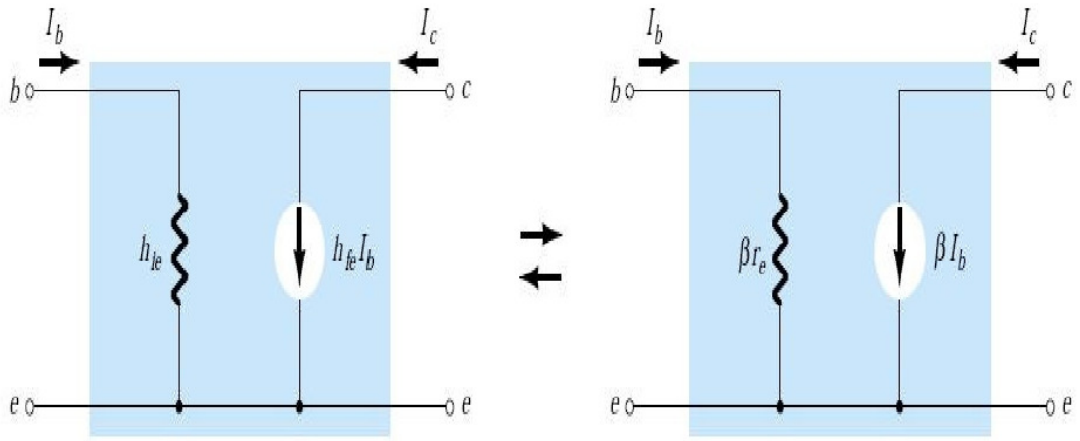


Fig 4.18 Hybrid equivalent model

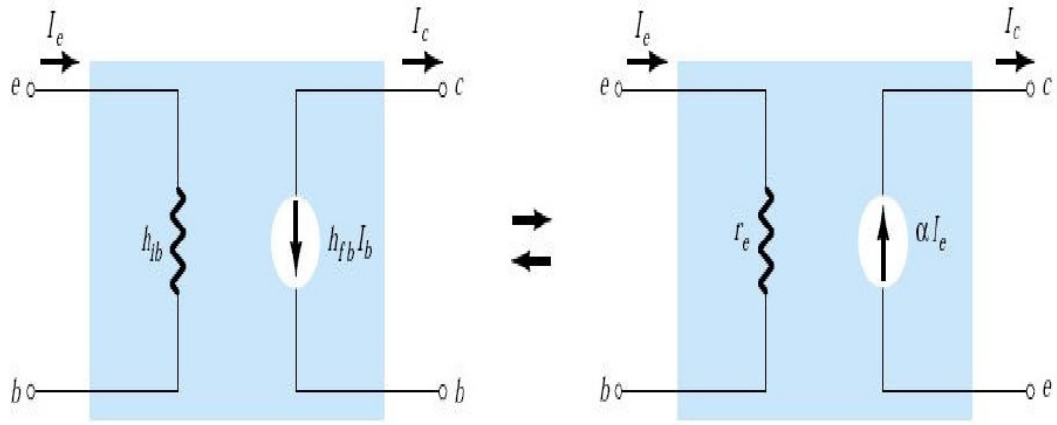
Common Emitter (Hybrid vs r_e model)



$$\mathbf{h_{ie} = \beta re}$$

$$\mathbf{h_{fe} = \beta ac}$$

Common Base (Hybridvs r_e model)



$$\mathbf{h_{ib} = r_e}$$

$$\mathbf{h_{fb} = - \alpha = -1}$$

4.6 GRAPHICAL DETERMINATION OF THE *h*-PARAMETERS

Using partial derivatives (calculus), it can be shown that the magnitude of the *h*-parameters for the small-signal transistor equivalent circuit in the region of operation.

For the common-emitter configuration h-parameters can be found using the following equations:

$$\mathbf{h_{ie} = \partial v_i/\partial i_i = \partial v_{be}/\partial i_b = \Delta v_{be}/\Delta i_b|_{VCE=constant}\ (ohms)}$$

$$\mathbf{h_{re} = \partial v_i/\partial v_o = \partial v_{be}/\partial v_{ce} = \Delta v_{be}/\Delta v_{ce}|_{IB=constant}\ (unitless)}$$

$$\mathbf{h_{fe} = \partial i_o/\partial i_i = \partial i_c/\partial i_b = \Delta i_c/\Delta i_b|_{VCE=constant}\ (unitless)}$$

$$\mathbf{h_{oe} = \partial i_o/\partial v_o = \partial i_c/\partial v_{ce} = \Delta i_c/\Delta v_{ce}|_{IB=constant}\ (ohms)}$$

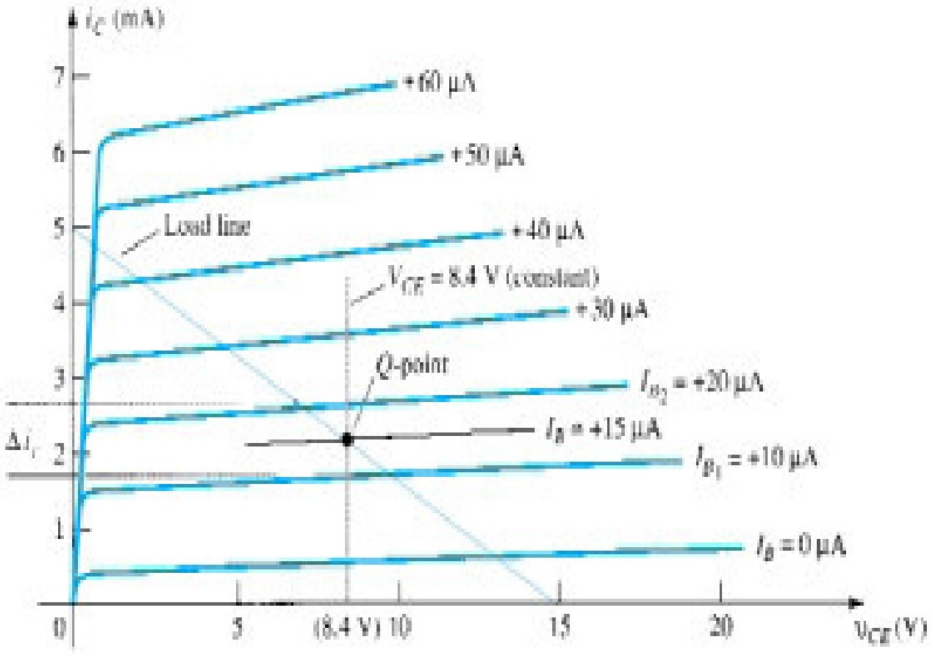


Fig 4.19 h_{fe} determination

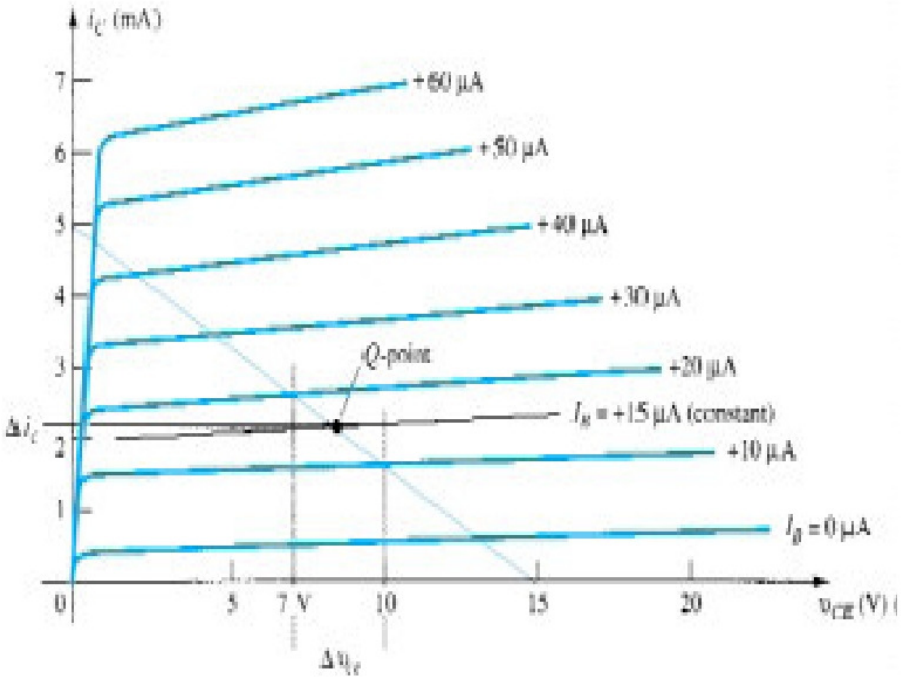


Fig 4.20 h_{oe} determination

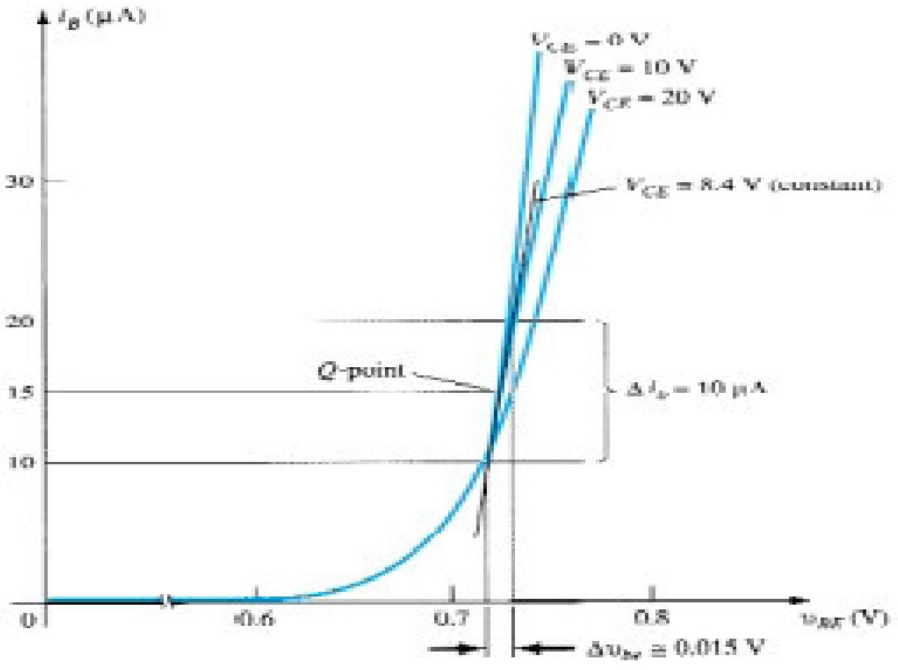


Fig 4.21 h_{ie} determination

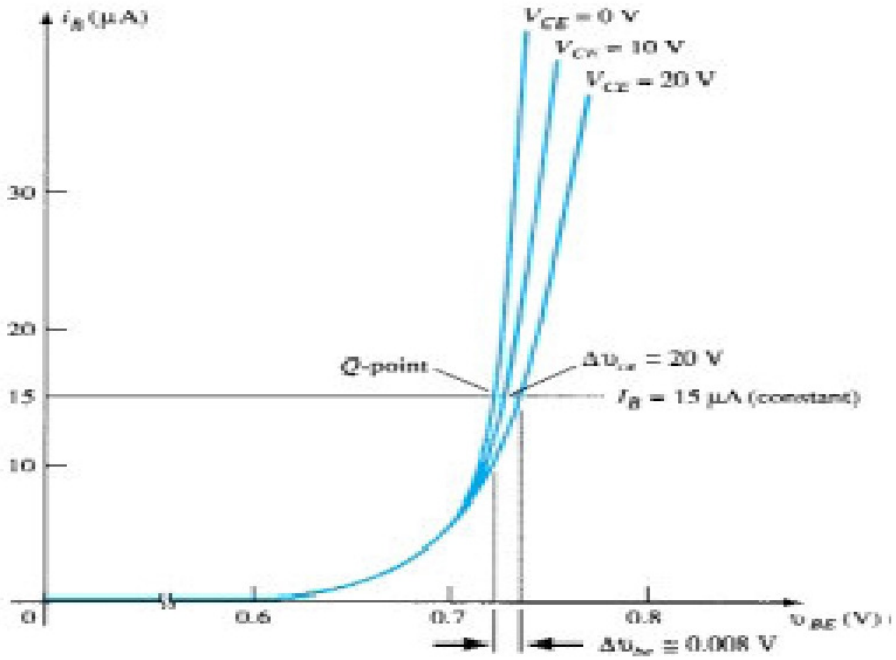


Fig 4.22 h_{re} determination

4.7 COMMON EMITTER FIXED-BIAS CONFIGURATION

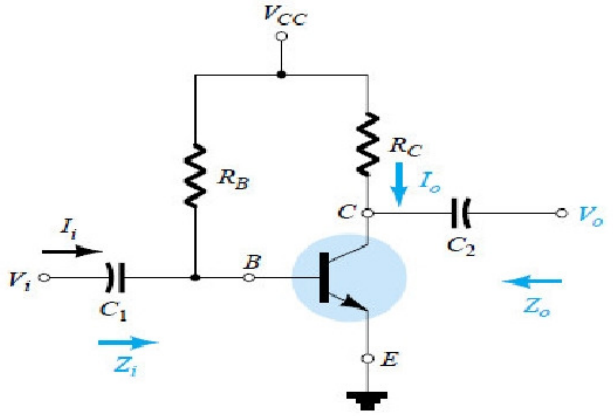


Fig. 4.23 Common-emitter fixed-bias configuration

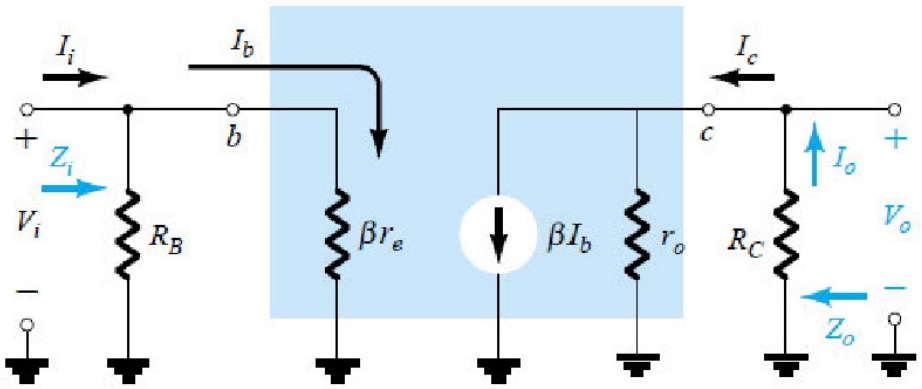


Fig. 4.24 Substituting the *re* model into the network of Fig 4.23

$$\mathbf{Z_i} = R_B \| \beta r_e$$

$$Z_o = R_C \| r_o$$

$$A_v = -(r_o \| R_c)/r_e$$

$$A_i = (R_B \beta r_o)/((r_o + R_c)(R_B + \beta r_e))$$

4.8 COMMON EMITTER VOLTAGE-DIVIDER BIAS CONFIGURATION

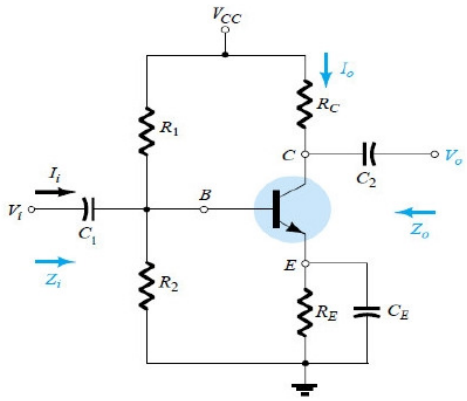


Fig. 4.24 Voltage - divider bias configuration

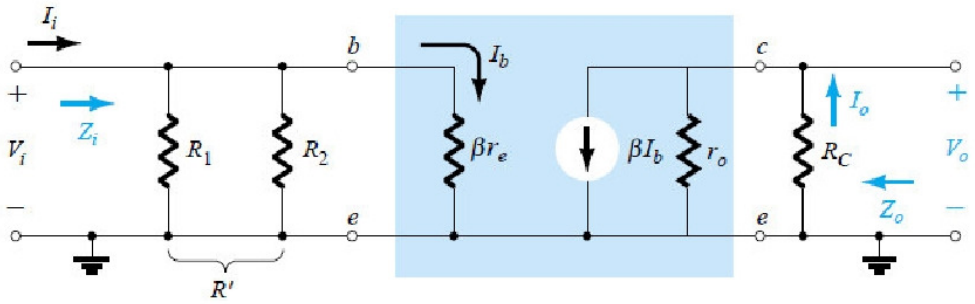


Fig. 4.25 Substituting the *re* model into the network of Fig 4.24

$$Z_i = R_1 \| R_2 \| \beta r_e$$

$$Z_o = r_o \| R_c$$

$$A_v = -(r_o \| R_c)/r_e$$

$$A_i = (R_B \beta r_o)/((r_o + R_c)(R_B + \beta r_e))$$

4.9 COMMON EMITTER-BIAS CONFIGURATION (UNBYPASSED)

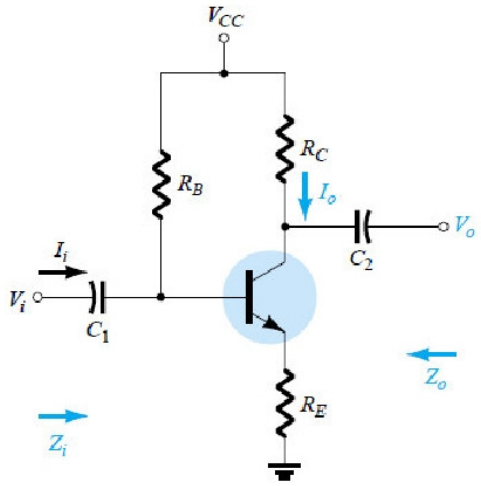


Fig. 4.27 Common Emitter Bias Configuration

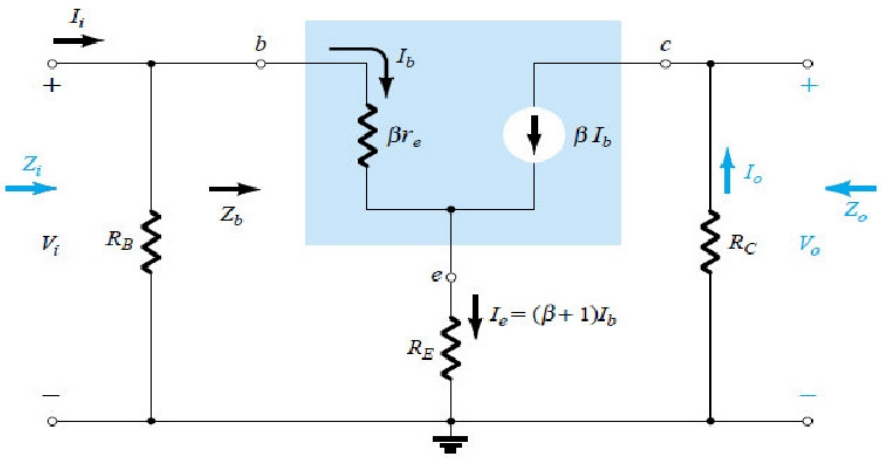


Fig. 4.28 Substituting the *re* model into the network of Fig 4.27

$$Z_i = R_B \| \beta(r_e + R_E)$$

$$Z_o = R_c$$

$$A_v = -(R_c)/(r_e + R_E)$$

$$A_i = (R_B\beta)/(R_B + \beta(r_e + R_E))$$

4.10 COMMON BASE CONFIGURATION

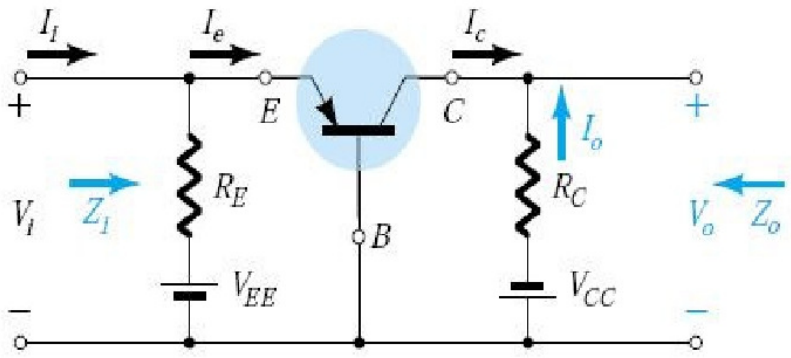


Fig. 4.29 Common Base Configuration

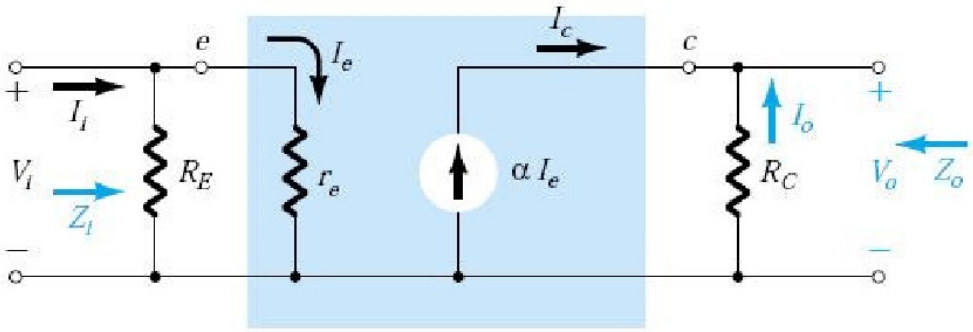


Fig. 4.30 Substituting the *re* model into the network of Fig 4.29

$$Z_i = R_E \| r_e$$

$$Z_O = R_C$$

$$A_V = R_C / r_e$$

$$A_i = -1$$

4.11 COLLECTOR FEEDBACK CONFIGURATION

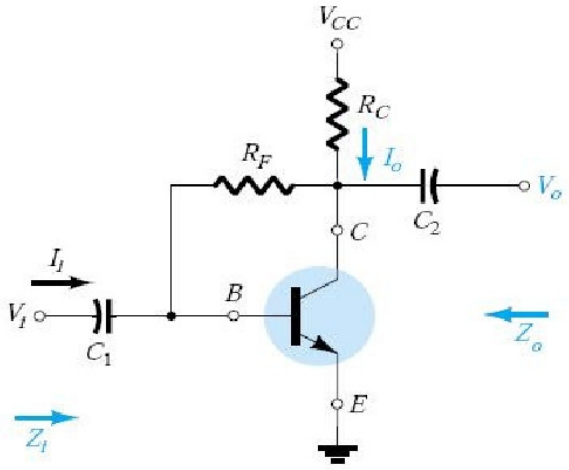


Fig. 4.31 Collector Feedback Configuration

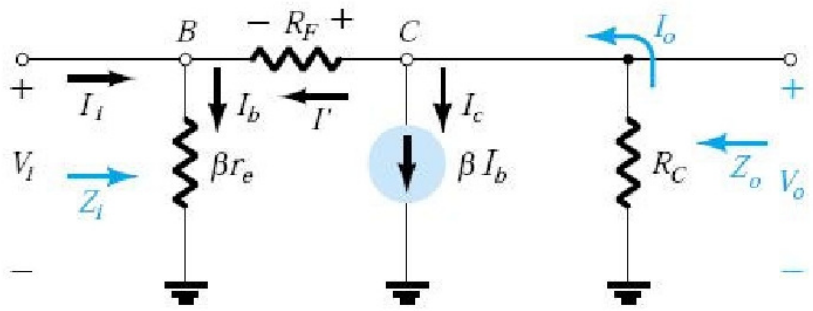


Fig 4.32 Substituting the *re* model into the network of Fig 4.31

$$Z_i = r_e/(1/\beta + R_C/R_F)$$

$$Z_O = R_C \| R_F \quad A_V = -R_C/r_e \quad A_i = R_F/R_C$$

4.12 APPROXIMATE HYBRID EQUIVALENTCIRCUIT

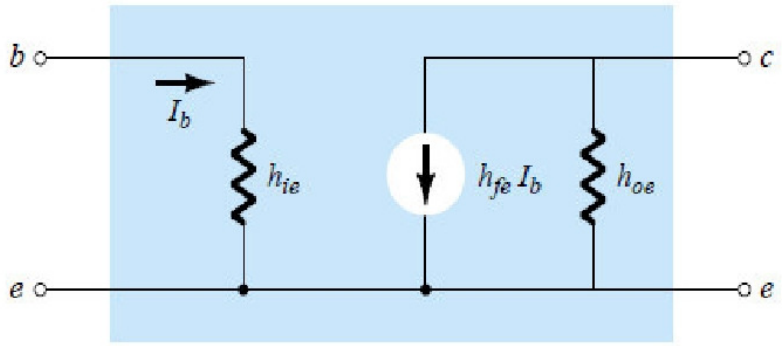


Fig. 4.33 Approximate Common-Emitter hybrid equivalent circuit

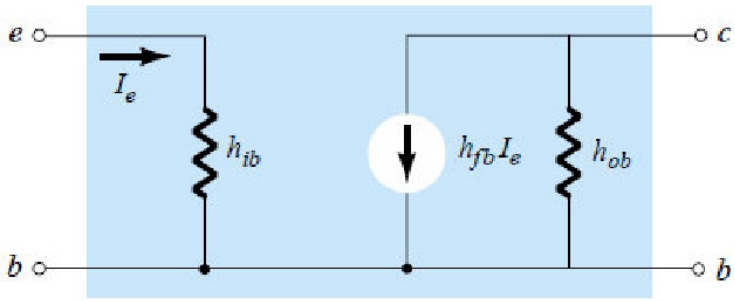
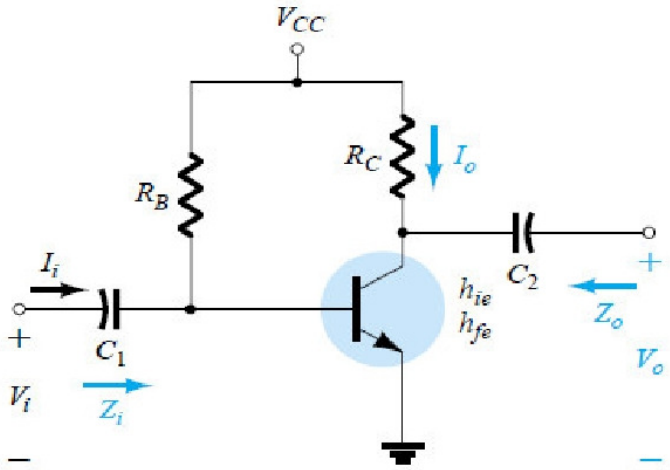
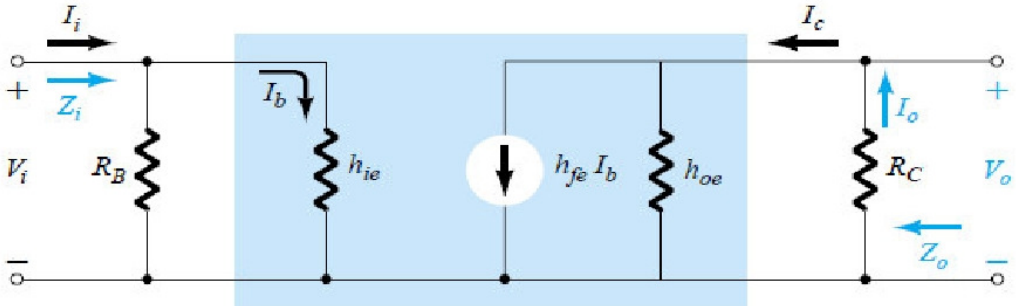


Fig. 4.34 Approximate Common-Base hybrid equivalent circuit

FIXED-BIAS CONFIGURATION





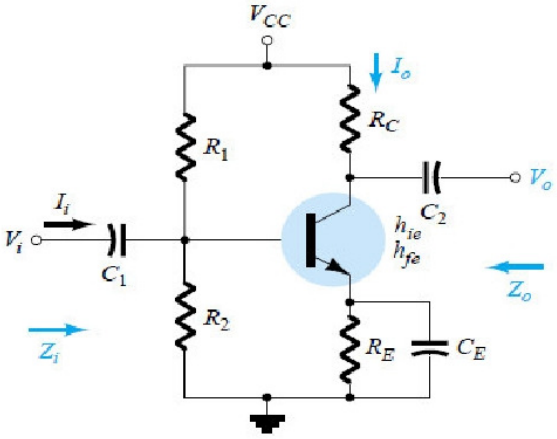
$Z_i=R_B\|h_{ie}$

$Z_o=R_c\|(1/h_{ie})$

$A_v=-(h_{fe}(R_c\|(1/h_{oe})))/h_{ie}$

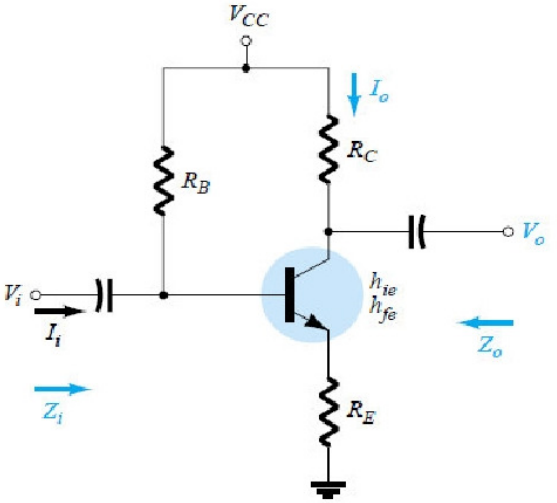
$A_i=h_{fe}$

VOLTAGE-DIVIDER BIAS CONFIGURATION



$$Z_i=R_B||h_{ie}$$
$$Z_o=R_c||(1/h_{ie})$$
$$A_v=-(h_{fe}(R_c||(1/h_{oe})))/h_{ie}$$
$$A_i=h_{fe}$$

UNBYPASSED EMITTER-BIAS CONFIGURATION



$$Z_i=h_{ie}+h_{fe}R_E$$
$$Z_o=R_c$$
$$A_v=-(h_{fe}R_c)/(h_{ie}+R_Eh_{fe})$$
$$A_i=(h_{fe}(R_B||Z_b))/(h_{ie}+R_Eh_{fe})$$

4.14 CASCADED SYSTEMS

The two-port systems approach is particularly useful for cascaded systems such as that appearing in Fig. 10.35, where Av1,Av2,Av3, and so on, are the voltage gains of each stage under loaded conditions. That is, Av1is determined with the input impedance to Av2 acting as the load on Av1. For Av2, Av1 will determine the signal strength and source impedance at the input to Av2.The total gain of the system is then determined by the product of the individual gains as follows:

$$\mathbf{A_{vt}=A_{v1}\,.A_{v2}\,.A_{v3}\,.\,A_{v4}}\text{……..}$$

and the total current gain by

$$\mathbf{A_{iT} = - A_{vT}(Z_{il}/\,R_L)}$$

No matter how perfect the system design, the application of a load to a two-port system will affect the voltage gain. Therefore, there is no possibility of a situation where Av1,Av2, and so on, of Fig. 10.35 are simply the no-load values. The loading of each succeeding stage must be considered.

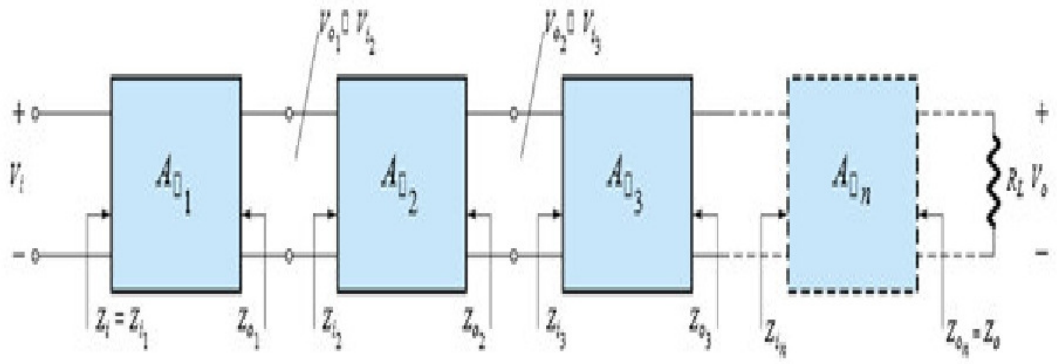


Fig. 4.35 Cascaded Systems

Topic 5 SMALL SIGNAL ANALYSIS OF FETS

5.1 INTRODUCTION

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also considered low-power consumption configurations with good frequency range and minimal size and weight. Both JFET and depletion MOSFET devices can be used to design amplifiers having similar voltage gains. The depletion MOSFET circuit, however, has a much higher input impedance than a similar JFET configuration.

While a BJT device controls a large output (collector) current by means of a relatively small input (base) current, the FET device controls an output (drain) current by means of a small input (gate-voltage) voltage. In general, therefore, the BJT is a *current-controlled* device and the FET is a *voltage-controlled* device. In both cases, however, note that the output current is the controlled variable. Because of the high input characteristic of FETs, the ac equivalent model is somewhat simpler than that employed for BJTs. While the BJT had an amplification factor β (beta), the FET has a transconductance factor, *gm*.

The FET can be used as a linear amplifier or as a digital device in logic circuits. In fact, the enhancement MOSFET is quite popular in digital circuitry, especially in CMOS circuits that require very low power consumption. FET devices are also widely used in high-frequency applications and in buffering (interfacing) applications.

While the common-source configuration is the most popular providing an inverted, amplified signal, one also finds common-drain (source-follower) circuits providing unity gain with no inversion and common-gate circuits providing gain with no inversion. As with BJT amplifiers, the important circuit features described in this chapter include voltage gain, input impedance, and output impedance. Due to the very high input impedance, the input current is generally assumed to be 0 μA and the current gain is an undefined quantity. While the voltage gain of an FET amplifier is generally less than that obtained using a BJT amplifier, the FET amplifier provides much higher input impedance than that of a BJT configuration. Output impedance values are comparable for both BJT and FET circuits.

5.2 FET SMALL-SIGNAL MODEL

The ac analysis of an FET configuration requires that a small-signal ac model for the FET be developed. A major component of the ac model will reflect the

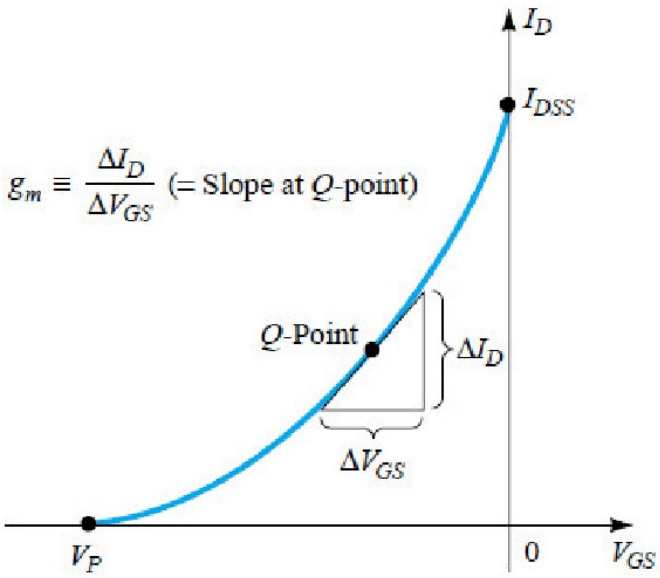
fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.
The gate-to-source voltage controls the drain-to-source (channel) current of an FET.

A dc gate-to-source voltage controlled the level of dc drain current through a relationship known as Shockley's equation: $I_D=I_{DSS}(V_{GS}-V_p)^2$

The *change* in collector current that will result from a *change* in gate-to-source voltage can be determined using the transconductance factor*gm* in the following manner: $\Delta I_D=g_m \Delta V_{GS}$

The prefix *trans-* in the terminology applied to*gm* reveals that it establishes a relationship between an output and input quantity. The root word *conductance* was chosen because*gm* is determined by a voltage-to-current ratio similar to the ratio that defines the conductance of a resistor $G = 1/R = I/V$ or, $g_m=\Delta I_D/\Delta V_{GS}$

5.3. GRAPHICAL DETERMINATION OF gm .



$g_m=m=\Delta y/\Delta x=\Delta I_D/\Delta V_{GS}$

5.4 MATHEMATICAL DEFINITION OF gm

$gm= 2\ I_{DSS}/|Vp|[1-V_{GS}/Vp]$

$gm0 = 2\ I_{DSS} / |Vp|$

$gm = gm0[1 - V_{GS}/Vp]$

Impact of I_D on gm : $gm = gm0[1 - V_{GS}/Vp] = gm0(\sqrt{I_D/I_{DSS}})$

FET Input Impedance zi: Zi(FET) = ∞Ω

FET Output Impedance zo: Zo(FET) = rd

5.4 FET AC EQUIVALENT CIRCUIT

a model for the FET transistor in the ac domain can be constructed. The control of *Id* by*Vgs* is included as a current source*gmVgs* connected from drain to source as shown in Fig. 5.1. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

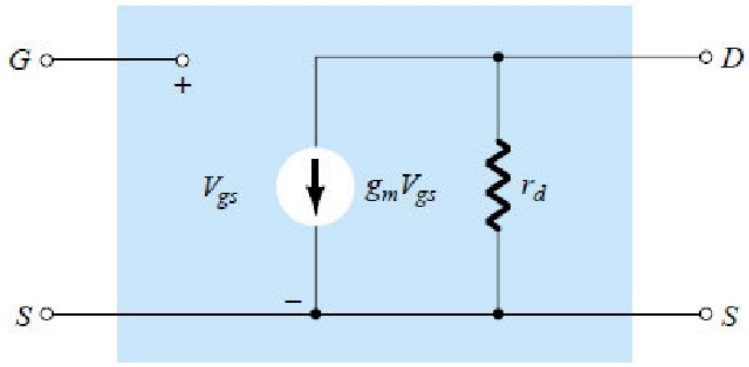


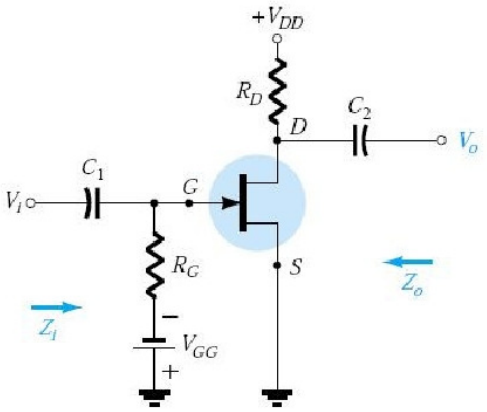
Fig. 5.1 FET AC Equivalent circuit

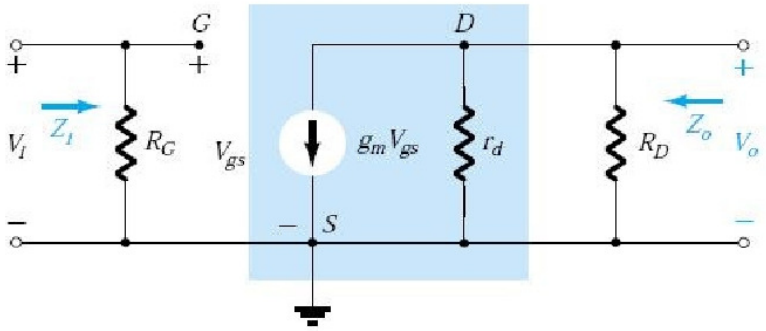
The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor*rd* from drain to source. Note that the gate to source voltage is now represented by*Vgs* (lower-case subscripts) to distinguish it from dc levels. In addition, take note of the fact that the source is common to both input and output circuits while the gate and drain terminals are only in "touch" through the controlled current source*gmVgs*.

In situations where*rd* is ignored (assumed sufficiently large to other elements of the network to be approximated by an open circuit), the equivalent circuit is

simply a current source whose magnitude is controlled by the signal*Vgs* and parameter*gm*— clearly a voltage-controlled device.

5.5 FIXED BIAS CIRCUIT



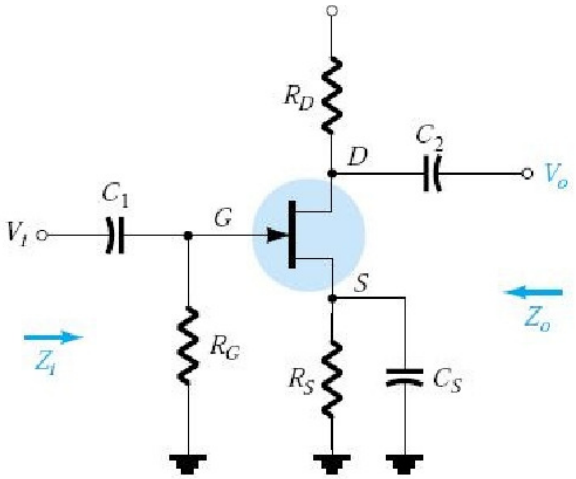


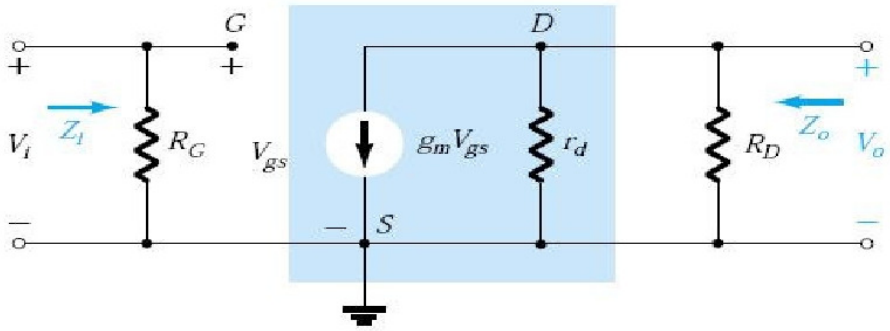
$$Z_i = R_G$$

$$Z_O = R_D \| r_d$$

$$Av = -gm(R_D \| r_d)$$

5.6 SELF BIAS CIRCUIT (UnbypassedRs)



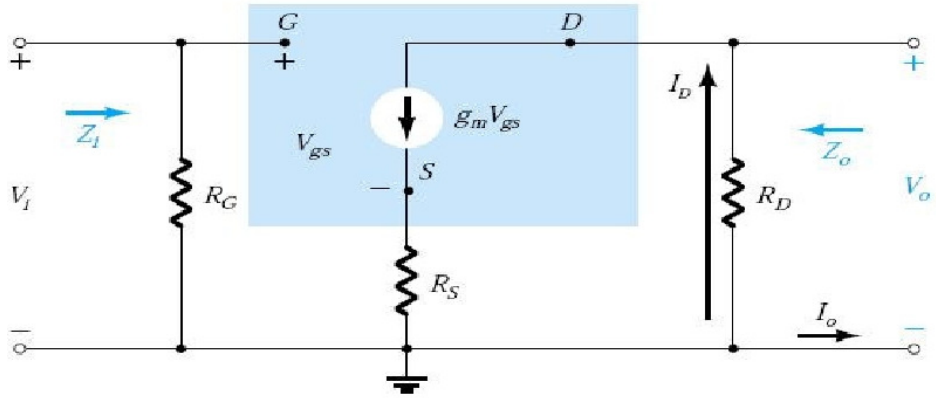


$$Z_i = R_G$$

$$Zo = R_D \| r_d$$

$$Av = -gm(R_D \| r_d)$$

5.6 SELF BIAS CIRCUIT (Bypassed Rs)

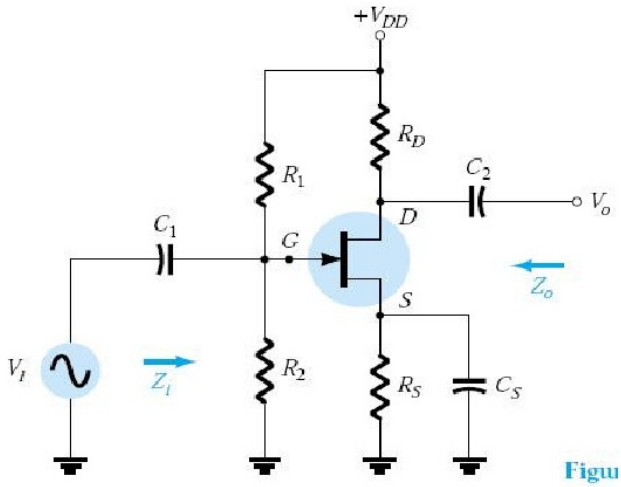


$$Z_i = R_G$$

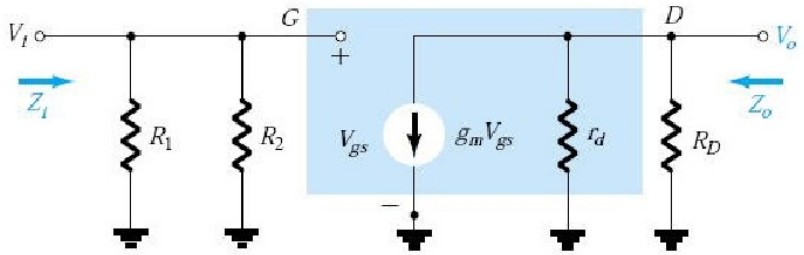
$$Zo = R_D$$

$$Av = -gmR_D[1+gmRs+(R_D+Rs)/r_d)]$$

5.6 VOLTAGE-DIVIDER CONFIGURATION



Figu

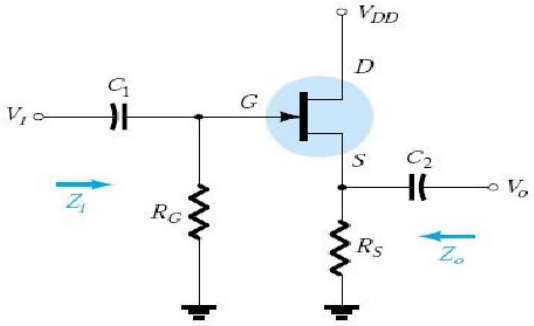


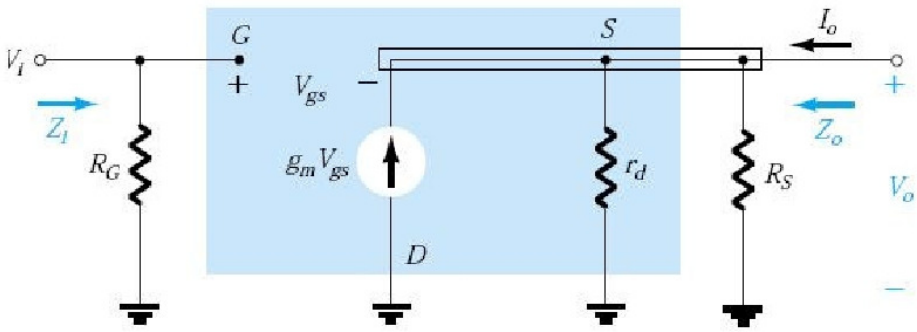
$$Z_i = R1 \| R2$$

$$Zo = r_d \| R_D$$

$$Av = -gm(r_d \| R_D)$$

5.7 SOURCE-FOLLOWER (COMMON-DRAIN) CONFIGURATION



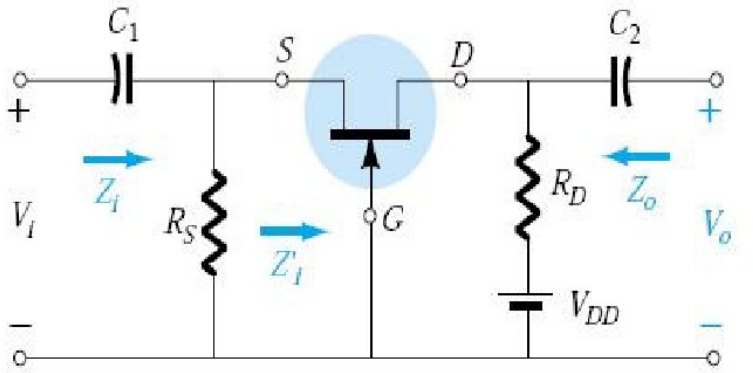


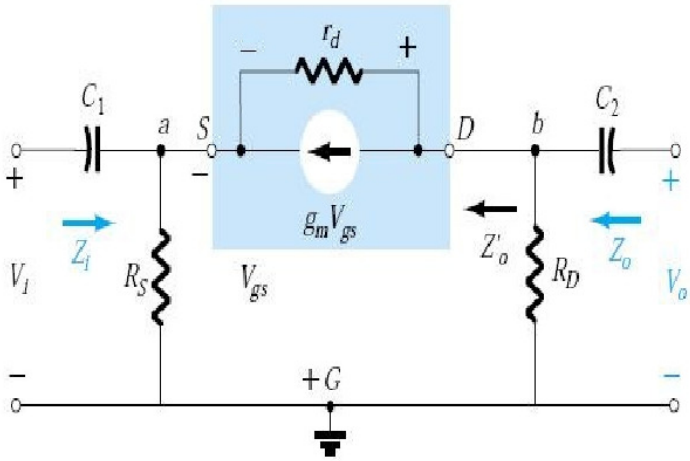
$$Zi = R_G$$

$$Zo = rd||Rs||1/gm$$

$$Av = gm(rd||Rs)/1+gm(rd||Rs)$$

5.8 COMMON-GATE CONFIGURATION





$$Zi = Rs||[(rd+R_D)/1+gmR_D]$$

$$Zo = rd||R_D$$

$$Av = [gmR_D+(R_D/rd)]/[1+(R_D/rd)]$$

Topic 6 HIGH FREQUENCY RESPONSE OF FETS AND BJTS

6.1 LOW-FREQUENCY RESPONSE — BJT AMPLIFIER

The capacitors *Cs*, *CC*, and *CE* will determine the low-frequency response.

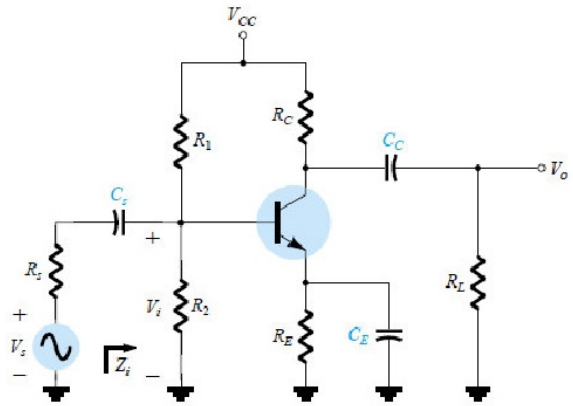


Fig. 6.1 Loaded BJT amplifier with capacitors that affect the low-frequency response

C_S :-

Since *Cs* is normally connected between the applied source and the active device, the general form of the *R-C* configuration is established by the network of Fig. 7.2. The total resistance is now*Rs +Ri*.

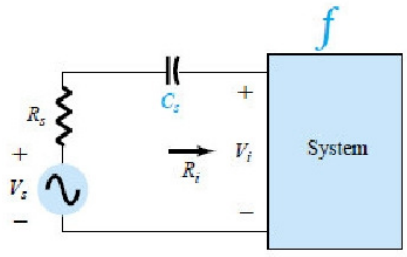


Fig. 6.2 Determining the effect of *Cs* on the low frequency response

$$f_{Ls} = 1/2\pi(Rs+Ri)Cs$$

At mid or high frequencies, the reactance of the capacitor will be sufficiently small to permit a short-circuit approximation for the element. The voltage*Vi* will then be related to*Vs* by

$$Vi|mid = RiVs/(Ri+Rs)$$

At f_{LS}, the voltage Vi will be 70.7% of the value assuming that Cs is the only capacitive element controlling the low-frequency response.

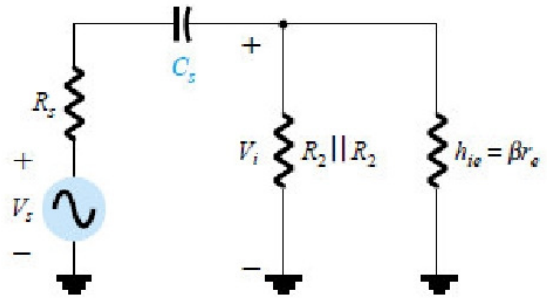


Fig. 6.3 Localized ac equivalent for Cs

$$\mathbf{Ri = R1 \| R2 \| Rs}$$

$$\mathbf{Vi = RiVs/(Rs+Ri-jXCs)}$$

C_C:-

Since the coupling capacitor is normally connected between the output of the active device and the applied load, the R-C configuration that determines the low cut-off frequency due to C_C appears in Fig. 6.4.
The total series resistance is now $Ro + R_L$ and the cut-off frequency due to C_C is determined by

$$\mathbf{f_{Lc} = 1/2\pi(Ro+R_L)C_C}$$

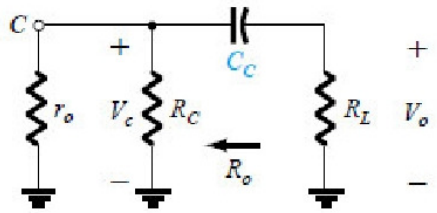


Fig. 6.5 Localized ac equivalent for C_C with Vi =0 V

Ignoring the effects of Cs and C_E, the output voltage Vo will be 70.7% of its mid-band value at f_{LC}. The resulting value for Ro=Rc||ro

C_E:-

To determinef_{LE}, the network "seen" by C_E must be determined as shown in Fig. 6.6. Once the level of *Re* is established, the cut-off frequency due to *CE* can be determined.

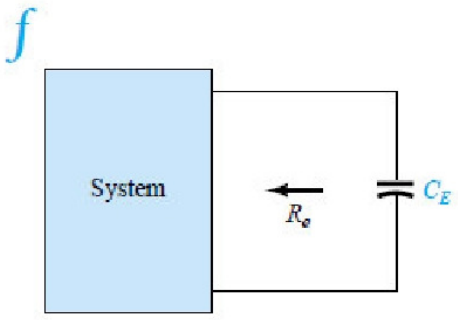


Fig. 6.6 Determining the effect of *CE* on the low-frequency response

$$\mathbf{f_{LE} = 1/2\pi ReC_E}$$

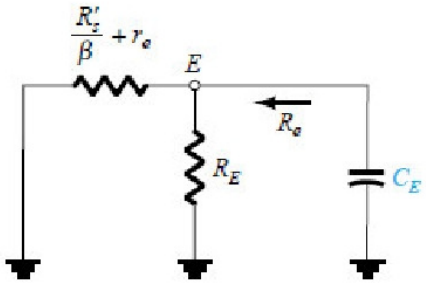


Fig. 6.7 Localized ac equivalent of C_E

$$\mathbf{Re = R_E \| (R's/\beta + re)}$$

Where, R's = R1||R2||Rs

Before continuing, keep in mind that *Cs*, C_C, and C_E will affect only the low frequency response. At the mid-band frequency level, the short-circuit equivalents for the capacitors can be inserted. Although each will affect the gain *Av* = *Vo*/*Vi* in a similar frequency range, the highest low-frequency cut-off determined by *Cs*, C_C, or C_E will have the greatest impact since it will be the last encountered before the mid-band level. If the frequencies are relatively far apart, the highest cut-off frequency will essentially determine the lower cut-off frequency for the entire system. If there are two or more "high" cut-off frequencies, the effect will be to raise the lower cut-off frequency and reduce the resulting bandwidth of the system. In other words, there is an interaction between capacitive elements that can affect the resulting low cut-off frequency.

However, if the cut-off frequencies established by each capacitor are sufficiently separated, the effect of one on the other can be ignored with a high degree of accuracy.

6.2 LOW-FREQUENCY RESPONSE — FET AMPLIFIER

The analysis of the FET amplifier in the low-frequency region will be quite similar to that of the BJT amplifier. There are again three capacitors of primary concern C_G, C_C, and C_S.

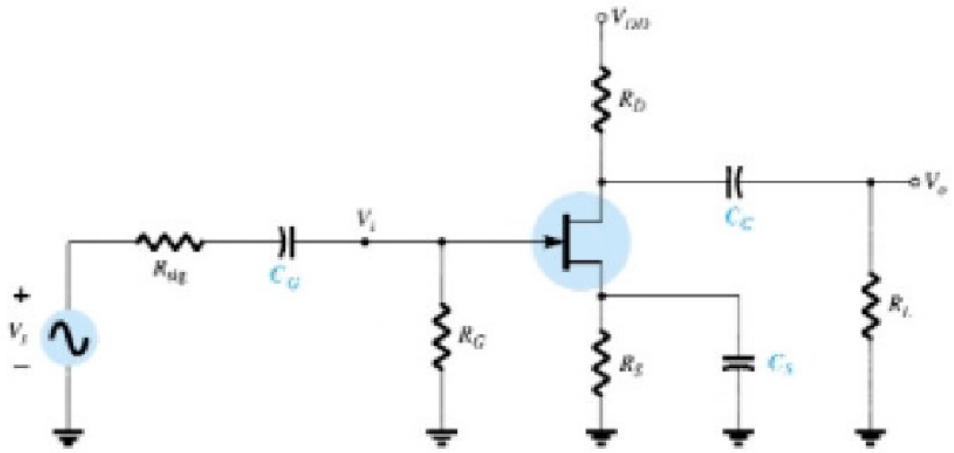


Fig. 6.8 Capacitive elements that affect the low-frequency response of a JFET amplifier

C_G:-

For the coupling capacitor between the source and the active device, the ac equivalent network will appear as shown in Fig. 6.9. The cut-off frequency determined by C_G will be

$$\mathbf{f_{LG} = 1/2\pi(Rsig+Ri)C_G}$$

where, $Ri = R_G$

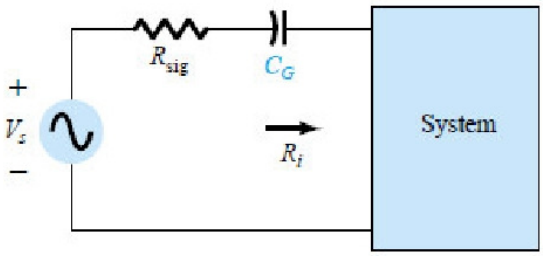


Fig. 6.9 Determining the effect of *CG* on the low-frequency response

C_C:-

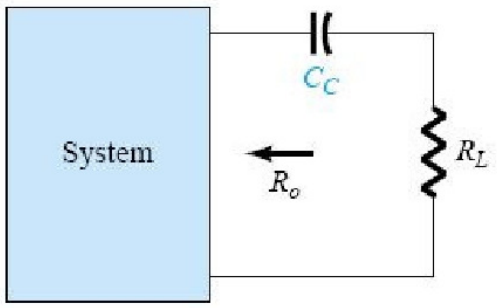


Fig. 6.10 Determining the effect of C_C on the low-frequency response.

$$\mathbf{f_{LC} = 1/2\pi(Ro+R_L)C_C}$$

$$\mathbf{Ro = rd||R_D}$$

C_S:-

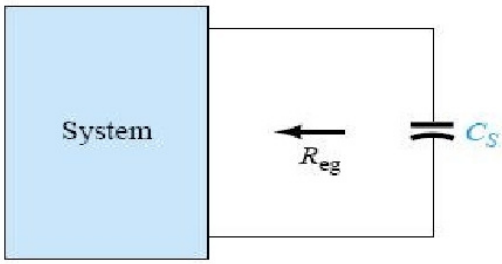


Fig. 6.11 Determining the effect of C_S on the low-frequency response.

$$\mathbf{f_{LS} = 1/2\pi ReqC_S}$$

$$\mathbf{Req = R_S/1+R_S(1+g_m r_d)/(r_d+R_D||R_L)}$$

6.3 MILLER EFFECT CAPACITANCE

In the high-frequency region, the capacitive elements of importance are the interelectrode (between terminals) capacitances internal to the active device and the wiring capacitance between leads of the network. The large capacitors of the network that controlled the low-frequency response have all been replaced by their short-circuit equivalent due to their very low reactance levels.

For *inverting* amplifiers (phase shift of 180° between input and output resulting in a negative value for *Av*), the input and output capacitance is increased by a capacitance level sensitive to the interelectrode capacitance between the input and output terminals of the device and the gain of the amplifier.

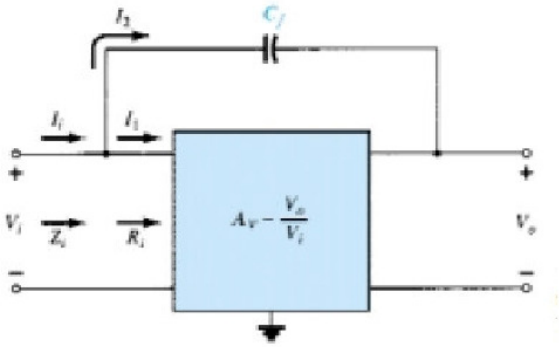


Fig. 6.12 Network employed in the derivation of an equation for the Miller input capacitance

$$\frac{1}{Z_i} = \frac{1}{R_i} + \frac{1}{X_{C_M}}$$

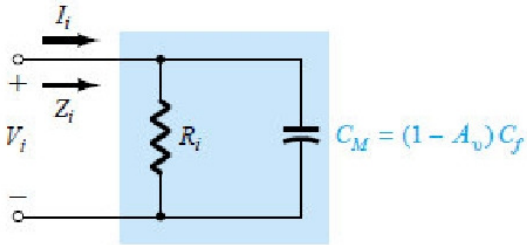


Fig. 6.13 Demonstrating the impact of the Miller effect capacitance.

In general, therefore, the Miller effect input capacitance is defined by

$$\boldsymbol{C_{Mi} = (1 - Av)C_f}$$

This shows us that:

For any inverting amplifier, the input capacitance will be increased by a Miller effect capacitance sensitive to the gain of the amplifier and the interelectrode capacitance connected between the input and output terminals of the active device.

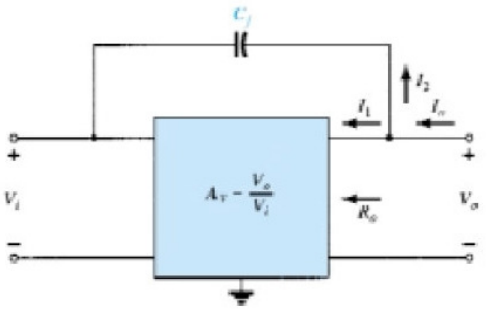


Fig. 6.13 Network employed in the derivation of an equation for the Miller output capacitance

$$\mathbf{C_{Mo} = (1- 1/Av)C_f}$$