



ANJUMAN-I-ISLAM'S
KALSEKAR TECHNICAL CAMPUS, NEW PANVEL
School of Engineering & Technology

Subject: SOOAD

Date: _____

Marks: 20

Duration: 1 Hr/s

Class: TE

Branch: CO

Instructions:

1. Attending Q1. is compulsory.
2. Compulsory attempt Q2 and Q3.
3. Attempt any one from Q2 and Q3.

Q1. Attempt any 5 from following. (2 X 5)

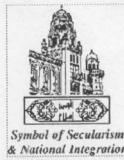
- a) What is a deployment diagram?
- b) What are the characteristics of good software design?
- c) Define fork and join.
- d) Draw and explain in short symmetric and asymmetric encryption techniques.
- e) What is mean by **State** in state diagram, draw notation of Advanced State.
- f) What is a Cohesion? List out its types.

Q2. Attempt any 1 (1 X 5)

- a) Write a Short Note on : Digital Signature
- b) What is a Coupling? Explain its types.

Q3. Attempt any 1 (1 X 5)

- a) Draw component diagram and deployment for online shopping web application.
- b) Draw activity diagram with swim lanes for adding goods into the cart.



**ANJUMAN-I-ISLAM'S
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Subject: OS

Date: / /2016

Marks: 20

Duration: 1 Hr

Class: TE

Branch: Computer

Instructions: All Questions are compulsory.

Q.1 Answer any 5 questions out of 6 (Each carry 2 marks)

(10M)

i) List out various File allocation Techniques.

ii) Differentiate between monolithic and micro kernel.

iii) What is the effect of page size on performance?

iv) Draw Process state diagram of UNIX OS.

v) What is Demand paging?

vi) Choose the correct option

a) A memory page containing a heavily used variable that was initialized very early and is in constant use is removed, then the page replacement algorithm used is:

1)LRU

2)FIFO

3) Optimal

4)LFU

b) Which one of the following address is generated by CPU.

1) Physical

2)Logical

3)Real

4)None

Q.2 Answer any one question.

(5M)

i) Explain various IO buffering technique.

ii) Explain Various File allocation Techniques.

Q.3 Solve any one Numerical.

(5M)

i) Implement LRU, Optimal and FIFO for the following Sequence
0, 1, 2, 4, 3, 7, 1, 4, 2, 3, Also calculate Hits and Faults.

ii) Assume that the disk head is initially positioned over track 100. For the disk space request of 27, 129, 110, 186, 147, 41, 10, 64 and 120. Show how the disk scheduling is done for SSTF and CSCAN.



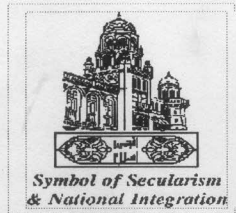
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Subject: CN
Marks: 20
Class: TE

Date: _____
Duration: 1 Hr/s
Branch: COMPUTER

Instructions: 1) Question No.1 is compulsory.
2) Assume suitable data wherever necessary.

- Q. 1) Define Attempt any 5 : (10)**
- a) ARP
 - b) Classes of IP Addresses (with range).
 - c) Subnetting and Supernetting
 - d) Piggy backing
 - e) Hamming distance
 - f) TCP and UDP
- Q. 2) A) Explain Classless Inter Domain Routing (CIDR). (5)**
OR
B) Why there is a need for congestion control? What are the different mechanisms? Explain them. (5)
- Q. 3) A) Explain how TCP handles error control and flow control. (5)**
OR
B) What are different types of routing ? Explain Distance Vector routing. (5)



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School of Engineering & Technology

Subject: MP
Marks: 20
Class: TECO

Date: 24/10/2016
Duration: 1 Hr/s
Branch: Computer

UT - II

Instructions:- Q-1 is Compulsory.

Q-1 Solve any 5.

- i) Explain in brief integer pipeline stages of PENTIUM processor. 2
- ii) Draw block diagram of Intel - PENTIUM processor. 2
- iii) Draw diag. of μ p-8086 operating in maximum mode. 2
- iv) Draw On-chip code cache memory organization of PENTIUM processor. 2
- v) Explain in brief integer data types supported by SPARC processor. 2
- vi) List out rules of instruction pairing in U-pipe & V-pipe. 2

Q-2 Attempt any one .

- i) Explain in brief dynamic branch prediction mechanism of PENTIUM processor. 5
- ii) Differentiate Intel's Core i3, i5 , i7 processor. (any 5 points) 5

Q-3 Attempt any one ,

- i) Explain in brief internal Architecture of Super SPARC processor (any 5 blocks). 5
- ii) Compare between Pentium processors P2 , P3 , P4. (any 5 points) 5