# Design of 4-bit Flash ADC

A Project Dissertation

Submitted in partial fulfillment of the requirement of

**University of Mumbai**

For the Degree of

**Bachelor of Engineering**
**(Electronics and Telecommunication Engineering)**

by

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**(13ET25)**

Under the guidance of

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in
**Electronics and Telecommunication Engineering**
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Head of Department

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# Abstract

This project presents design of low power comparator and low power encoder for 4 bit flash ADC. A 4 bit Flash ADC required 15 comparators and a thermometer code to binary code encoder. The major issue in the design of Flash ADC is the large power consumption due to the large number of comparators used. So in order to reduce the power consumption of Flash ADC, we have to design a comparator with very low power consumption. Different comparators are designed and their power consumptions are observed. The comparator with lowest power consumption is selected. Encoder is design with XOR gate. Both comparator and encoder are designed and simulated in CMOS 90nm technology. The schematic of the all circuits are design with LtSpice and DSCH3. Microwind software is used to design the layout. These designs have been also tested in CMOS 65nm and 45nm technology. Comparators and encoder have better stability and power consumption is less.

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# CHAPTER 1

# INTRODUCTION

## 1.1 OVERVIEW

The development in the digital signal processor field is rapid due to the advancement in the integrated circuit technology over the last decade. Moreover, advantage of digital processing is that it is more immune to noise. So analog-to-digital converter plays an interface role in between analog signal and digital signal processing system. The continuous speed enhancement of the wireless communication systems have bring out huge demands in speed and power specifications of high speed low resolution analog-to-digital converters.

In reality, digital signal has the benefits of effortless processing, testing and storage. So we convert the analog signal to the digital signal for processing. The way to implement this is with the help of analog-to-digital converter as the interface. Researchers are exploring new design techniques for an ADC with the aim of drop off power consumption and to enhance the speed of operation. In all the other types of ADCs, flash ADC design turns out to be more significant as a result of the reality that it frequently plays a crucial role in other types of ADCs such as multi bit sigma delta ADC and pipelined ADC.

Over the years, improvement of digital integrated circuit has strongly followed Moore's Law. As a result, transistor size has significantly reduced in size and the speed of digital circuit has been exponentially boosted. This trend broadens the gap between the digital circuit and its analog counterpart, for which the technology progress is not as beneficial. On one hand, there exists high speed digital circuit with its ever growing processing power and efficiency. On the other hand, analog circuit struggles and largely falls short to maintain pace. Most of systems require communication with the real analog world at some point or other. For that purpose analog interface circuit, is a crucial factor in the whole system. It is attractive to push the analog digital border nearer to the real world, where the system can acquire enhanced advantage of the high speed digital circuit. This development places high pressure on analog circuit designers to build up very high speed interface circuits, analog-to- digital and digital to analog converters (ADCs and DACs) that can sustain with the digital world by maintaining other desirable attributes like small chip area and low power consumption.

## 1.2 OBJECTIVES

The main objectives of this project are

- To inspect ADC architecture and identify its requirement and specification of an ADC for the application.
- Design and implement a low power CMOS comparator for the specific application.
- Develop and implement a XOR gate based encoder which converts thermometer code to binary code in flash ADC.
- Implement a high speed ADC for the application by combining resistor ladder, comparators and encoder.
- Analyse and compare the results with other types of similar ADCs.

# 1.3 ANALOG TO DIGITAL CONVERTERS

Analog-to-Digital converters (ADC) translate analog signals, real world signals like temperature, pressure, voltage, current, distance, or light intensity, into a digital representation of that signal. This digital representation can then be processed, manipulated, computed, transmitted or stored. In many cases, the analog to digital conversion process is just one step within a larger measurement and control loop where digitized data is processed and then reconverted back to analog signals to drive external transducers. These transducers can include things like motors, heaters and acoustic divers like loudspeakers. The performance required of the ADC will reflect the performance goals of the measurement and control loop. ADC performance needs will also reflect the capabilities and requirements of the other signal processing elements in the loop.

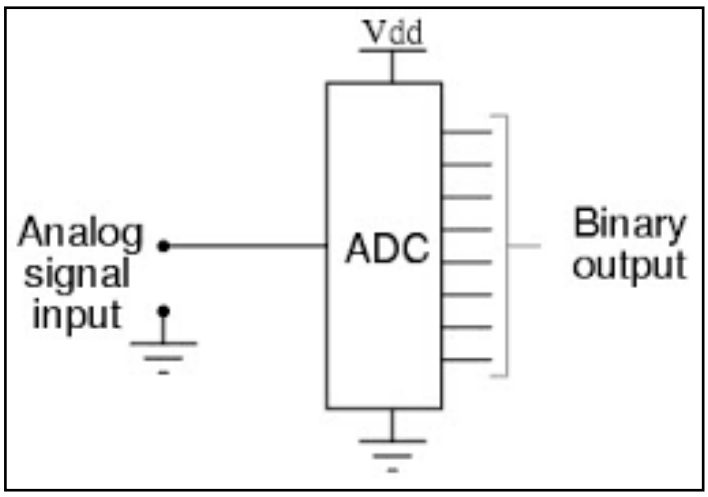


Fig. 1.1 Analog to Digital Converter

There are several different types of ADCs available, depending on the type of application. They are usually classified into three main categories depending on their speed of operation. The three types of ADCs are low speed /serial ADC, medium speed ADC and high speed ADC. Typically the serial ADCs have very high resolution which means they support high accuracy whereas high speed ADCs operate at very high frequencies but have relatively low resolution.

## 1.4 TYPES OF ADC

| Parameters | Flash ADC | Pipeline ADC | SAR ADC | Sigma-Delta ADC | Dual-slope ADC |
|---|---|---|---|---|---|
| Selection of ADC | High speed and low resolution | Medium speed and medium resolution | Low speed and medium resolution | Medium speed and high resolution | Lo bandwidth and high resolution |
| Conversion method | Parallel conversion with $2^{n-1}$ comparators | Serial conversion | Binary search algorithm is used | Conversion with integrator, comparator and single bit DAC | Conversion with integrtor and comparator |
| Encoding method | Thermometer to binary code encoder | Digital correction logic | Successive approximation | Digital filter | Analog intergration |
| Optimum Resolution | 4 to 8 bits | 12 to 16 bits | 10 to 16 bits | 14 to 20 bits | 16 bits |
| Disadvantages | Large die size and high power consumption | Cannot be used in high speed applications | Requirement of anti-aliasing factor | Higher order DAC is required for high bit ADC | Slow conversion rate |

Table 1.1 Comparison of ADC Architectures

# 1.5 CMOS TECHNOLOGY

## 1.5.1 BASICS CMOS CONCEPTS

Ideally, a transistor behaves like a switch. For NMOS transistors, if the input is a 1 the switch is on, otherwise it is off. On the other hand, for the PMOS, if the input is 0 the transistor is on, otherwise the transistor is off. Here is a graphical representation of these facts:

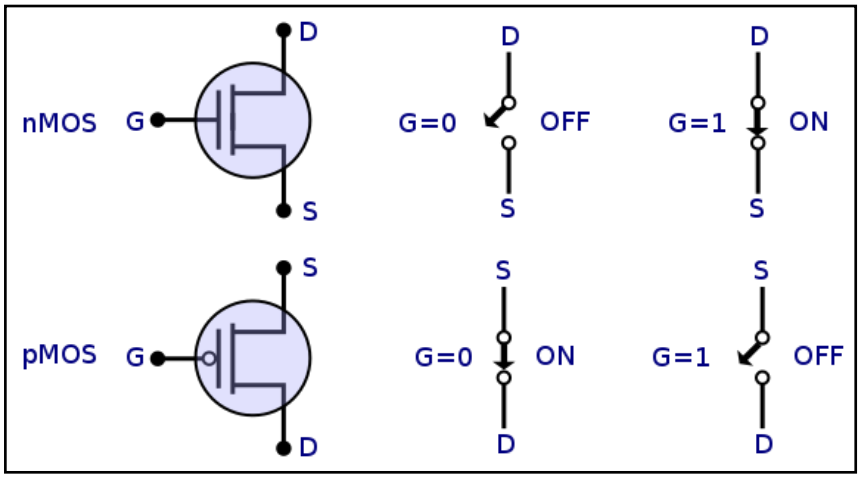


Fig. 1.2 NMOS and PMOS

When a circuit contains both NMOS and PMOS transistors we say it is implemented in CMOS (Complementary MOS)

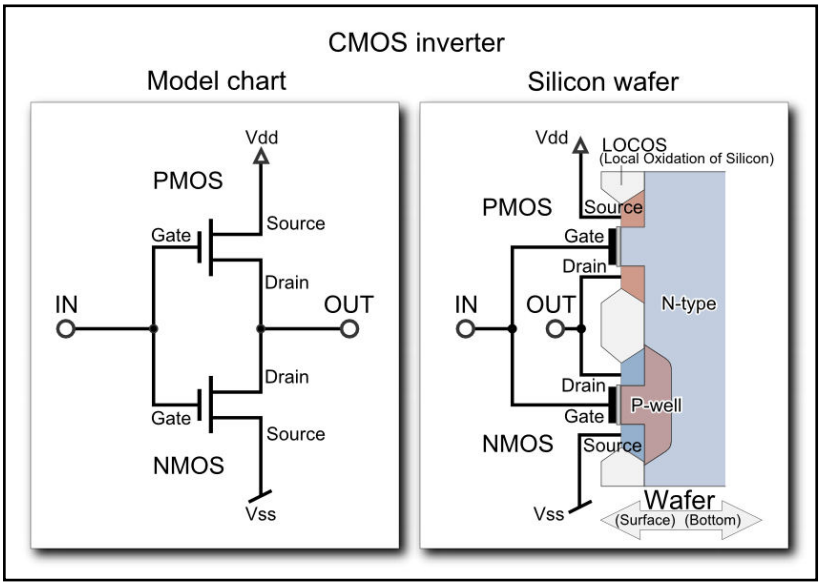


Fig. 1.3 CMOS

## 1.5.2 DRAIN CURRENT EQUATION

The linear model describes the behavior of a MOSFET biased with a small drain-to-source voltage. As the name suggests, the linear model, describes the MOSFET acting as a linear device. More specifically, it can be modeled as a linear resistor whose resistance is modulated by the gate-to-source voltage. In this regime, the MOSFET can be used as a switch for analog and digital signals or as an analog multiplier.

The general expression for the drain current equals the total charge in the inversion layer divided by the time the carriers need to flow from the source to the drain:

$$I_D = -\frac{Q_{inv} WL}{t_r} \tag{1}$$

where $Q_{\text{inv}}$ is the inversion layer charge per unit area, $W$ is the gate width, $L$ is the gate length and $t_{\text{r}}$ is the transit time. If the velocity of the carriers is constant between source and drain, the transit time equals:

$$t_r = \frac{L}{v} \tag{2}$$

where the velocity, $v$, equals the product of the mobility and the electric field:

$$v = \mu \mathcal{E} = \mu \frac{V_{DS}}{L} \tag{3}$$

The constant velocity also implies a constant electric field so that the field equals the drain-source voltage divided by the gate length. This leads to the following expression for the drain current:

$$I_D = -\mu Q_{inv} \cdot \frac{W}{L} \cdot V_{DS} \tag{4}$$

We now assume that the charge density in the inversion layer is constant between source and drain. We also assume that the basic assumption described in section 2 applies, namely that the charge density in the inversion layer equals minus the product of the capacitance per unit area and the gate-to-source voltage minus the threshold voltage:

$$Q_{inv} = -C_{ox}(V_{GS} - V_T), \text{for } V_{GS} > V_T \tag{5}$$

The inversion layer charge is zero if the gate voltage is lower than the threshold voltage. Replacing the inversion layer charge density in the expression for the drain current yields the linear model:

$$I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T)V_{DS}, \text{for } |V_{DS}| << (V_{GS} - V_T) \quad (6)$$

Note that the capacitance in the above equations is the gate oxide capacitance per unit area. Also note that the drain current is zero if the gate-to-source voltage is less than the threshold voltage. The linear model is only valid if the drain-to-source voltage is much smaller than the gate-to-source voltage minus the threshold voltage. This insures that the velocity, the electric field and the inversion layer charge density is indeed constant between the source and the drain.

An example of the linear current-versus-voltage (*I-V*) characteristics of a MOSFET is shown in Fig.1.4

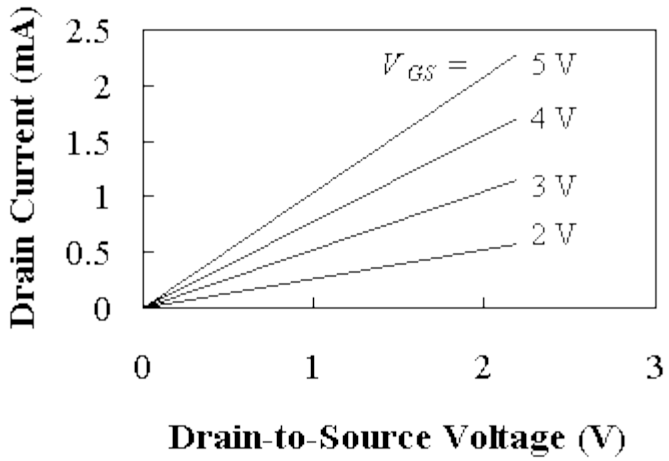


Fig. 1.4 Linear *I-V* characteristics of a MOSFET

The figure illustrates the behavior of the device in the linear regime: While there is no drain current if the gate voltage is less than the threshold voltage, the current increases with gate voltage once it is larger than the threshold voltage. The slope of the curves equals the conductance of the device, which increases linearly with the applied gate voltage. The figure therefore illustrates the use of a MOSFET as a voltage-controlled resistor.

# Chapter 2
# LITERATURE SURVEY

## 2.1 IEEE 2016 PAPERS

**1. A Reference Voltage Interpolation-Based Calibration Method for Flash ADCs** :
In year 2016, Hsuan-Yu Chang and Ching-Yuan Yang has presented the paper on 6-bit flash ADC that uses interpolating voltage calibration. The ADC uses the digital calibration technique to both reduce power and improve linearity, so that we can overcome the inherent power versus linearity tradeoff in the ADC design the proposed ADC is of interested in high speed, lower powerapplications and is suitable for implementation for the submicrometer process.

**2. High Density Magnetic Flash ADC using Domain Wall Motion and Pre-Charge Sense Amplifiers :**
In year 2016, Yogendra Kumar Upadhyaya and Mohd. Hasan presented the paper on designing and simulation of a domain wall motion based magnetic ADC in which the comparator is realized using domain wall motion in a magnetic stripe in combination with MTJ and PCSA with high sample rate, less area and power along with non-volatility. ADC is a key building block in networking and consumer electronic products. The proposed magnetic ADC can convert not only electrical signals but also magnetic analog signals. Moreover, magnetic analog signals can be directly converted into digital contrary to traditional approach of converting a magnetic signal into an electrical signal.

**3. A Bit Swap Logic (BSL) Based Bubble Errorn Correction Method for Flash ADC :**
In year 2016, Pranati Ghoshal and Sunit Kumar Sen presented the paper onmethod that can correct either first, second or any order bubble error – the order of correction depends on the individual system need.It is seen that as the number of output bits increases, the proposed method requires lesser number of transistors.

**4. A Metastability Error Detection and Reduction Technique for Partially Active Flash ADCs:**
In year 2016, Xiaochen Yang, Guoping Cui, Yang Zhang, Jiajun Ren and Jin Liu presented a paper on metastability detection and reduction technique for PA-flash ADCs. Metastability mechanisms of the proposed comparator-based and prior logic gate-based MDs are analyzed. Because of the exponential regeneration, the proposed MD can reduce the ADC metastability rate significantly and measurement shows metastability error rate improvement from $10^{-6}$- $10^{-12}$.

**5. Design and Characterization of a 3-bit 24-GS/s Flash ADC in 28-nm Low-Power Digital CMOS :**
In year 2016, Gregor Tretter, Mohammad Mahdi Khafaji, David Fritsche, Corrado Carta, presented a paper on 3-bit single-core flash ADC in LP digital CMOS achieving sampling rates up to 24 GS/s without time interleaving. This is the result of a design that aims at the highest possible sampling rate for a single ADC core. In order to achieve this goal, the bandwidth requirements for the ADC input stages have been investigated and evaluated in the form of simple math equations for efficient circuit implementation

## 2.2 IEEE 2015 PAPERS

**6. Comparative Analysis of Low Power Novel Encoders for Flash ADC in 45nm Technology :**

In year 2015, Aditi Kar, Moushumi Das, Bipasha Nath, Durba Sarkar and Alak Majumder presented a paper on various existing encoders and proposed two new logics for encoder circuit which can be used for Flash ADC operations. The proposed architectures are simulated at various supply voltages and analyzed that outputs are quite smooth without any missing bit. After comparison of power, they have seen that both the proposed structure has outperformed the existing models of encoder and proposed binary based encoder is the best for ultra low power Flash ADC based applications.

**7.Design of a 10Gsps TI-Flash ADC with Modified Clocking Scheme :**

In year 2015, Khaled A.El-Gammal and Sameh A.Ibrahim presented a paper on high speed flash ADC with four bit resolution and sampling speed of 10Gsps. The ADC achieves low power and low FOM of 115 fJ/cs with the help of the modified clocking scheme which is also robust across PVT variations. The ENOB is greater the 3.5 bits for input frequencies till Nyquist rate. The comparator design was enhanced using two stage pre-amplifiers along with the SA-latch and SR-latch which eliminated the need for any digital calibration techniques and hence decreasing the total power of the TI-ADC.

**8. Design of 4 Bit Flash ADC using TMCC & NOR ROM Encoder in 90nm CMOS Technology :**

In year 2015,Mr. K. N. Hosur, Mr. Dariyappa, Mr. Shivanand, Mr. Vijay, Mr. Nagesha, Dr. Girish V. Attimarad, Dr. Harish. presented a paper on the 4 bit Flash ADC with 90nm CMOSTechnology. Its internal blocks like TMCC, 1 out of 15encoder and NOR ROM encoder are designed andsimulated. The main advantage of proposed architecture is that, the static power consumption is very less due to elimination of resistor ladder network. The average power consumed by this circuit is 4.43mW for input frequency of 2 MHz. The use of TMCC slightly reduces the transistor matching problem thereby providing a very low power and high speed.

**9. Design of Ultra Low Power Novel 3-Bit Flash ADC in 45nm CMOSTechnology :**

In year 2015, Moushumi Das, Bipasha Nath, Durba Sarkar, Aditi Kar and Alak Majumder presented a paper on an important issue that forces the demand for low power is the long-life battery operation. Reduction of power loss also incorporates additional functionalities on the same power budget. We have simulated our proposed model on Tanner tool V15 with 45nm technology. The designs consumes a power of 235nW and a delay of 9.8 us. The DNL curve shows that they have no missing bits in their design.

**10. A 7GS/s, 1.2 V. Pseudo logic Encoder based Flash ADC Using TIQ Technique :**

In year 2015,Liyaqat Nazir,Burhan Khurshid and Roohie Naaz Mir presented paper on a 4- bit Flash type ADC. It has a step size of 0.01300 V. The ADC uses pseudo-dynamic logic encoding network. Transient analysis simulations are carried in order to measure important performance parameter. Three main ADC parameters i.e. power consumed, highest conversion speed achieved and DNL were measured. Differential (DNL) errors measured are between -0.06283 LSB to +0.088924 LSB. The ADC consumes 1.9807 mW from a 1.2V supply.

## 2.3 PROBLEM STATEMENT

One of the major problem while designing Flash ADC is the power consumption. Flash ADC consumes more power because of large number of comparators are used. In order to reduce the power dissipation of Flash ADC, the comparator with very low power has to be design. In this project, the comparators has to be design with the power dissipation in few µW and the Flash ADC which is operating at 1V of power supply for the resolution of 4 bits with the power consumption in few mW.

# Chapter 3
# FLASH ADC

## 3.1 General Block Diagram of Flash ADC

The General block diagram for a N bit Flash ADC is given in fig. 3.1. A Flash ADC is formed of mainly three blocks- Resistor ladder, Comparator array and Thermometer to Binary code encoder. Resistor ladder is used for generating various reference voltages. The incoming analog signal is compared with these generated reference voltages using the comparator array and the corresponding thermometer code will be generated. These thermometer codes are given to the digital encoder which will convert them to the corresponding binary codes.

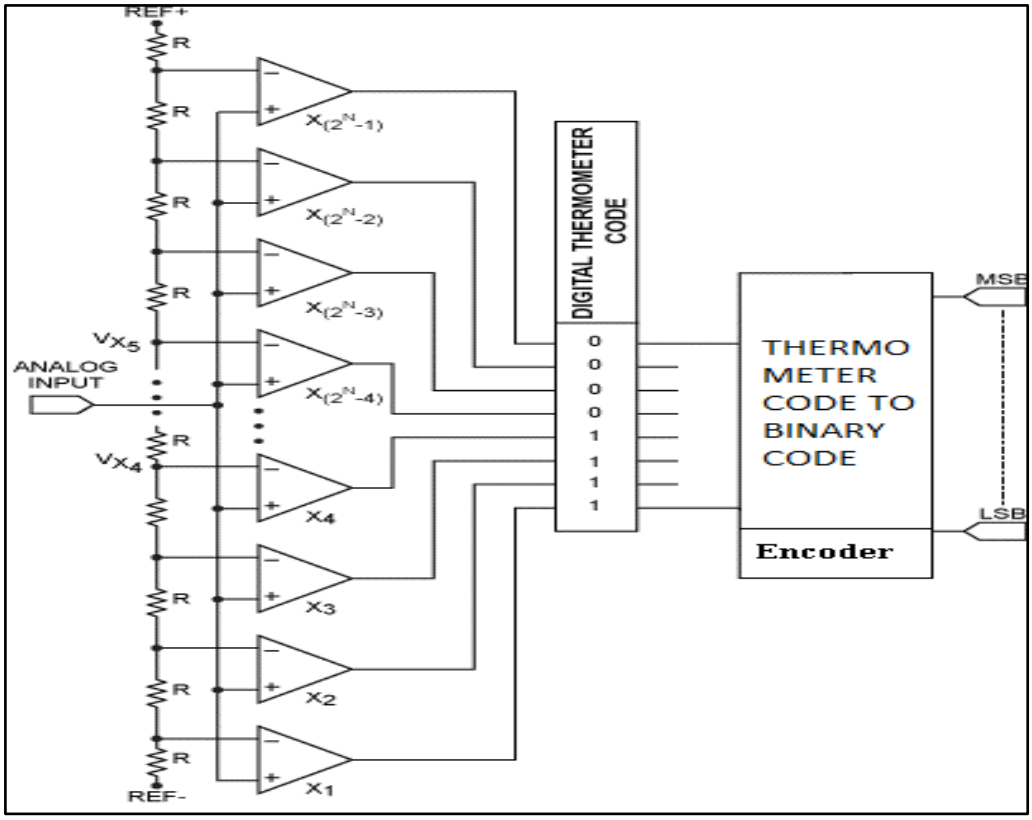


Fig.3.1 General Block Diagram of Flash ADC

Flash or parallel converters have the highest speed of any type of ADC. As seen in Fig. 3.1, they use one comparator per quantization level ($2^N$ - 1) and $2^N$ resistors (a resistor-string DAC). The reference voltage is divided into $2^N$ values, each of which is fed into a comparator. The input voltage is compared with each reference value and results in a thermometer code at the output of the comparators. A thermometer code exhibits all zeroes for each resistor level if the value of vm is less than the value on the resistor string, and ones if Vin is greater than or equal to voltage on the resistor string. A simple $2^N$ - 1 : N digital thermometer decoder circuit converts the compared data into an TV-bit digital word.

Flash ADCs have been implemented in many technologies, varying from silicon-based bipolar (BJT) and complementary metal–oxide FETs (CMOS) technologies to rarely used III-V technologies. Often this type of ADC is used as a first medium-sized analog circuit verification.

The earliest implementations consisted of a reference ladder of well matched resistors connected to a reference voltage. Each tap at the resistor ladder is used for one comparator, possibly preceded by an amplification stage, and thus generates a logical 0 or 1 depending on whether the measured voltage is above or below the reference voltage of the resistor tap. The reason to add an amplifier is twofold: it amplifies the voltage difference and therefore suppresses the comparator offset, and the kick-back noise of the comparator towards the reference ladder is also strongly suppressed. Typically designs from 4-bit up to 6-bit and sometimes 7-bit are produced.

Designs with power-saving capacitive reference ladders have been demonstrated. In addition to clocking the comparator(s), these systems also sample the reference value on the input stage. As the sampling is done at a very high rate, the leakage of the capacitors is negligible.

Recently, offset calibration has been introduced into flash ADC designs. Instead of high-precision analog circuits (which increase component size to suppress variation) comparators with relatively large offset errors are measured and adjusted. A test signal is applied, and the offset of each comparator is calibrated to below the LSB value of the ADC.

Another improvement to many flash ADCs is the inclusion of digital error correction. When the ADC is used in harsh environments or constructed from very small integrated circuit processes, there is a heightened risk that a single comparator will randomly change state resulting in a wrong code. Bubble error correction is a digital correction mechanism that prevents a comparator that has, for example, tripped high from reporting logic high if it is surrounded by comparators that are reporting logic low.

# Chapter 4
# DESIGN OF COMPARATORS

## 4.1 COMPARATORS

The comparator is a crucial part of almost all kind of analog-to-digital (ADC) converters. In todad's analog world, everything is digitized. As a result, we have to convert the analog data into digital data with the help of ADCs. A lot of research work is currently going on in the field of high speed low power ADCs. As the technology expands, with the help of small feature size processes, reduction in power consumption can be achieved. Comparators play a vital role in the design of an ADC. Speed, gain, power dissipation, offset and resolution are the important parameters of any type of comparators. The type and architecture of the comparator is having a considerable impact on the performance of the target application. Comparator block diagram is shown in Fig.4.1. The fundamental aim of the comparator is to compare an input signal (VIN) with a reference signal (VREF) and to produce an output logic low or logic high depending on whether the input signal is greater or smaller than reference. Comparator can be considered as a decision making circuit because it makes a decision based on the value of input signal and reference signal.

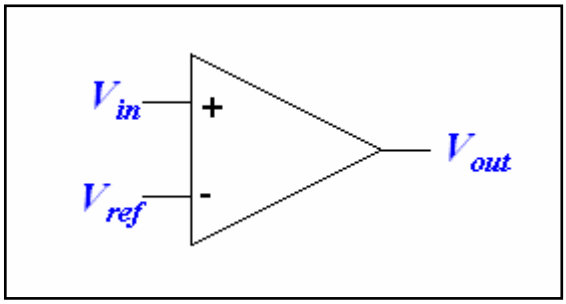


Fig.4.1 Basic block diagram of Comparator

Fig. 4.2 shows the ideal transfer characteristics of the ideal comparator. If the reference signal is above the input signal, the comparator output (VOUT) shifts to logic low and if the reference voltage is below the input signal, the output is logic high.

If VIN > VREF, VOUT = logic high

If VIN < VREF, VOUT = logic low

Comparators can be roughly classified into open-loop (continuous time) comparators and regenerative comparators. The main difference resides on whether or not feedback is applied to the op amp used. To obtain the benefits offered by both types of comparators, many configurations have been developed that employ a combination of open-loop stages with regenerative stages that use positive-feedback.

In high frequency circuits, an optimum value should be made between power dissipation and speed. Slew rate requirement is one of the important factors that influences the speed of the comparator. The comparator gain also affects the power dissipation and

speed. With the increase of power supply, the gain can be increased. But increasing the power supply beyond a specific limit is not possible for a specific technology. Generally comparators can be categorized into open loop and regenerative comparators. Open loop comparators are op-amps without compensation. Regenerative comparators make use of the positive feedback mechanism to carry out the comparator operation.

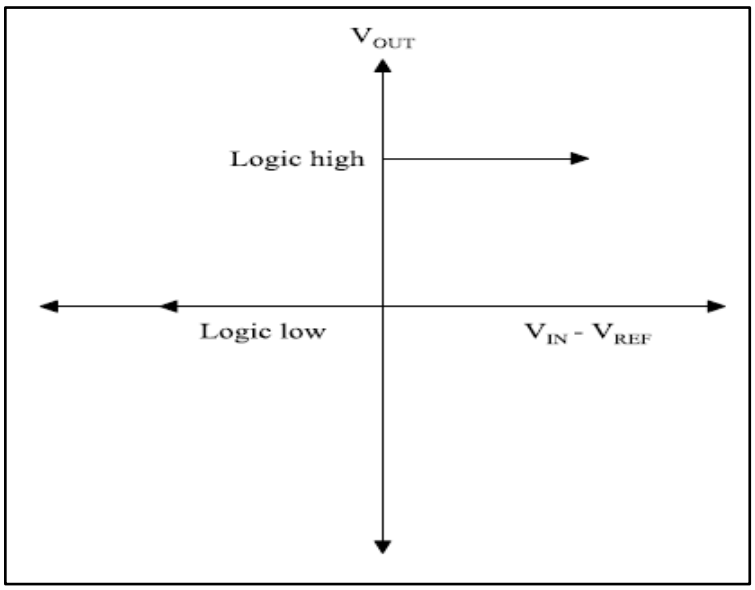


Fig.4.2 Transfer characteristics of ideal comparator

# 4.2 CHARACTERISTICS OF COMPARATORS

Comparator performance can be specified in terms of static and dynamic characteristics.

**4.2.1. Static Parameters:** The static parameters describes the performance of a comparator under DC or steady-state conditions. The main parameters are resolution, gain,offset, noise, and ICMR

.

**4.2.1.1.Resolution** is the minimum input difference that can be resolved by the comparator in order to switch between its binary states. When employed in ADCs,the resolution specification must be equal or lower than the least-significant-bit (LSB) defined by the converter.

**4.2.1.2 Gain:** The gain, Av, is one of the key limiting factors in achieving the desired resolution for the comparator.

**4.2.1.3 Offset** is defined as the minimum amount of input voltage required for the binary-state transition to take place. In a real comparator the offset adds to the minimum voltage for which the resolution was designed reducing the resolution of the circuit.

**4.2.1.4 Noise** has great influence on the operation of the comparator, thus affects the performance of an ADC. The effect of noise in the circuit's response can be seen as uncertainty in the time when the comparator's output switches between its two states.

**4.2.1.5 Input common-mode range (ICMR)** is the permissible voltage range over which the input common-mode signal can vary while all transistors remain biased in the saturation region.

**4.2.2 Dynamic characteristics**

**4.2.2.1 Propagation delay:** Propagation delay is one of the significant parameters for many applications because it limits the maximum input frequency which can be processed. Propagation delay gives an idea about the speed of the amplifier with which it responds to the applied inputs. Propagation delay is defined as the time needed for the output to attain the 50 % point of a transition after the differential input signal crosses the offset voltage, when driven by a square wave.

**4.2.2.2 Slew rate:** Propagation delay varies in accordance with the amplitude of the input. A larger input results in a smaller delay and vice versa. There is an upper limit for an input voltage above which the voltage is not be having any effect on delay. This effect is called slewing and this introduces the term slew rate. The rate of change of output voltage is called slew rate

**4.2.2.3 Settling Time** is defined as the time needed for the output to be settled within a specified percent of its final value.

## 4.3 Proposed Comparators

### 4.3.1 Differential Comparators:

Comparator is the basic building block of flash ADC as it determines the speed and accuracy of ADC. For a four bit flash ADC, fifteen comparators which operate at different threshold voltages are designed. The performance of flash ADC depends on its ability to sample the input without jitter. Therefore, clocked comparators consisting of a differential amplifier and a latch are used in this design. The clock signal given to the latch is same as the sampling clock of flash ADC.

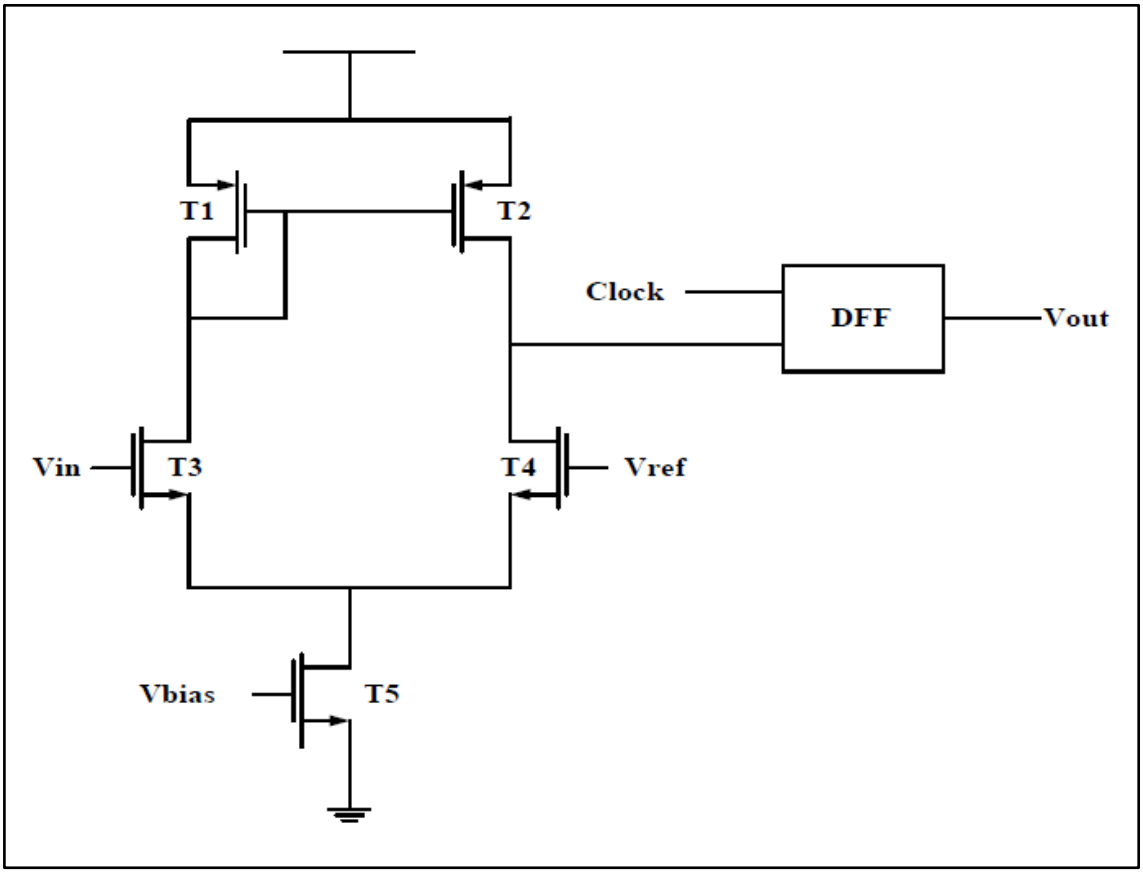


Fig. 4.3 Differential Comparator

The comparator generates a high whenever the input voltage exceeds the reference voltage. Thereby, this acts as one bit ADC. The bias voltage and the width of transistors must be chosen carefully to ensure all transistors are in saturation. The latch also ensures that the output of all comparators arrive at the same time at the input of encoder. Therefore, the outputs from comparators are in synchronization with the sampling clock.

The design of D- latch is vital as it is used in the back end of clocked comparator. Here a very high speed and low jitter D flip- flop (DFF) is designed as shown in fig. 4.4. This design makes use of only nine transistors thereby reducing the capacitance at the comparator output. The input pin Clk is connected with the sampling clock of the ADC while pin In is connected to comparator outputs.

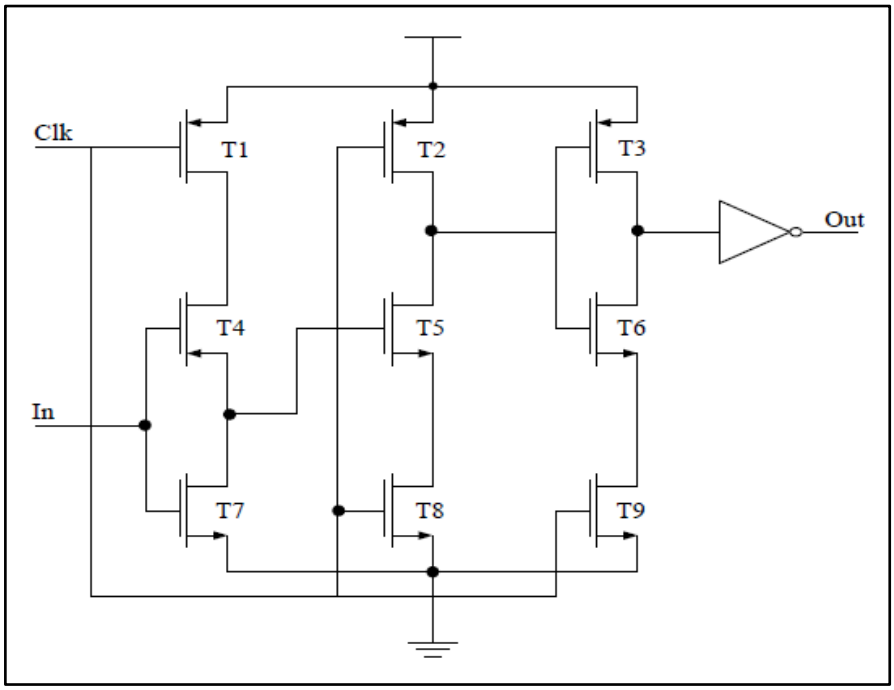

Fig. 4.4 D-flip flop

### 4.3.2 Pseudo Dynamic latched Comparators:

The proposed preamplifier consists of transistors M0 to M4. Since the input differential pair uses NMOS transistors M0 & M1, while the load transistor uses PMOS transistors M2 & M3, the gain of this preamplifier easily reach an acceptable value with small size of input differential pair. The Latch is the most sensitive part in the comparator design. It consists of two inverters connected back to back with each other forming a differential comparator and an NMOS transistor is connected between the two differential nodes of the latch. The schematic of latch consist of transistors M5 to M13 which includes cross coupled inverter pair M5-M6 & M7-M8 and the charge imbalance circuitry M9-M11. Transistors M5-M8 forms the main regenerative loop for the latch. For least capacitive effects, width and lengths of transistors M5-M8 are kept minimum and W/L ratio is kept as for an ideal inverter. Sizes are further optimized to set the meta-stable trip point of the inverter to half of the supply voltage. The switching transistor M11 short circuits the latch's differential nodes to a common DC level. An ad-vantage of increasing its width is that it brings the DC level on both nodes close to each other. Transistors M9-M10 are used to avoid the clock feed through and kickback effects from the latch to the input. Width of these transistors also affects the performance of the latch. If the width is increased, it adds to the equivalent capacitance on the nodes of the latch and increases the effect of clock feed through on the input; resulting in degradation in sensitivity of the latch. If the width is decreased, then input signal has to be increased otherwise charge imbalance on the latch is not properly created. The latch operates in two phases; reset and regeneration. In the Reset phase, the charge imbalance is created on the differential nodes of the latch proportional to the variation in the input signal. In regeneration mode, the voltage imbalance on the nodes is amplified to the rail-to-rail digital levels by the NMOS and PMOS regeneration loops.

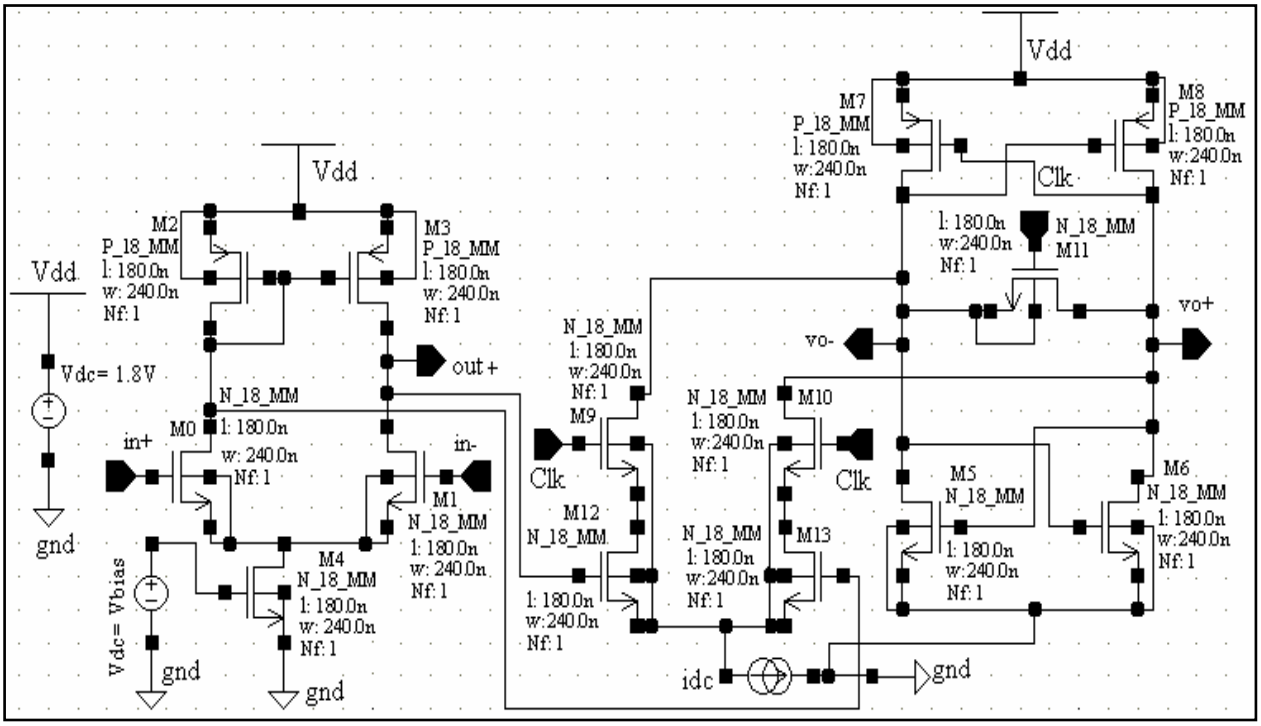


Fig. 4.5 Pseudo Dynamic Latched Comparator

When clk goes high, the amplifier is disabled and the latch is being to amplify the difference obtained at its input transistors M12-M13 to generate logic levels at the output. Fig. 4.6 shows the schematic view of the pro- posed comparator design. In the design we have used 4 transistors (two NMOS-PMOS pair) in the inverter combination. This combination reduces the parasitic capacitance and hence high comparison speed can be achieved. During the reset phase, the switching transistor short circuits the latch's outputs and the output of that point is approximately equal to 1/2 power supply. The advantage for this characteristic is that in the second phase the re- generative loop can easily shift the output to the corresponding digital levels as determined by the charge imbalance. This also increases the speed and performance of the comparator.

### 4.3.3 Open-Loop Comparators:

An open-loop comparator is an operational amplifier designed to operate with its output saturated, close to the supply rails, based on the polarity of the applied differential input. The op amp does not employ the use of feedback and hence no compensation is required to achieve stability in the system. This does not poses a problem since the linear operation is of no interest in comparator design. The main advantage of not compensating the op amp is that it can be designed to obtain the largest possible bandwidth, thereby improving its time response.

The circuit of open-loop comparator is shown in Figure 4.6. It is based on the commonly used two-stage op amp. The first stage is a NMOS differential-pair consisting of transistors M1 and M2, with PMOS transistors M3 and M4 acting as a diode-connected active load. NMOS Transistor M3 is used to bias the input pair. The output stage is a current-sink inverter consisting of transistors M5 and M6.

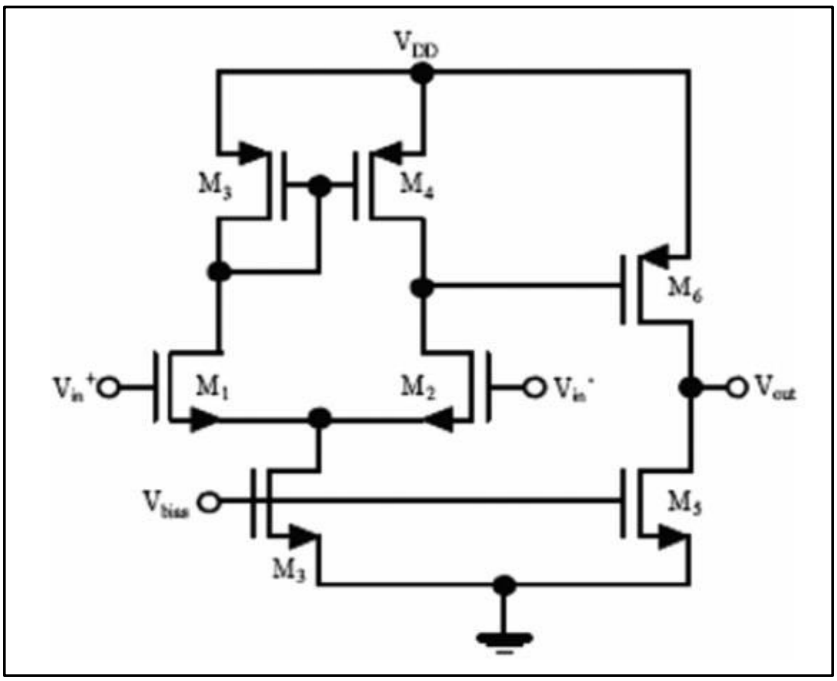


Fig. 4.6 Open-loop Comparator

### 4.3.4 Resistive Driving Comparators

Fig. 4.7 shows the structure of resistive driving latch. Transistor M3 – M6 forms a cross-coupled latch and M7 – M8 forms an input comparing circuit. As CLK is low, the circuit works in the reset mode. It is disconnected from GND by M9 while M1 – M2 is on and precharge the outputs to VDD. During this time the power consumption is only due to VDD charging the two output capacitors When CLK is high, the circuit works in the regeneration mode. M1 and M2 are cut off, and M9 is on. In this mode, the circuit can compare the input voltages by using input transistors operated in the triode region.

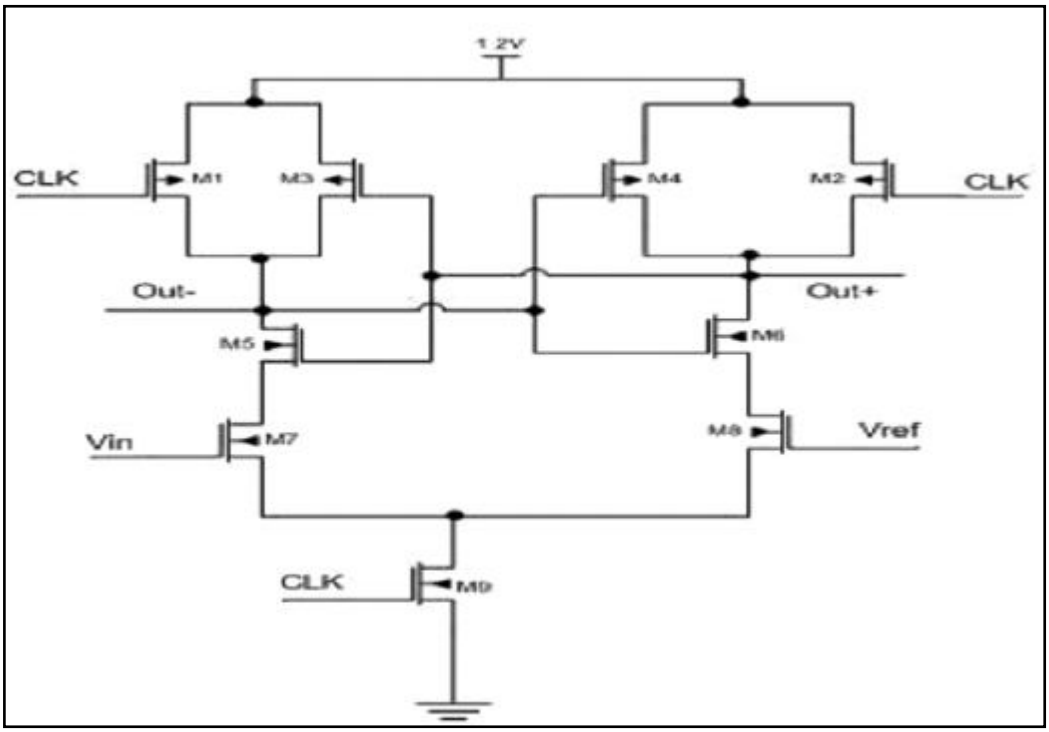


Fig. 4.7 Resistive Driving Comparator

The comparing circuit which can be model has values of resistors R1 and R2 can be described in the equations. Assume that WA = W7 and WB = W8 and Vtn is the threshold voltage of the NMOS transistor. If Vin = 1 and Vref = 0 then node Out-will try to discharge through M5 and M7 but the transistor M3 try to charge up node Out. Therefore it is very important to make transistor M3 and M4 very weak as compared to M5, M7 and M6, M8, so that the output will discharge very fast and the propagation delay will decrease.

# Chapter 5

# DESIGN OF ENCODERS

## 5.1 INTRODUCTION

Flash ADC is one of the fastest methods to convert analog information into digital information. Flash ADCS are highly used in applications where large bandwidth is required such as radar processing, sampling oscilloscopes, data acquisition and satellite communication applications. Flash ADC comprises of three parts; resistor ladder, comparator and thermometer code to binary code converter. N bit flash ADC architecture requires $2^{N-1}$ comparators for its operation. The reference voltage is generated with the help of $2^N$ equally sized resistor which constitutes resistor ladder. Since the comparators are working in parallel, flash ADC completes its conversion in one cycle. The output of the comparators is coming in a specific manner which is called thermometer code. The thermometer code is converted into binary code with the help of thermometer code to binary code conversion. The speed of the converter plays a crucial role in the design of flash ADC.

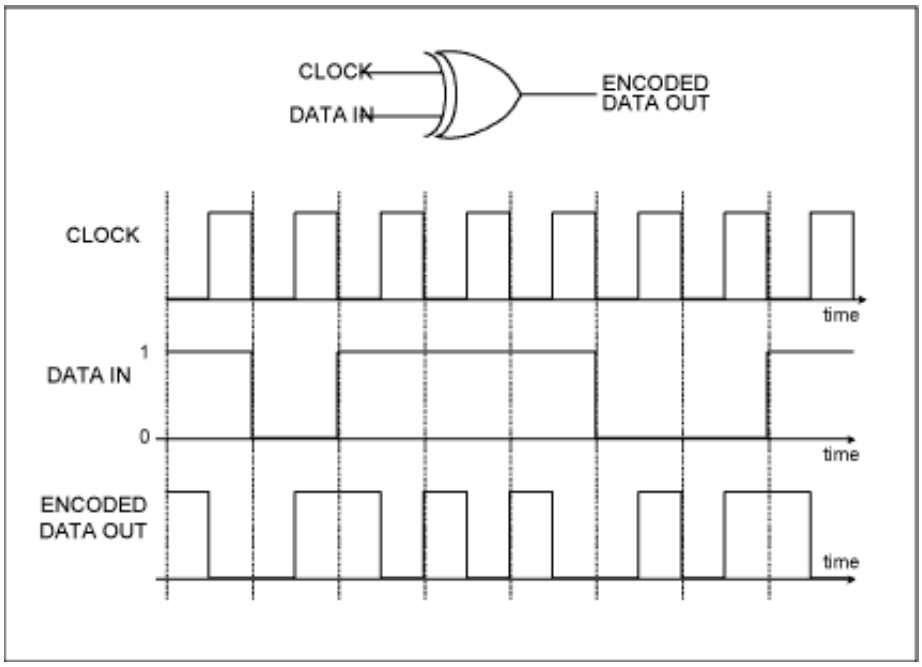


Fig. 5.1 XOR Gate

## 5.2 TYPES OF THERMOMETER TO BINARY CODE ENCODER

There are different ways with which the implementation of thermometer code to binary code conversion can be done. It includes

### 5.2.1 ROM encoder :

A standard and uncomplicated method to encode the thermometer code to binary code is to utilize ROM encoder. The ROM based method is having two stages. In the initial stage, the thermometer code is translated in to 1 out of $2^{N-1}$ code. This can be made by using array of NAND gates. The second stage is the ROM configuration which receives the 1 out of $2^{N-1}$ code as input and chooses suitable row in the ROM and generates the binary outputs.

### 5.2.2 Multiplexer based encoder :

Multiplexer based encoder needs a smaller amount of hardware and has a smaller critical path than Wallace tree encoder. The regular structure of multiplexer based encoder helps in drawing the layout easily [68, 69]. If half of the outputs in the thermometer code are logic high indicates that most significant bit (MSB) of the binary output is logic high. So MSB is the value of the thermometer output at level of 2N-1. In order to find out the value of second most significant bit, the original thermometer code is separated into two partial thermometer codes spaced by 2N-1. The encoding is done with the help of 2:1 multiplexers. The control input of the multiplexer is the previously encoded binary output. The second most significant bit is calculated with the use of two partial thermometer codes and 2:1 multiplexers. This process is sustained continuously until one 2:1 multiplexer persists. The output of the last 2:1 multiplexer is the least significant bit.

### 5.2.3 Wallace tree encoder :

Wallace tree counts the number of one‟s available in the output of the comparators. The basic building block of the Wallace tree encoder is full adder cell. The total number of full adders utilized in an encoder of N bit is $2^N - N - 1$. At the first logical level, each cell adds up the number of logical one‟s at its entries and gives an output of two bit binary code. The second stage carries out the adding of two bit words of adjacent cells to give three bit binary outputs and so on with the intention of obtaining the final binary output code for the converter.

### 5.2.4 Logic style encoder:

There are different logic styles to implement the encoder design. Generally the implementation is done using static CMOS logic style. The advantage of static CMOS logic style is that it is having the lowest power consumption with a lower speed. For achieving a higher speed, other logic styles are preferred.

### 5.2.5 XOR based encoder :

The thermometer to binary encoding is accomplished in two stages in the fat tree encoder. The first stage translates the thermometer code to 1 out of N code which means there is only single logic high is present in the code. The second stage translates the 1 out of N code to binary code with the help of multiple trees of OR. The binary bits are generated using Fat tree encoder is having a high speed of operation with less power dissipation in comparison with ROM encoder. Fat tree encoder doesn't require a clock signal or pull up resistors. Noise immunity of the fat tree encoder is higher than that of the ROM encoder.

## 5.3 PROPOSED ENCODER :

The logic function for the encoder is reconstruct to reduce wire critical path ,crossings and delays, in this encoder conversion also in two stage i.e. thermometer to gray & then gray to binary to reduce the bubble error and also the meta-stability. XOR gates can be used to replace the AND/NAND gates due to the special format of the thermometer code itself.

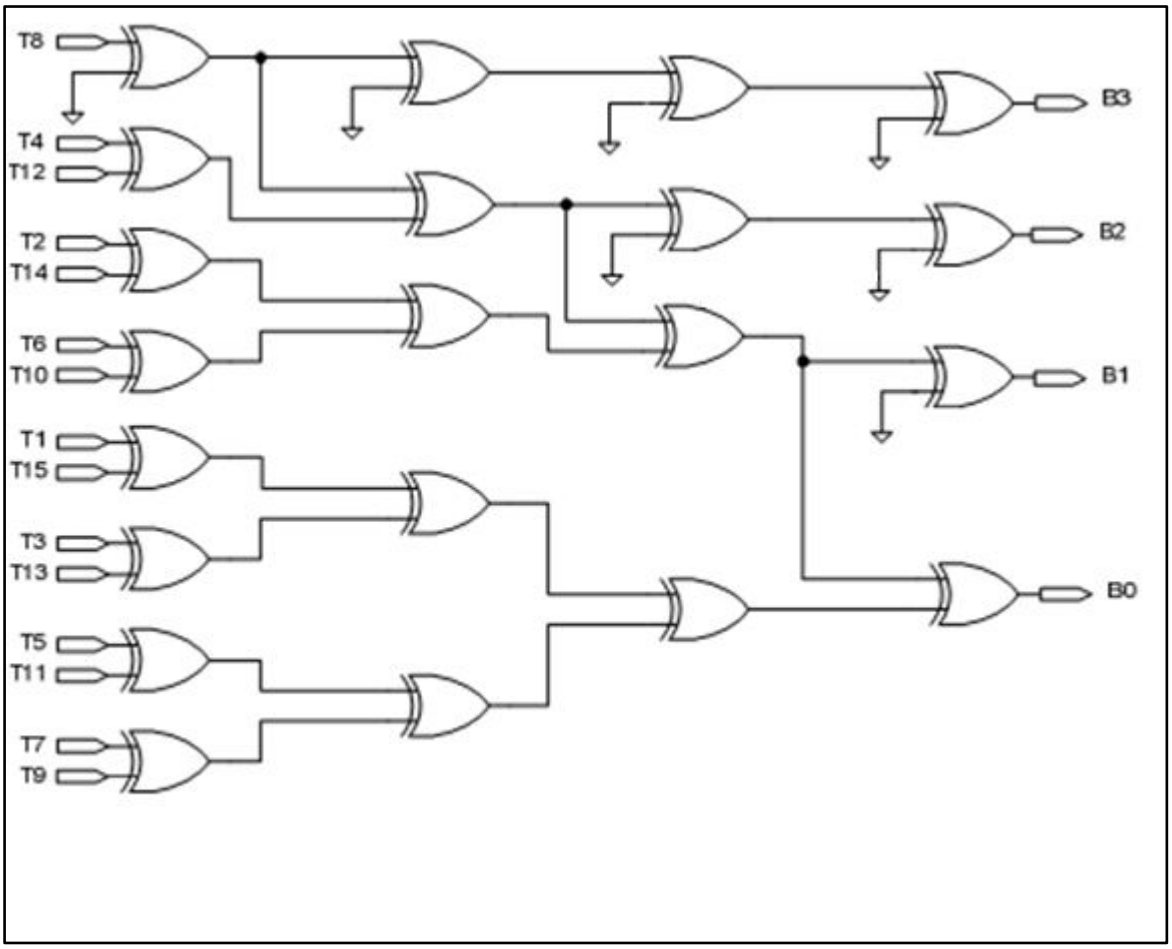


Fig. 5.2 XOR Encoder

# Chapter 6

# IMPLEMENTATION OF FLASH ADC

The previous chapters describe about different comparator and XOR based encoder for a 4 bit flash ADC. The flash ADC comprises mainly three blocks such as resistor ladder, comparators and thermometer to binary code converter. In this chapter, a 4 bit flash ADC is designed using combining the above mentioned blocks.

## 6.1 RESISTOR LADDER

The resistor ladder is designed mainly to provide a stable reference voltage to the comparators. The resistor ladder network is formed by 2N resistors which generates the reference voltage. The reference voltage for all comparator is one least significant bit (LSB) less than the reference voltage for the comparator immediately above it. The ladder divides main reference voltage into 2N equally spaced voltages

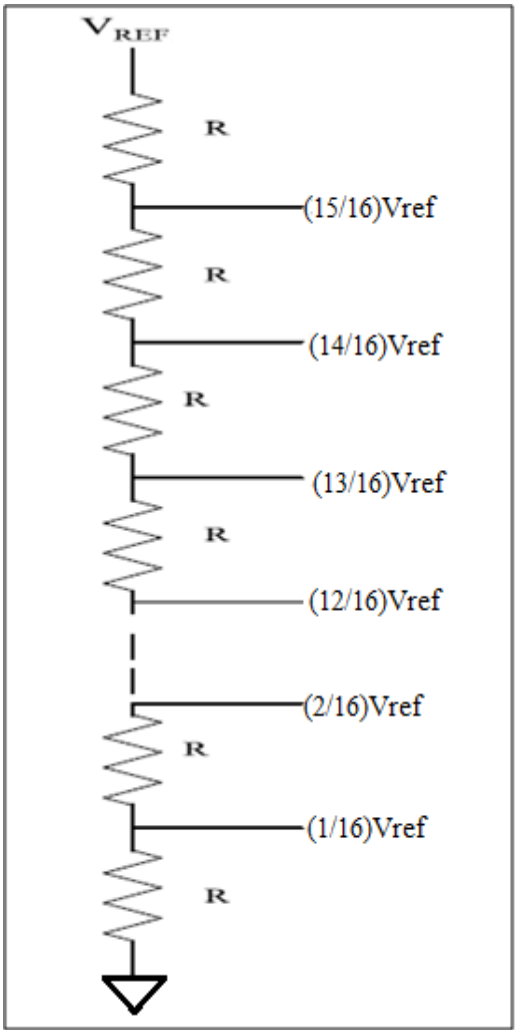


Fig. 6.1 Resistor Ladder

## 6.2 COMPARATOR

The comparator compares the input signal with the reference voltages generated by the resistor ladder. The high speed resistive driving comparator which is designed in the chapter 4 is used in the 4 bit flash ADC implementation.. The comparator dissipates a 17 μW for a 1 V supply.

## 6.3 ENCODER

High speed bubble tolerant encoder is chosen for the specific application of designing a 4 bit flash ADC due to bubble tolerance, low power dissipation. With the assist of proposed encoder, power dissipation of 0.399 mW from 1 V.

## 6.4 FLASH ADC IMPLEMENTATION

The three blocks (resistor ladder, 15 comparators and thermometer code to binary code converter) and integrated together to get the functionality of 4 bit flash ADC. The high speed 4 bit flash ADC is designed and simulated in LTspice software.

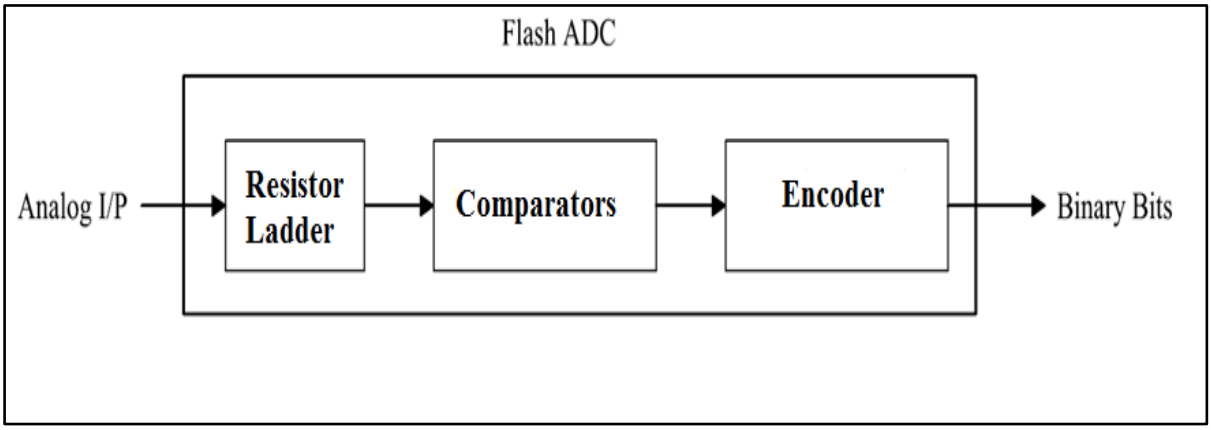


Fig. 6.2 Flash ADC

# Chapter 7

# SOFTWARE

## 7.1 DSCH3

### Introduction

The DSCH3 software is a logic editor and simulator. DSCH3 is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH3 provides a user-friendly environment for hierarchical logic design, and simulation with delay analysis, which allows the design and validation of complex logic structures. A key innovative feature is the possibility to estimate the power consumption of the circuit.

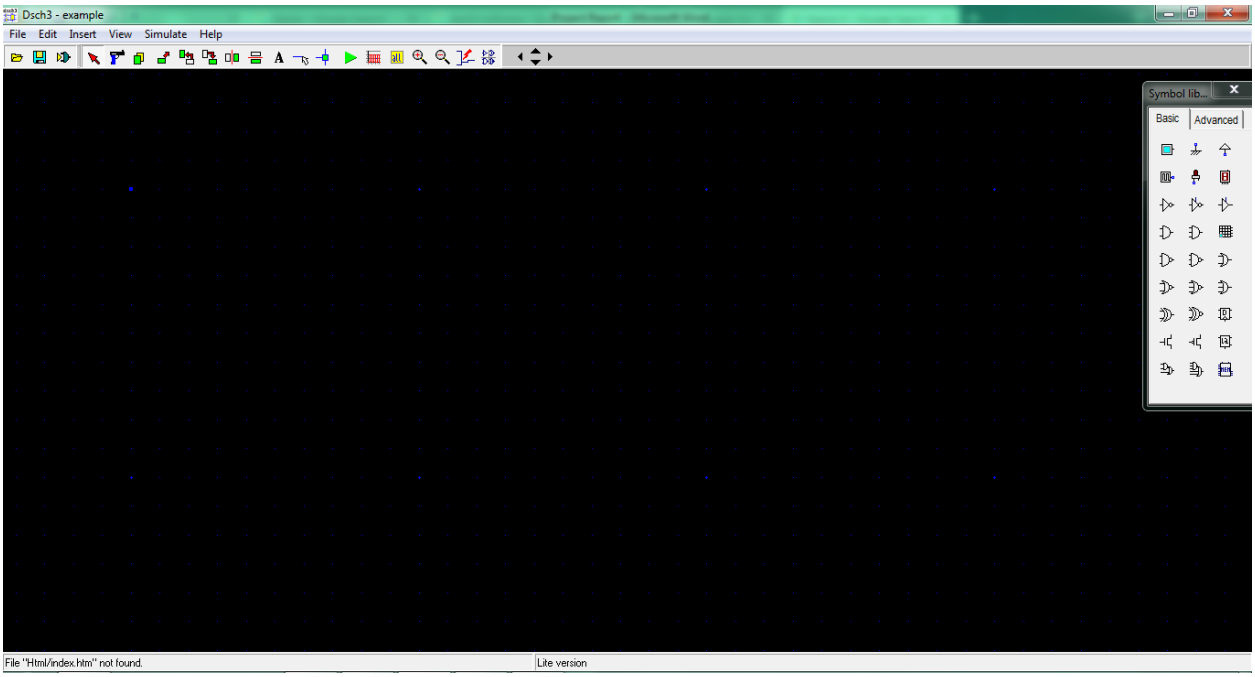


Fig.7.1 DSCH3 software

## 7.2 LTspice IV

### Introduction

LTspice is a analog circuit simulator with integrated schematic capture and waveform viewer. It was explicitly written to outperform analogous tools for sale from software companies in the interest of being used for in-house IC design as part of Linear Technology Corporation's competitive advantage as a semiconductor company. This is a reasonable strategy despite the plethora of existing commercial SPICE offerings. At least I think so, speaking from benefit of the perspective of having written physical simulators for some decades, I see the best simulators developed by the concerns that actually need them and not software companies.

Now, what is unusual about LTspice is that is it also freely distributed in the interest of allowing potential customers to simulate LTC products in a faster simulator. Further, the freely distributed version is not crippled to limit its capability in the hope that it will be useful.

This is a unique situation for a SPICE simulator and has made LTspice's popularity no less than fantastic. LTspice is overwhelmingly the most widely distributed and used SPICE program in the industry to date. It has become the de facto standard SPICE program.

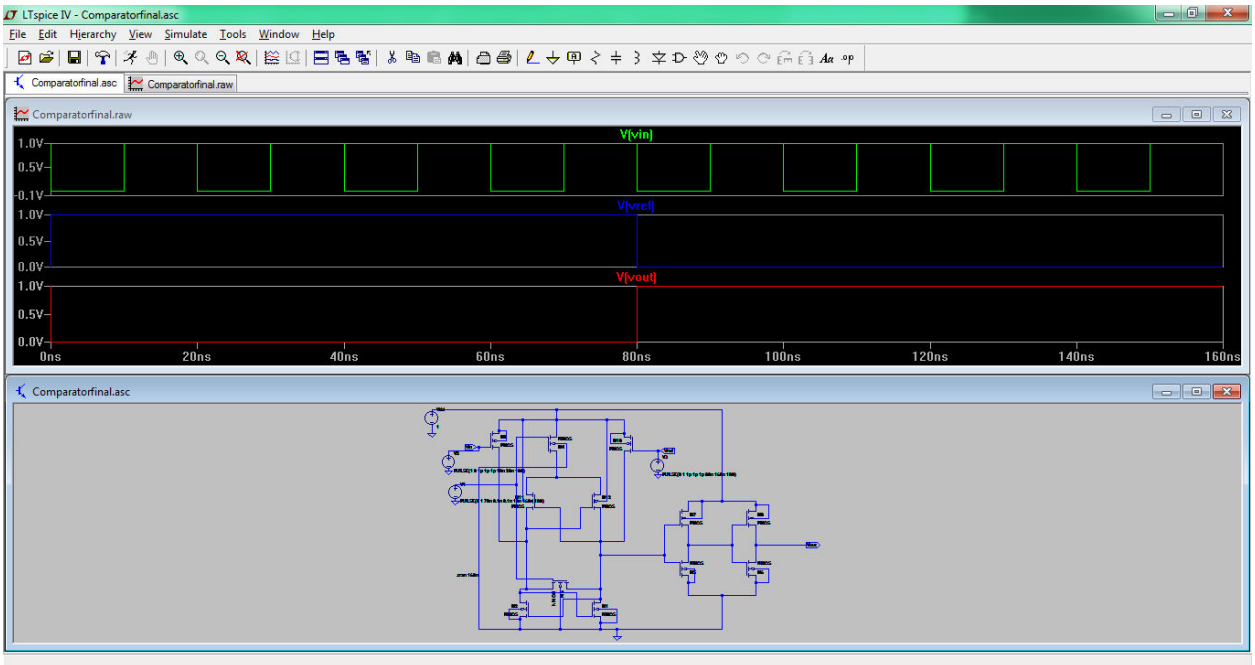


Fig.7.2 LTspice software

# 7.3 MICROWIND3

## Introduction

The MICROWIND 3 program allows the student to design and simulate an integrated circuit at physical description level. The package contains a library of common logic and analog ICs to view and simulate. MICROWIND 3 includes all the commands for a mask editor as well as original tools never gathered before in a single module (2D and 3D process view, VERILOG compiler, tutorial on MOS devices). You can gain access to Circuit Simulation by pressing one single key. The electric extraction of your circuit is automatically performed and the analog simulator produces voltage and current curves immediately

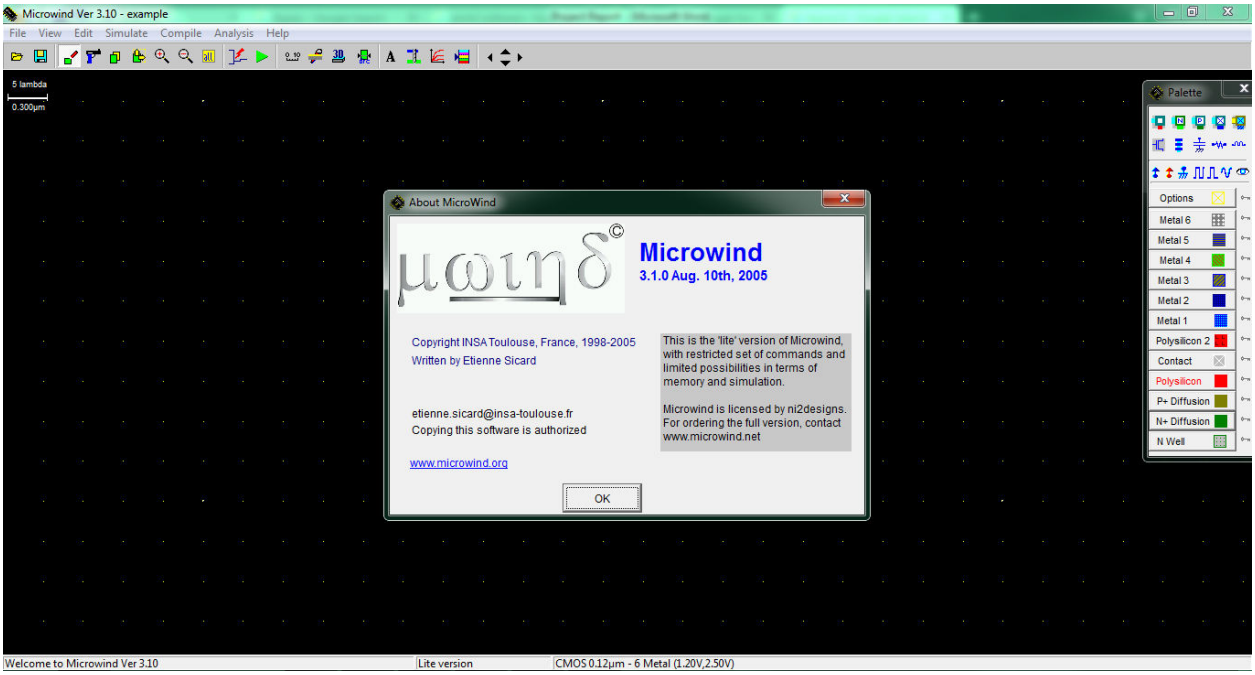


Fig.7.3 Microwind software

# Chapter 8

# SIMULATION RESULTS

## 8.1 COMPARATORS

### 8.1.1 Differential Comparator

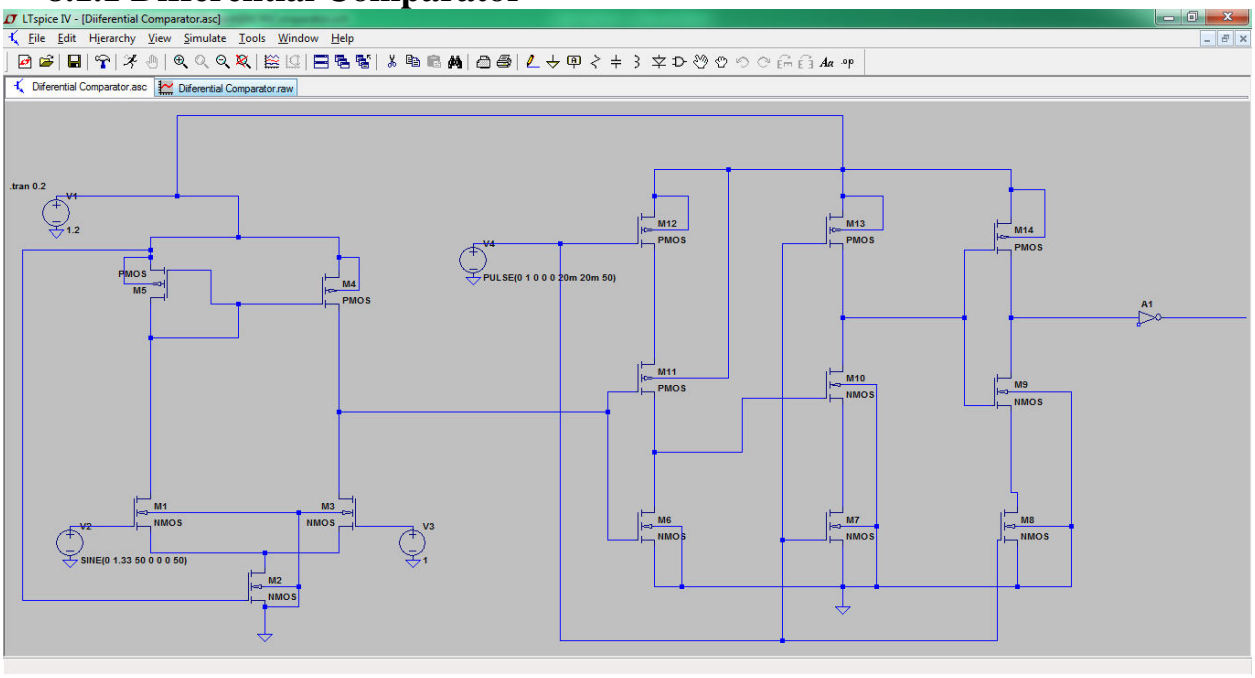


Fig. 8.1 Schematic of Differential Comparator

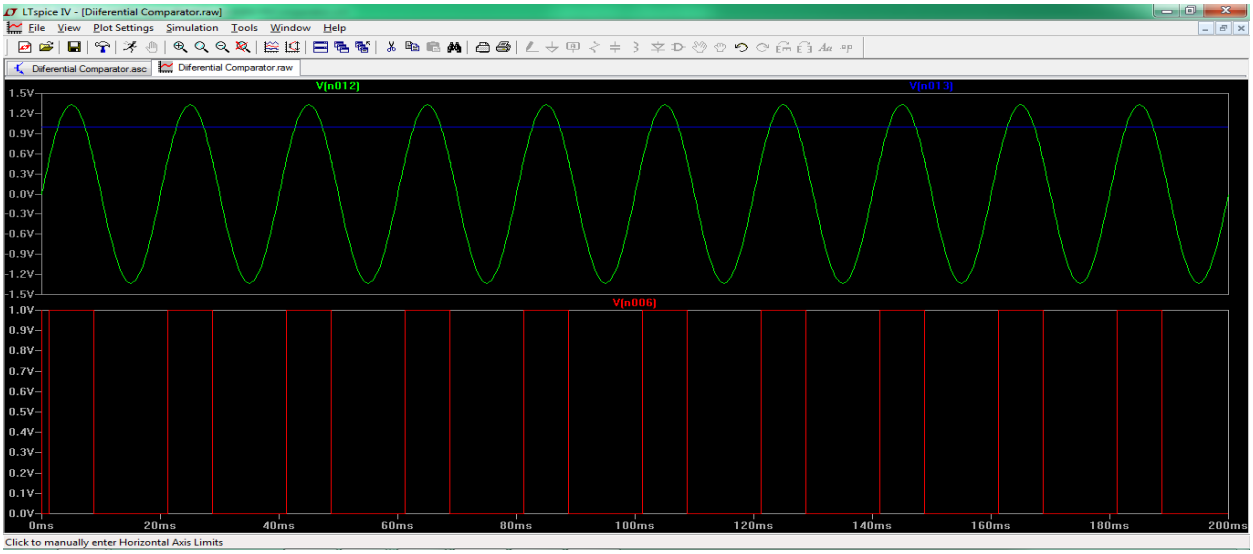


Fig. 8.2 Simulation of Differential Comparator

## 8.1.2 PSEUDO DYNAMIC LATCHED COMPARATOR

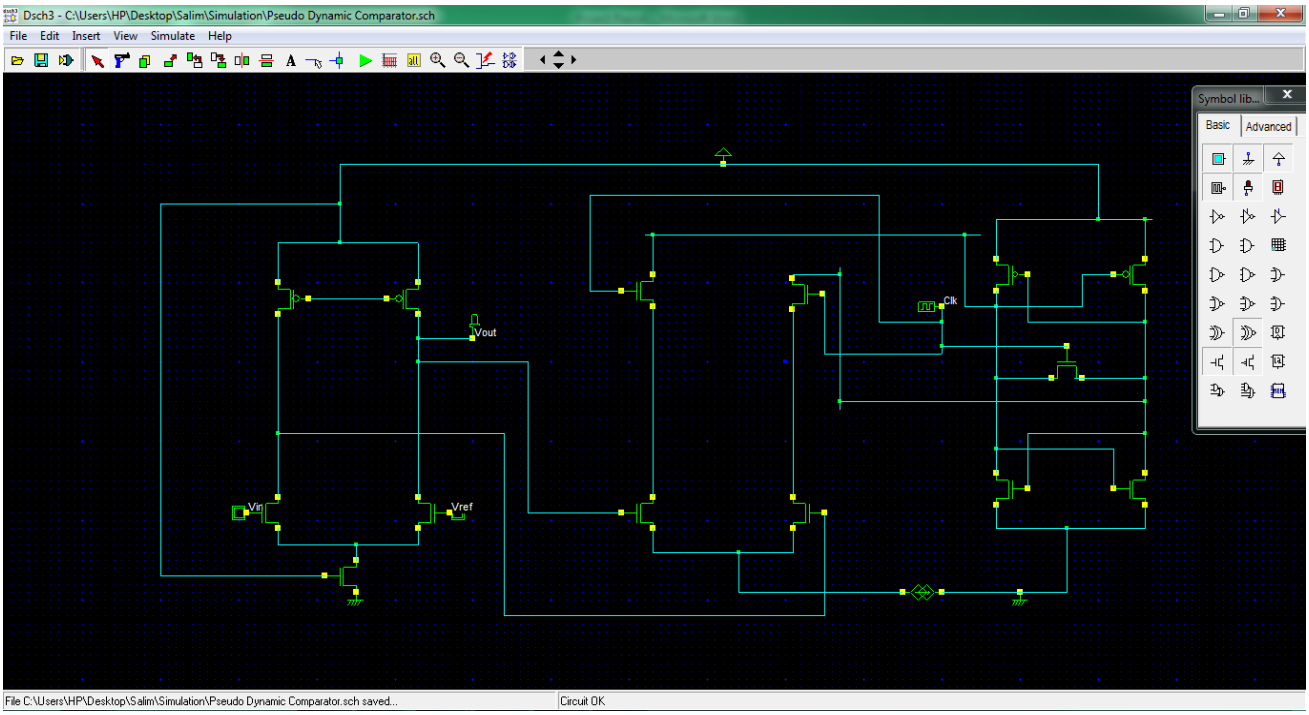


Fig.8.3 Schematic of Pseudo Dynamic Latched Comparator

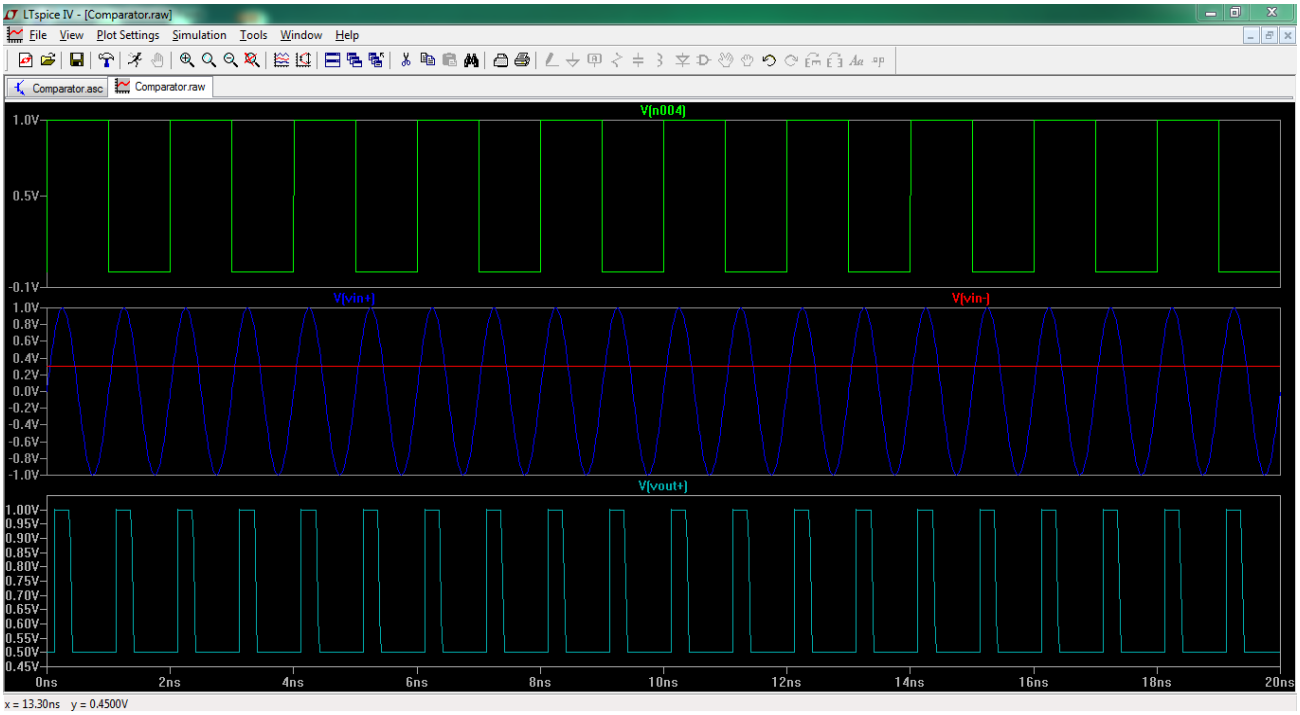


Fig.8.4 Simulation of Pseudo Dynamic Latched Comparator

## 8.1.3 OPEN LOOP COMPARATOR

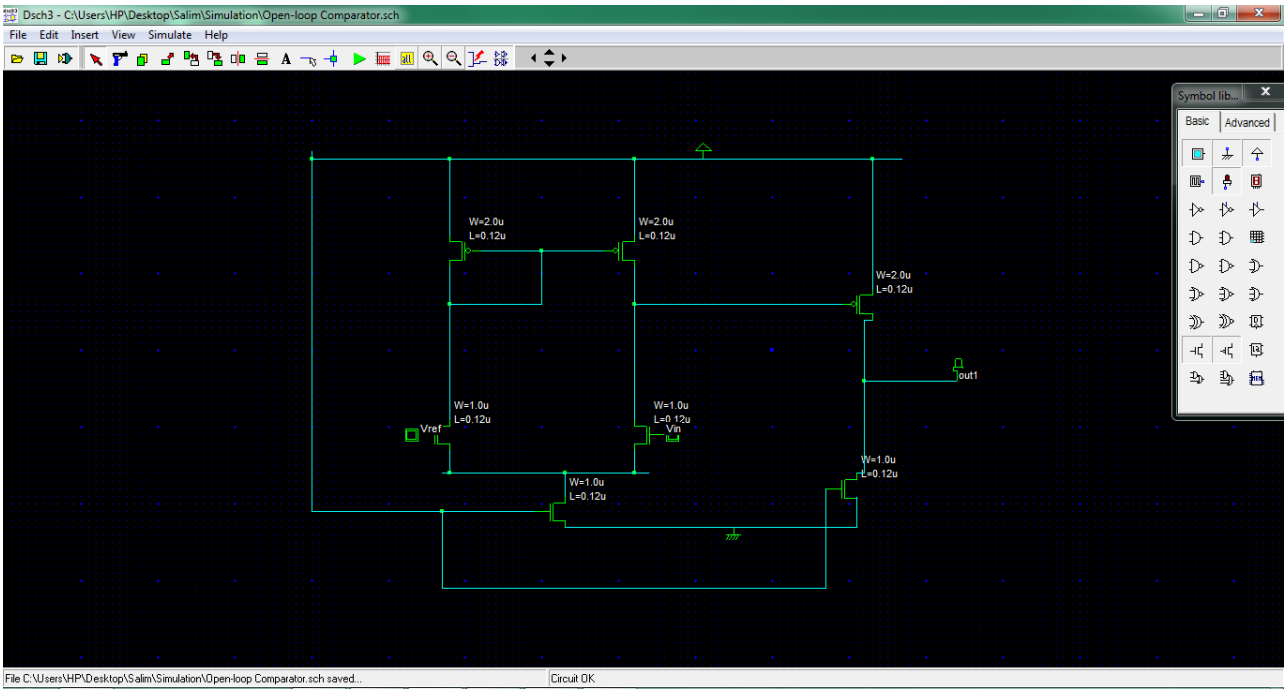


Fig. 8.5 Schematic of Open-loop Comparator

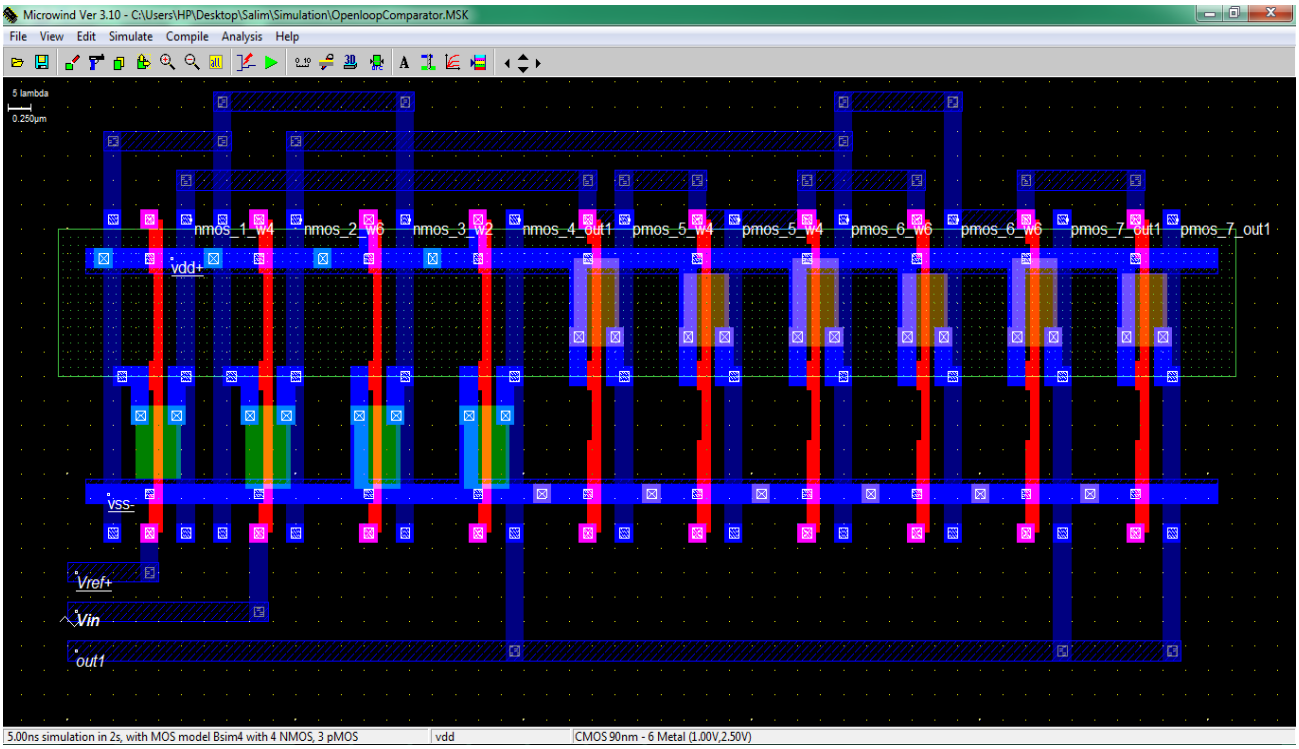


Fig.8.6 Layout of Open-loop Comparator

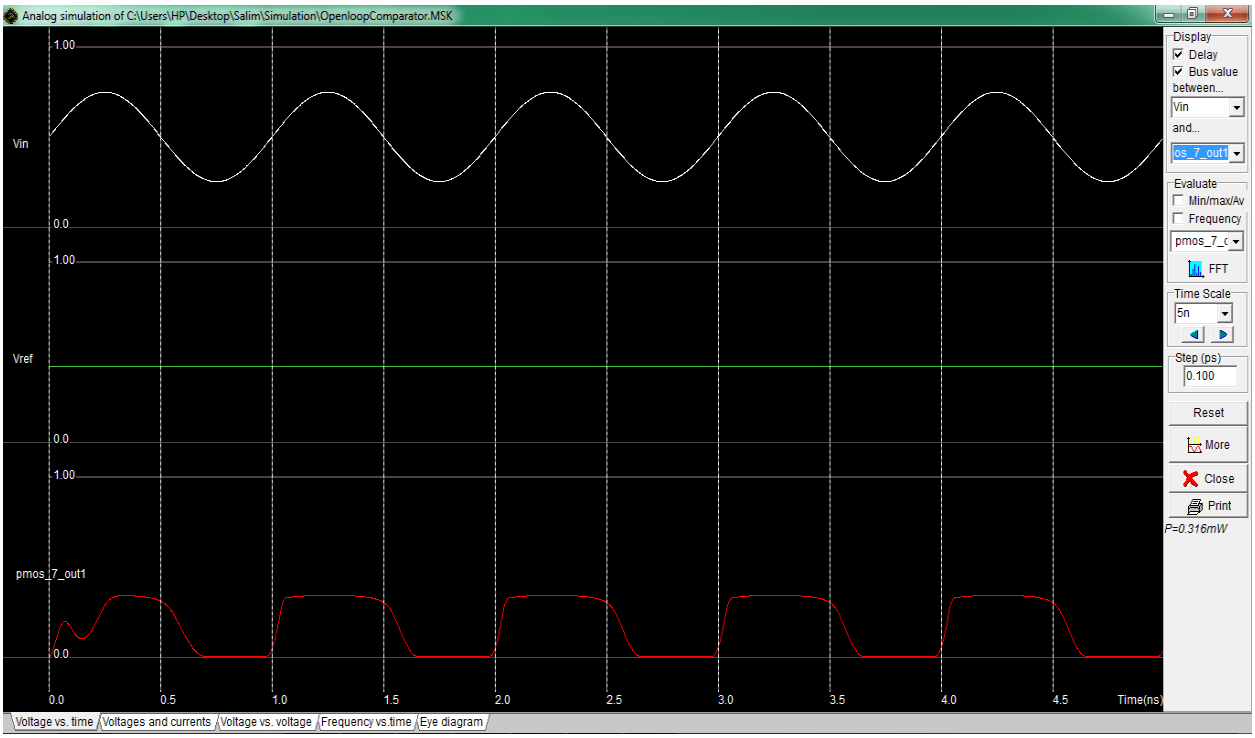


Fig.8.7 Simulation of Open-loop Comparator using CMOS 90nm

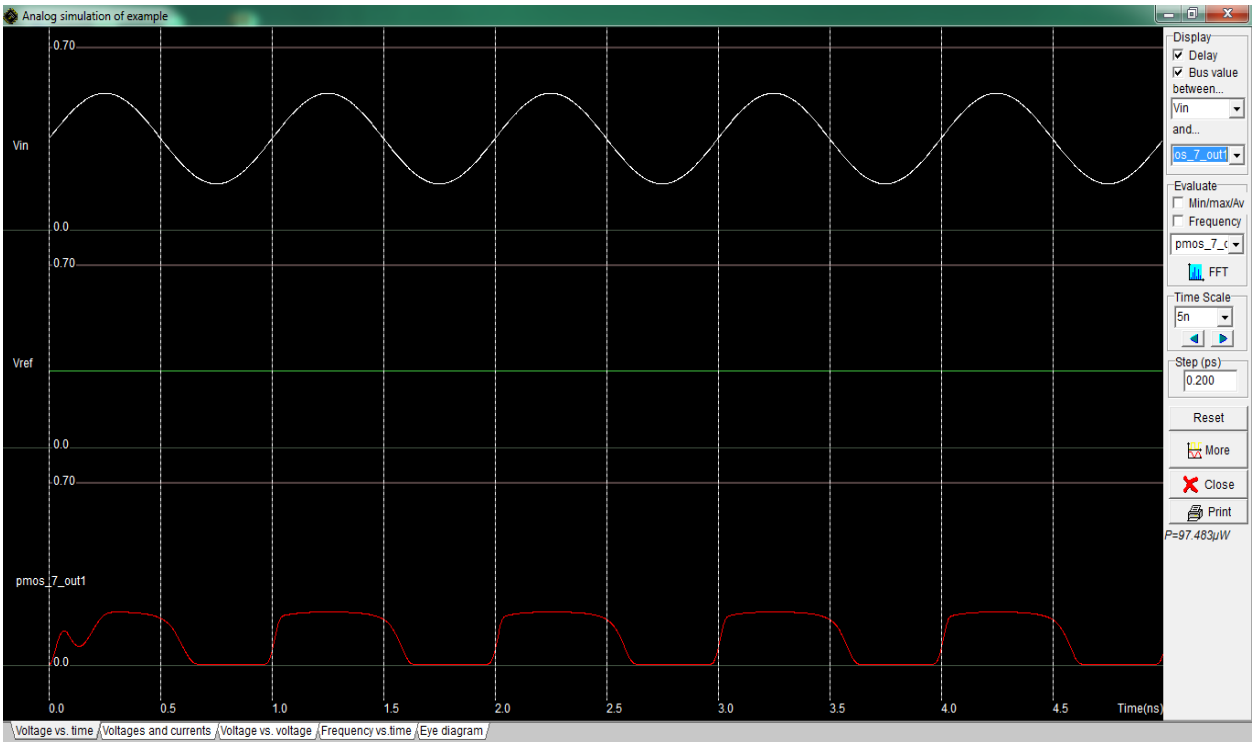


Fig.8.8 Simulation of Open-loop Comparator using CMOS 65nm

## 8.1.4 RESISTIVE DRIVING COMPARATOR (RDC)

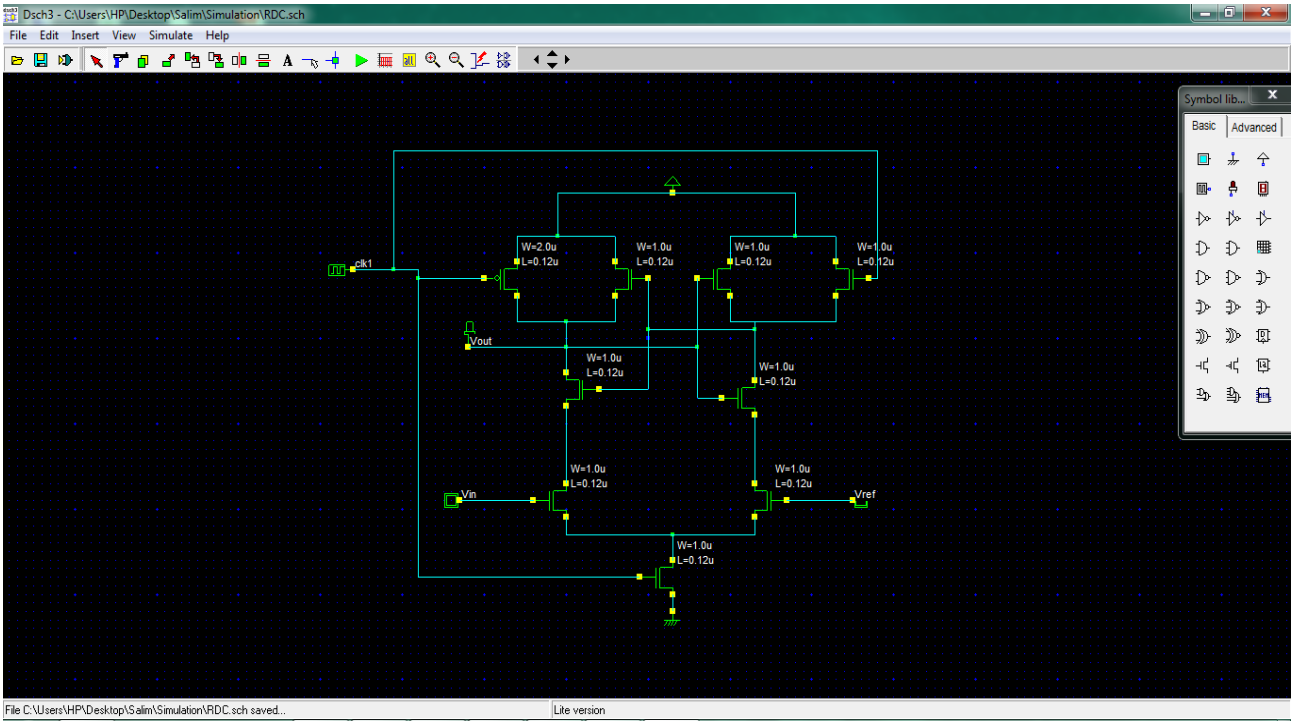


Fig.8.9 Schematic of RDC

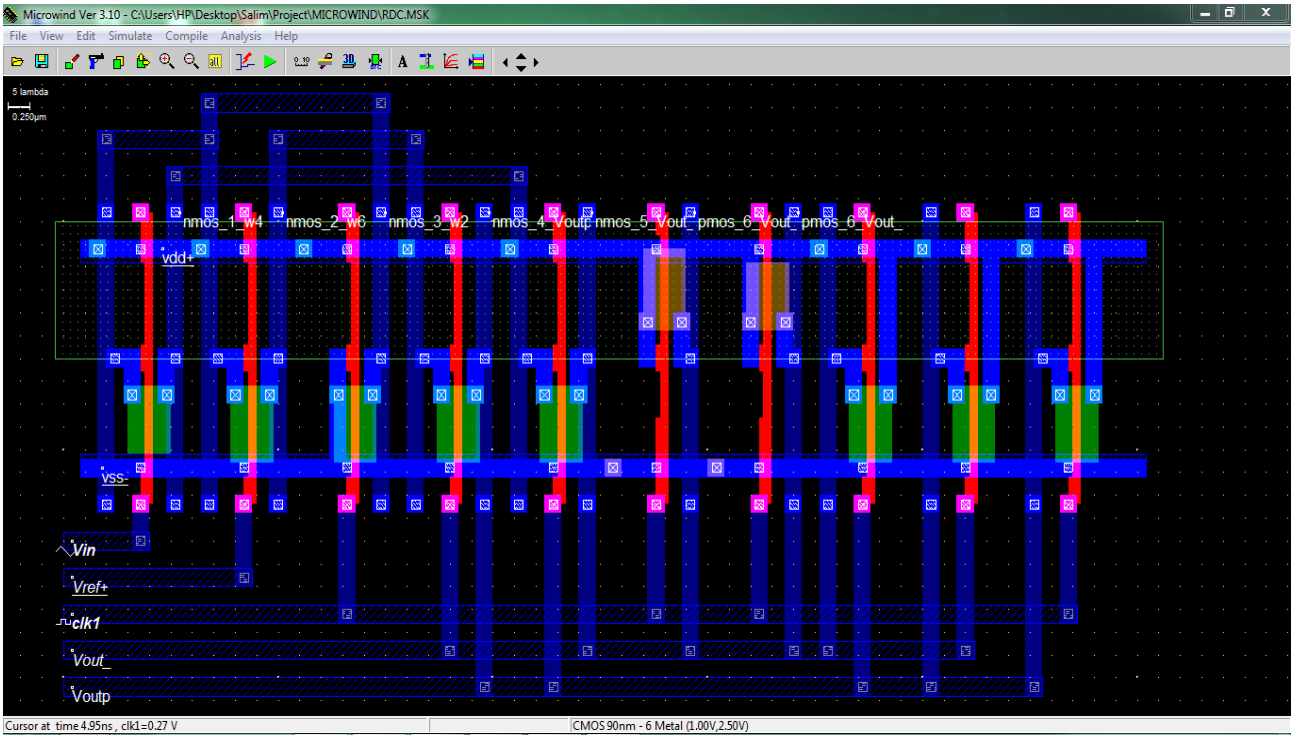


Fig.8.10 Layout of RDC

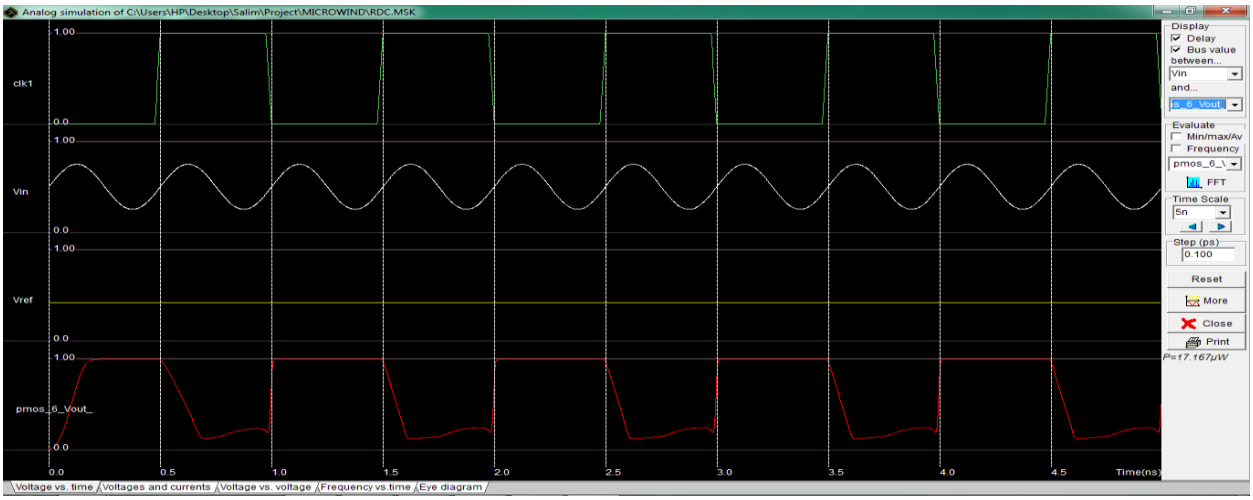


Fig.8.11 Simulation of RDC using CMOS 90nm

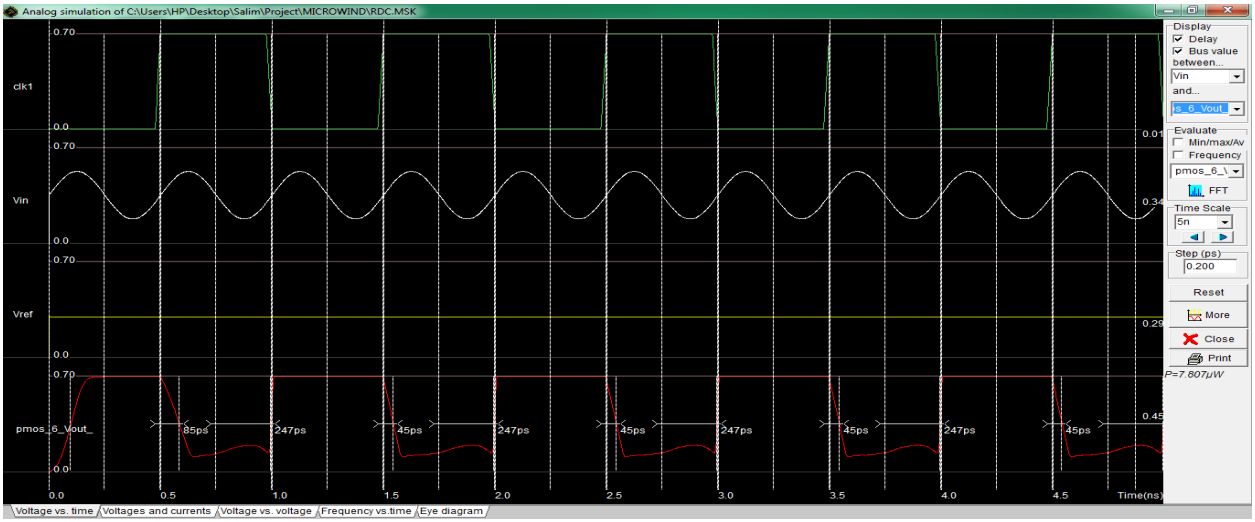


Fig.8.12 Simulation of RDC using CMOS 65nm

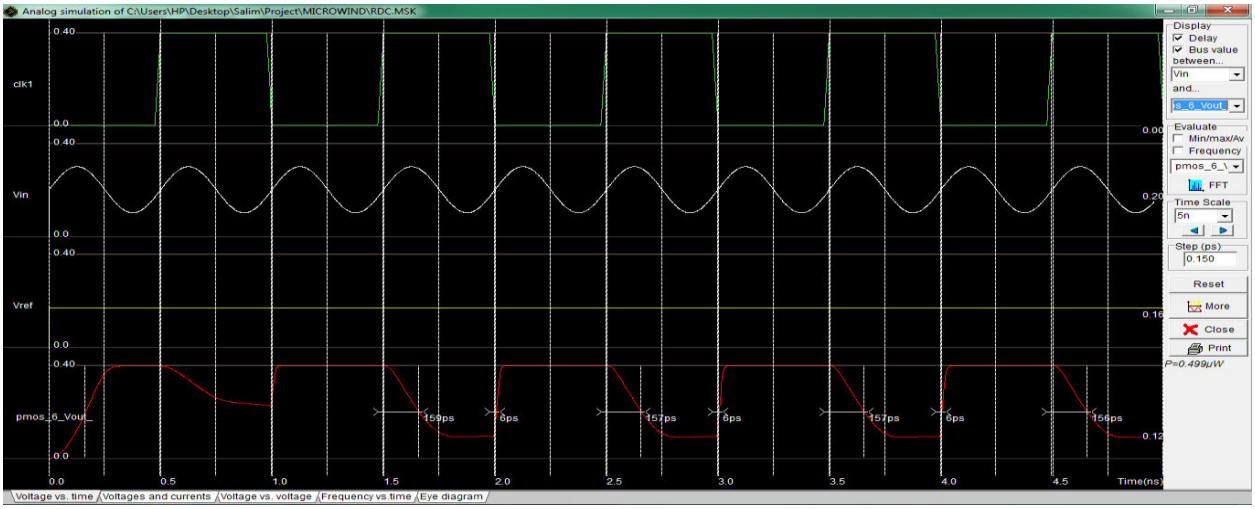


Fig.8.13 Simulation of RDC using CMOS 45nm

# 8.2 THERMOMETER TO BINARY CODE ENCODER

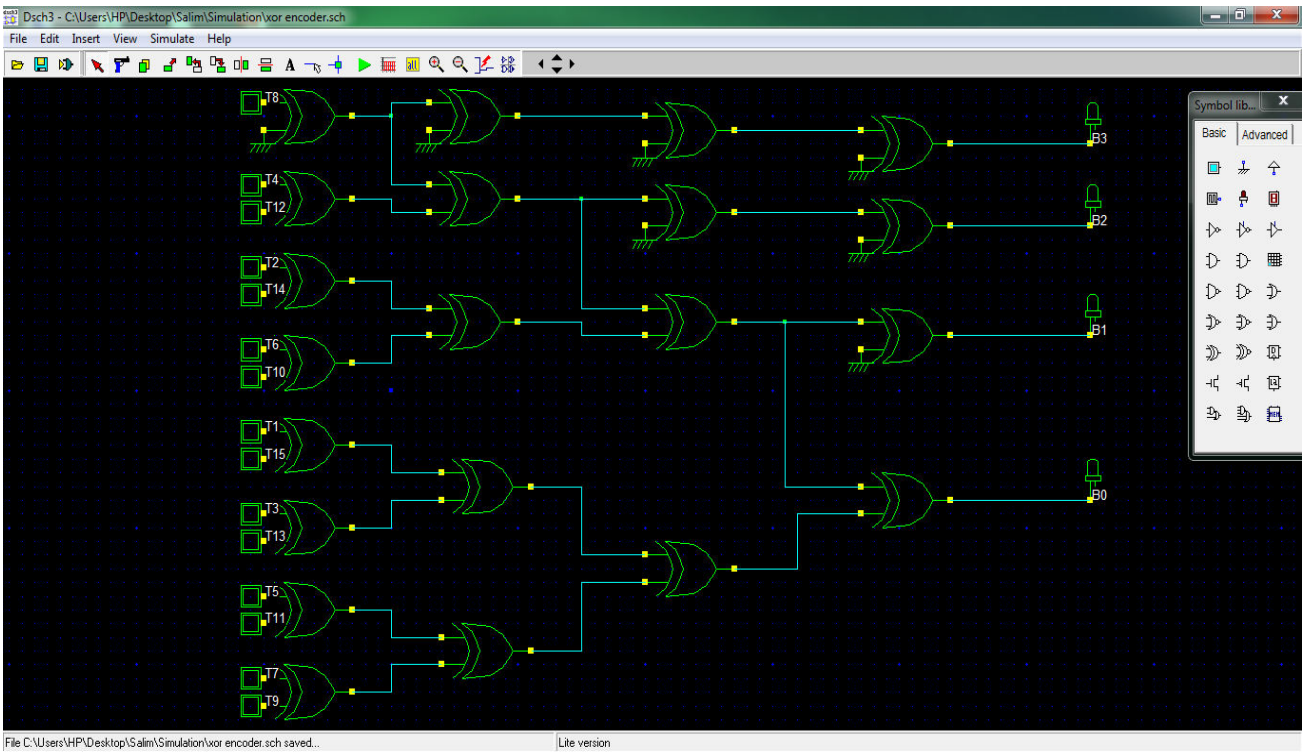


Fig. 8.14 Schematic of XOR Encoder

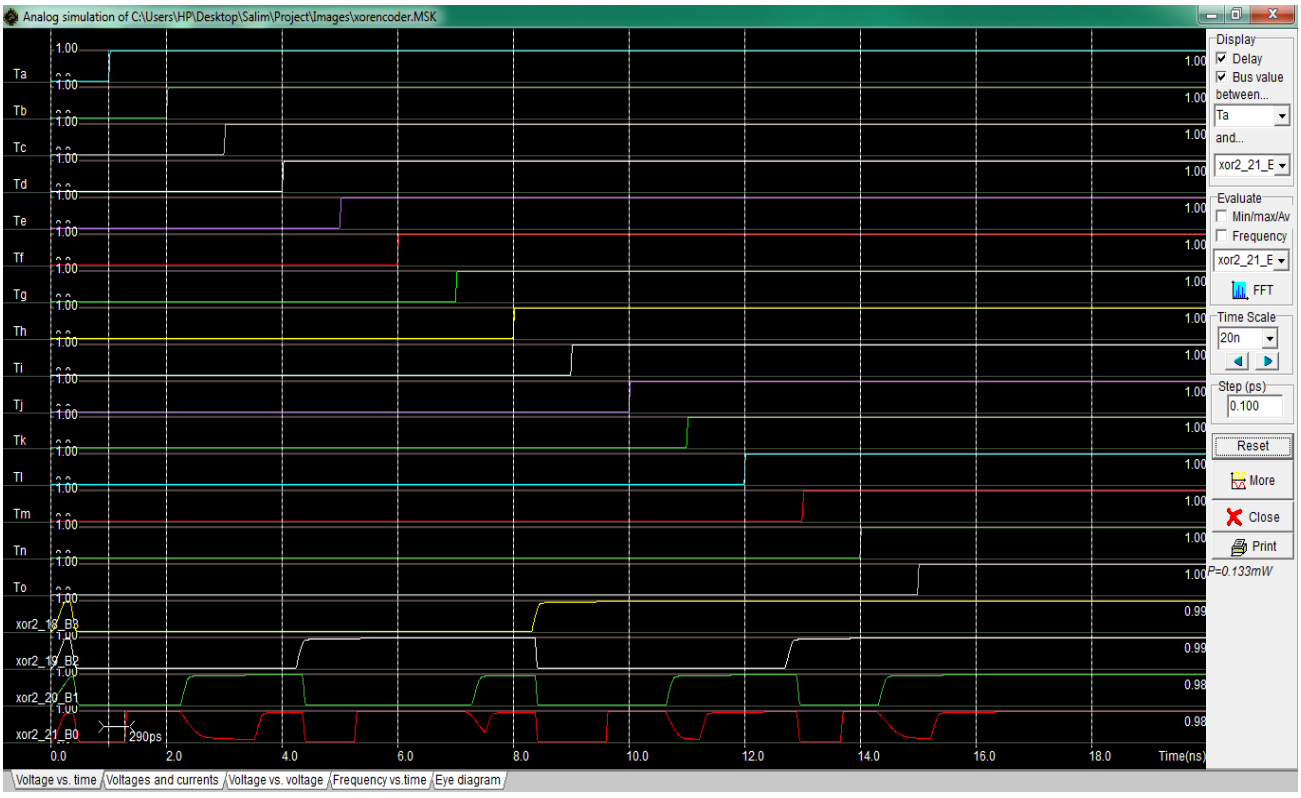


Fig. 8.15 Simulation of XOR Encoder

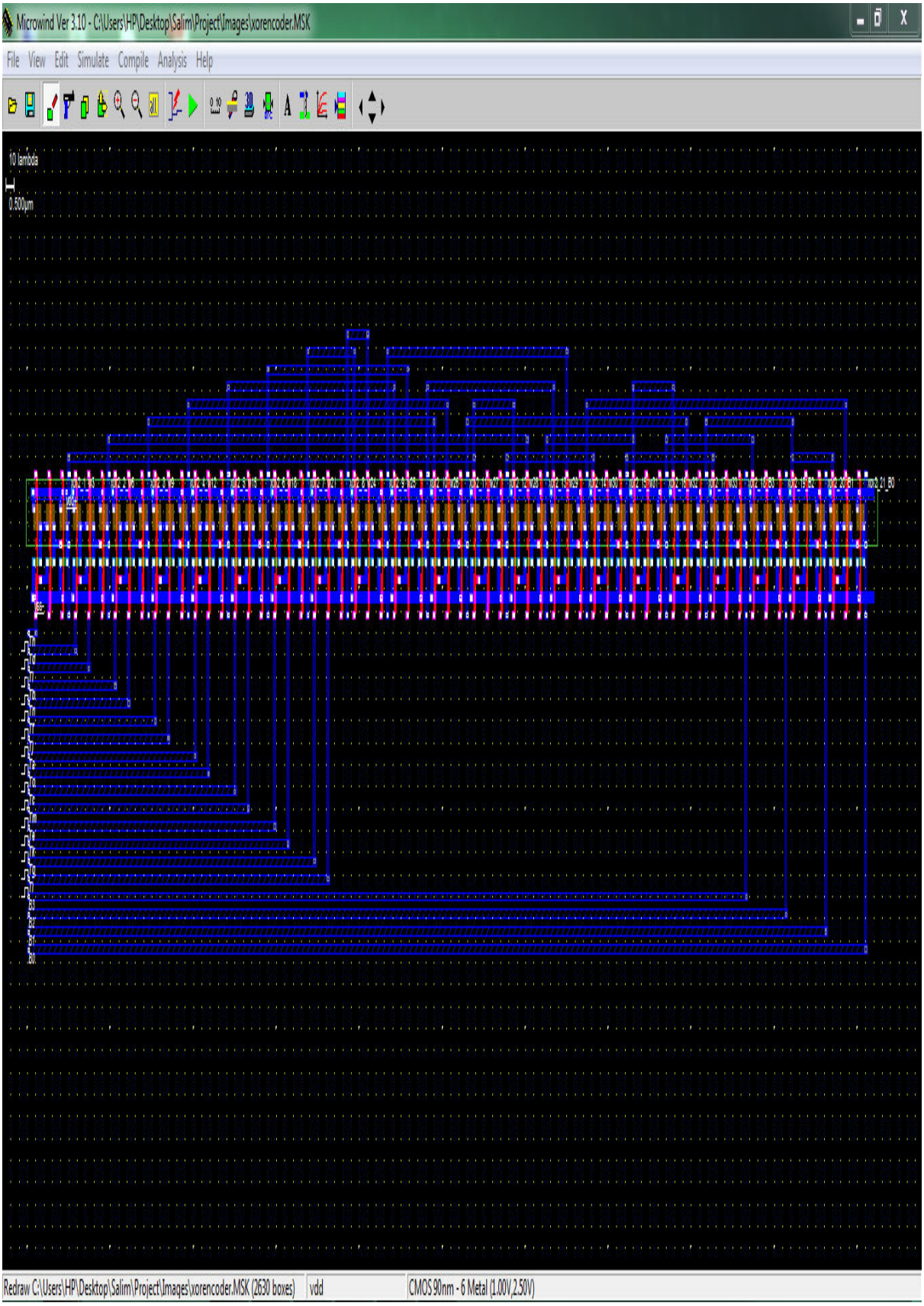


Fig. 8.16 Layout of XOR Encoder

# 8.3 FLASH ADC

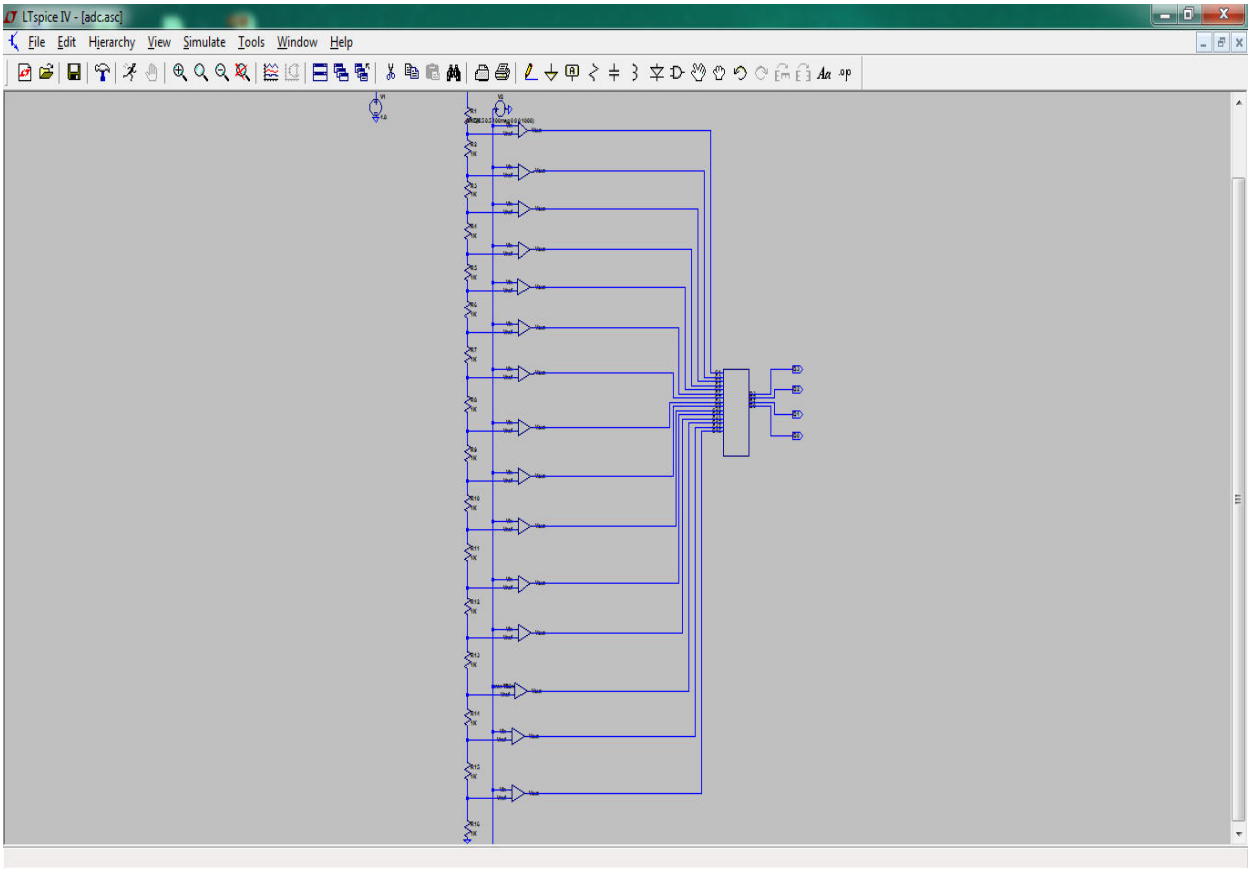


Fig. 8.17 Schematic of 4 bit Flash ADC

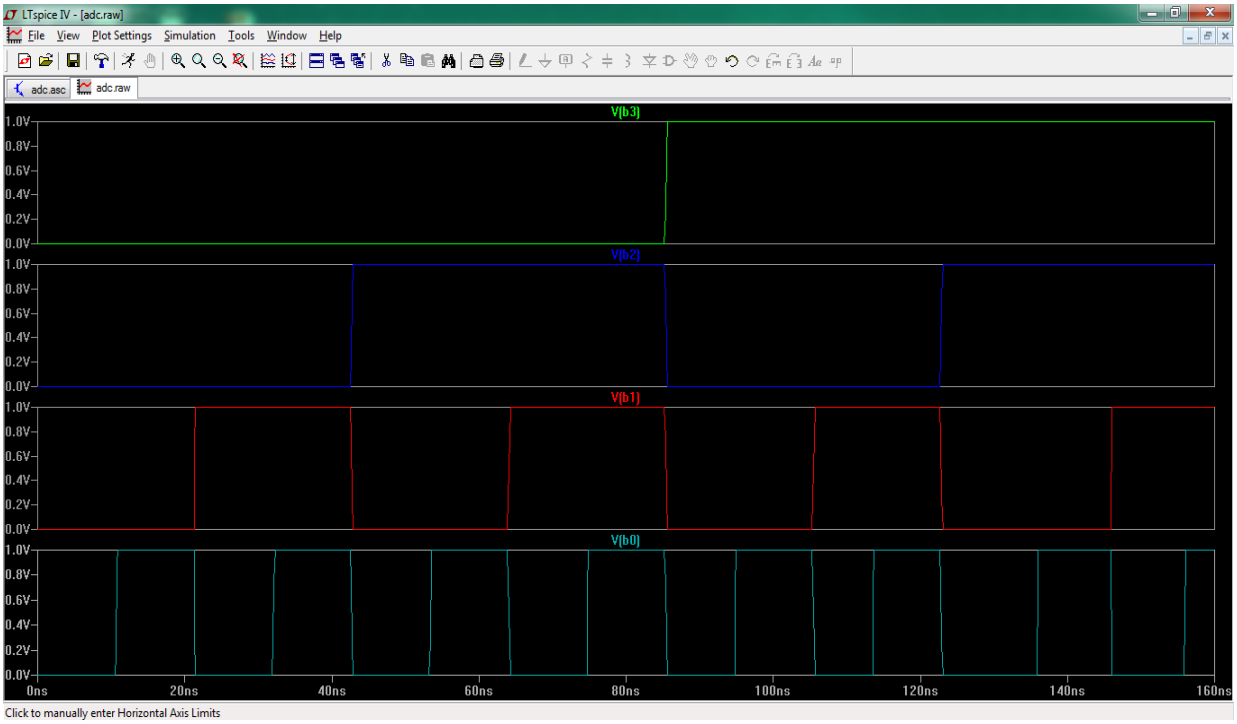


Fig. 8.18 Simulation of 4 bit Flash ADC

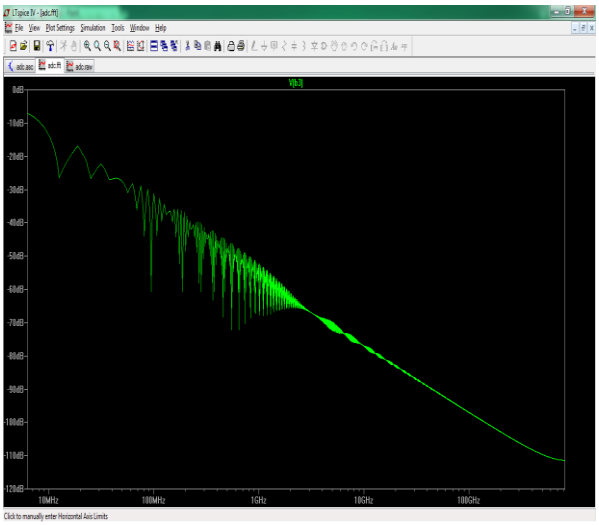

Fig. 8.19 FFT of B3

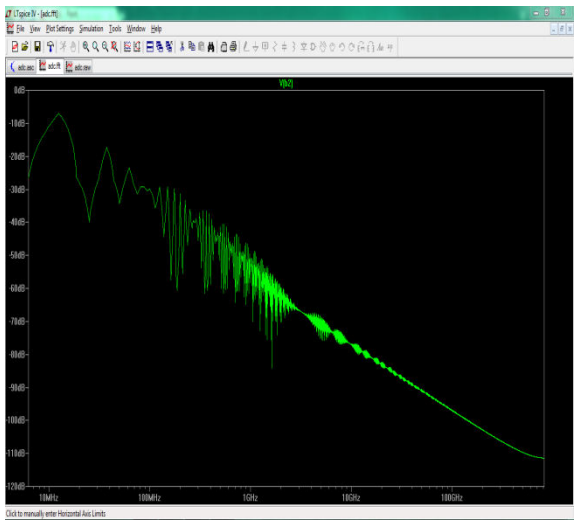

Fig. 8.20 FFT of B2

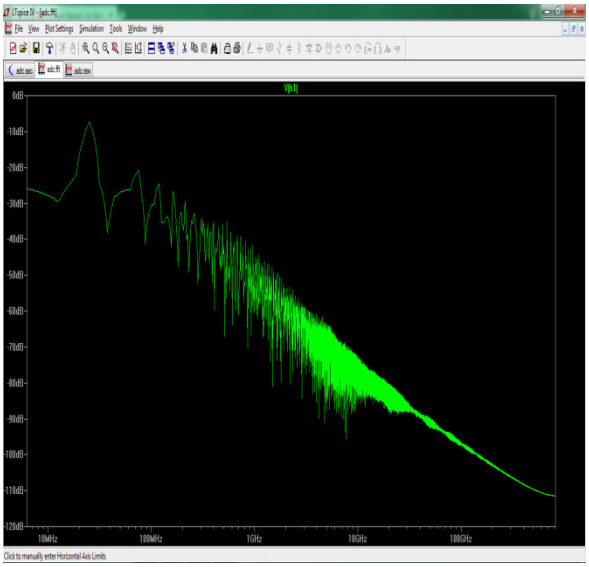

Fig. 8.21 FFT of B1

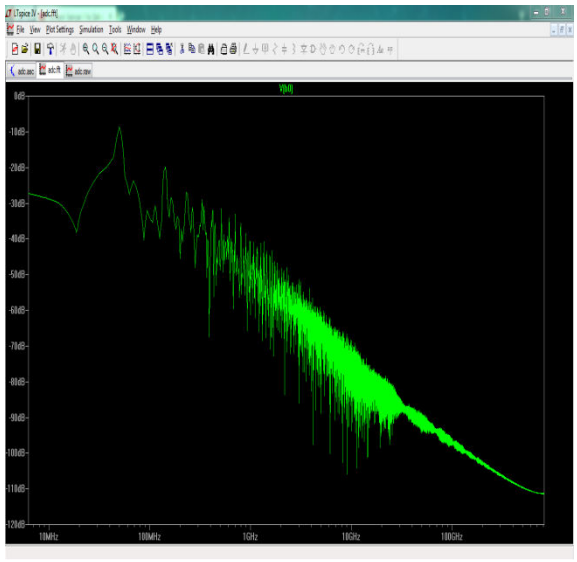

Fig. 8.22 FFT of B0

# 8.4 RESULTS

## 8.4.1 Power dissipation of Comparators

| Comparators | CMOS 90nm | CMOS 65nm | CMOS 45nm | Layout Area(WxH) |
|---|---|---|---|---|
| Open-loop | 316µW | 97.483µW | 7.034µW | 16µm x 12µm |
| RDC | 17.168µW | 7.807µW | 0.499µW | 16µm x 12µm |

Table 8.1 Power Dissipation of Comparators

## 8.4.2 Power dissipation of Encoder

| Encoder | CMOS 90nm | CMOS 65nm | Layout Area(WxH) |
|---|---|---|---|
| XOR Encoder | 0.133mW | 45.105µW | 62µm x17µm |

Table 8.2 Power Dissipation of XOR Encoder

## 8.4.3 Power dissipation of Flash ADC

The average power dissipation of Flash ADC in CMOS 90nm is 0.5mW to 0.7mW.

# Chapter 9
# APPLICATIONS

- The very high sample rate of this type of ADC enables high-frequency applications (typically in a few GHz range) like
  - (i) Radar detection
  - (ii) Wideband radio receivers
  - (iii) Sampling oscilloscopes
  - (iv) Optical communication links
- More often the flash ADC is embedded in a large IC containing many digital decoding functions.
- Also a small flash ADC circuit may be present inside a delta-sigma modulation loop.
- Flash ADCs are also used in NAND flash memory, where up to 3 bits are stored per cell as 8 voltages level on floating gates.

# Chapter 10

# FUTURE SCOPE

## Future Scope :

- All the parameters of flash ADC can be considered for higher resolution and compare its characteristics with other low resolution ADCs.
- Offset cancellation technique can be adopted in order to reduce the offset in the comparator which improves the efficiency of the total flash ADC.
- Calibration technique shows great potential in high speed and low power flash ADC design.
- This technique can be adopted in order to simplify the design.

# Chapter 11

# CONCLUSION

Flash ADC is taken as the best architecture for the high speed application. The first step of this project is to design Comparator. Different comparators are designed. Among them a comparator is selected with the power dissipation of 17.168µW in CMOS 90nm technology using 1V power supply. The layout had been drawn and the layout area of comparator obtained is 16µm x 12µm. The XOR based Encoder is designed with the power dissipation of 0.133mW with 1V power supply. The layout had been drawn and the layout area of Encoder obtained is 62µm x 17µm. Finally by combining resistor ladder, 15 comparators and encoder, a 4 bit Flash ADC is designed and simulated. The average power dissipation of designed Flash ADC is 0.5mW to 0.7mW. All the designs are simulated in Ltspice and DSCH3 software and the layout are drawn on Microwind3 software.

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