Design of ADC using CMOS for Wireless communication

Submitted in partial fulfillment of the requirements
of the degree of

(Bachelor of Engineering)

By

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AIKTC/Mumbai University

(2016-2017)

CERTIFICATE

This is to certify that the project entitled "**Design of ADC using CMOS for wireless communication"** is the bonafide work carried out by

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B.E EXTC students of Anjuman-I-Islam Kalsekar Technical Campus , Panvel , during the year 2016-17, in partial fulfillment of the requirements for the Bachelor of engineering in Electronics and telecommunication engineering and is submitted to the Mumbai University. The project report has been approved.

_____	_____	_____
(H.O.D)	**(Examiner)**	**(Guide)**
Prof. Mujib Tamboli		**Prof. Zarrar Khan**

APPROVAL SHEET

Project Report Approval for B. E.

This project report entitled (***Design of ADC using CMOS for Wireless communication***) by

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is approved for the degree of B.E EXTC.

Examiners

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Supervisors

1.----------

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Date:

Place: New Panvel

DECLARATION

I declare that this written submission represents my ideas in my own words and where others' ideas or words have been included, I have adequately cited and referenced the original sources. I also declare that I have adhered to all principles of academic honesty and integrity and have not misrepresented or fabricated or falsified any idea/data/fact/source in my submission. I understand that any violation of the above will be cause for disciplinary action by the Institute and can also evoke penal action from the sources which have thus not been properly cited or from whom proper permission has not been taken when needed.

(Mujassam Ashrafi 14DET73)

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(Shehzad Thakur 14DET125)

Date:

ACKNOWLEDGEMENT

We appreciate the beauty of a rainbow, but never do we think that we need both the sun and the rain to make its colors appear. Similarly, this project work is the fruit of many such unseen hands. It's those small inputs from different people that have lent a helping to our project.

I also take this opportunity to express a deep sense of gratitude to **Asst.Prof. Mr. Mujib Tamboli**,HOD of EXTC department for his cordial support, valuable information and guidance, which helped us in completing this task through various stages.

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I am obliged to the staff member of AIKTC, for the valuable information provided by them in the respective fields. I am grateful for their cooperation during the period of my project work.

ABSTRACT

In the current technical era, the technology advancement leads most of the applications demanding for a reduction in the whole size of the system in terms of its space occupied in any device. Mobile applications are one of the apt scenarios for this category. Apart from the size reductions due to the technology advancement, it also calls in for the reduction in the power consumption.

The Data Converters section, besides being very power hungry, it is also usually extremely power hungry in comparison with the other blocks of any architecture and that's why low power has also become a tough requirement in most of the systems. The total power consumption of the system being maintained in a low figure has almost become a mandatory specification in many applications.

The SAR Analog to Digital Converter architecture is chosen in this master thesis project, as it is one of the very successful moderate resolution achievable converter system present among all the data converter architectures. The schematic model of the entire system is implemented in Cadence system in order to fulfil the technical requirements of the project.

The SAR architecture is implemented in Cadence 180 nm technology and the power supply used is 2.5 volts. A differential configuration of the whole system is thoroughly studied and an equivalent single ended system is also studied, implemented and measured in this project. The differential architecture is studied in this project to learn the merits behind the differential architecture, which basically avoid the linearity and offset errors raised in the single ended architecture. The resolution for which the system is designed is 10 bits.

INDEX

Chapter 1

INTRODUCTION

In the fastest changing electronics world, the grip which Analog electronics has always had, can never be changed or manipulated in any kind of applications right from old trivial designs to high end designs. In--- spite of the Herculean development in Digital electronics, the status of Analog electronics still remains proud enough as the real world always operates on Analog concepts.

As all the real quantities are analog in nature, in any kind of applications there should be some means to convert those analog quantities into digital logic levels to process the signals according to the applications' accuracy requirements. So the referred critical job of converting from Analog levels to Digital levels is generally carried out with the help of Data Converters.

The two obvious types of Data converters are Analog to Digital (ADC) and Digital to Analog (DAC) converters. In this thesis work, the type ADC is chosen to evaluate the merits and demerits with respect to its expected specifications. There again comes a major classification in types of ADCs namely the Nyquist type ADCs and Oversampled ADCs mostly differentiated by the sampling frequency specified.

In all the portable applications, the main concerned issue would be the withstanding capacity of the battery power, which directly reflects to the power dissipation capability of all the circuits present in that system. As the technology develops/advances, the Digital world does as well, equally in terms of its circuits' performance but the real bottleneck has been posed on Analog side of the application as low voltage analog powered systems demand some tough compromises in the circuit to maintain the same or improved performance levels as before.

As normally any data converter circuits possess both analog and digital circuits in its system, the technological constraints like operating frequency, supply voltage levels, voltage swing limits, power consumption do speak a lot in terms of its difficulties in implementing the system in par to the advancement in technology.

Chapter 2

RELATED THEORY

2.1 DATA CONVERTERS:

In general, Data Converters (here ADC) constitutes an important block in any kind of applications where the continuous amplitude, continuous time real world analog signals are transformed into discrete time, quantized amplitude digital signals as an end product.

An entire ADC system can be divided into four main sections namely

- Anti Aliasing Filter
- Sampling
- Quantisation
- Coding

The operation of an ADC is highly non---linear as the sampling and quantization process is inherently a non---linear operation. The operating frequency (sampling frequency) decides the design and specifications of the anti aliasing filter. Based on the sampling frequency, the ADCs can be broadly classified into two major categories namely

- Nyquist Rate ADCs
- Oversampled ADCs

2.2 NYQUIST RATE ADCS:

When the referred ADC's sampling frequency is minimum twice the signal frequency as per the Nyquist's Sampling theorem, then those ADCs are termed as Nyquist Rate ADCs. There are various different types of Nyquist rate ADCs present in the Data Converters market out of which the very familiar and famous ones are mentioned with suitable explanation of its operation.

The converters, which can be thought of very successful, are

- Flash ADC
- Interpolating ADC
- R---2R and C---2C ADC
- Pipeline ADC
- SAR ADC

2.2.1 **FLASH ADC**:

Flash ADC referred also as Direct Conversion ADC is one of the familiar types of ADC for its fast operation. It comprises a linear voltage ladder with different reference voltage nodes created by resistors. The input voltage signal is compared with the respective voltage node from the voltage reference ladder with the help of a comparator, which are there each at every reference node point and the output of the comparator is allowed to enter the digital logic circuitry to produce the necessary output in the respective format.

Pros: Extremely fast Conversion time

Con: Number of comparators (2^n---1) increases as the resolution (n) increases and hence the noise and power consumption.

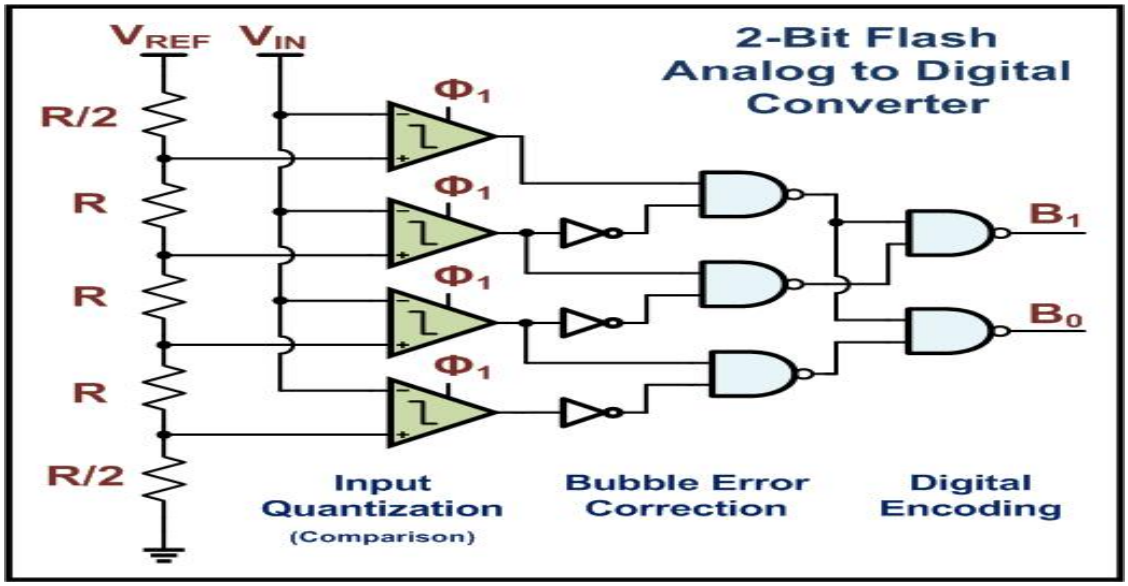


Figure 2.1: 2---bit Flash AD *(Ref: Wikipedia)*

2.2.2 **INTERPOLATING ADC**:

This type of ADC converts an unknown input voltage into a definite digital value through the help of an integrator and a known reference voltage source. The basic operation is as follows. An unknown input voltage level is applied to the inverting input of an integrator and allowed to ramp up for a certain predetermined run---up time. Once the run---up time is reached, then a known level of reference voltage of opposite polarity to the input voltage is now applied to the inverting output of the integrator. The time it takes to ramp down the integrator response is noted down and it's called as run---down time. So an unknown voltage level can thus be computed as a function of reference voltage, run---up and run---down time.

Pros: Highly Accurate

Con: Extremely slow (6 samples per second) and thus not suitable for audio and signal processing applications. Used in digital voltmeters.

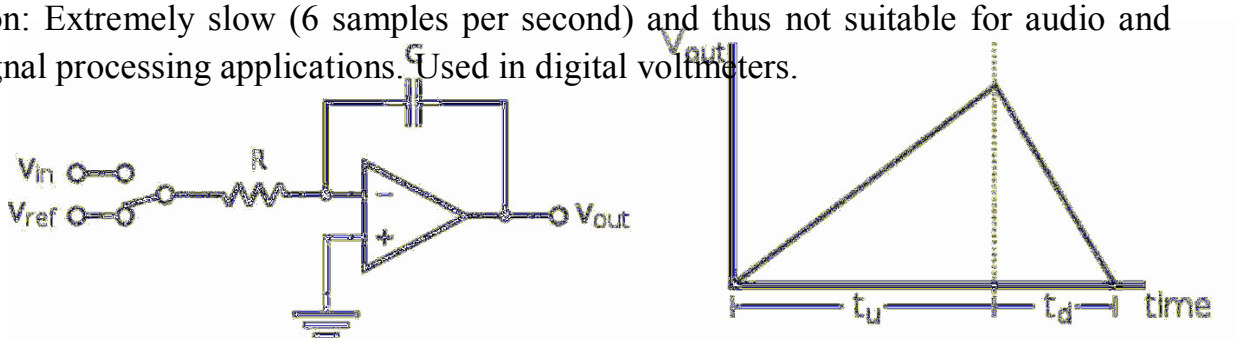


Figure 2.2: Integrating ADC and its output waveform (*Ref*: *Wikipedia*)

2.2.3 **PIPELINE ADC**:

This type of ADC, which is also known as Sub ranging ADC is very notorious for its high---resolution achievement and better throughput. As the lower sampling rate applications are dominated by SAR converters Integrating ADCs and Delta---Sigma Converters and the higher sampling rate applications are dominated by Flash Converters, the pipeline ADC can be considered to be in the middle range which compromises in a good way with most of the technical specifications of the Data converters in general such as SNR, SNDR, Resolution, Quantization noise etc.

The operation of this converter is as follows with respect to the figure presented below. It consists of four identical stages in which the conversion takes place successively. The input analog voltage is allowed to pass through a sample---and---hold circuit to make a discrete time signal. It is also passed through a Flash ADC to convert the signal into 3---bit digital value. But this is called as the stage of coarse conversion, which concentrates mostly on the computation of MSBs. This 3--- bit digital value is subtracted from the sample---and---hold value and the residue value is sent to the successive stages for further refinement of the signal for better accuracy. The output of the final stage is connected to a 4---bit flash converter where the LSBs are computed.

Pros: High throughput, better efficiency, moderate sampling rate

Con: Latency

2.3 **OVERSAMPLED CONVERTERS**

2.3.1 **DELTA SIGMA ADCS**:

This converter is one of the very famous and efficient types of ADCs present in the current market. This converter trades off sampling rate for high resolution. The oversampling ratio (OSR), which is defined as the ratio of the Nyquist frequency (fs/2) and the signal frequency, decides the efficiency of the converter. The order of the converter depends on the application it is used for. Most of the time, second order is preferred as it has a good compromise between circuit complexity and better performance. The basic first order modulator is explained as follows.

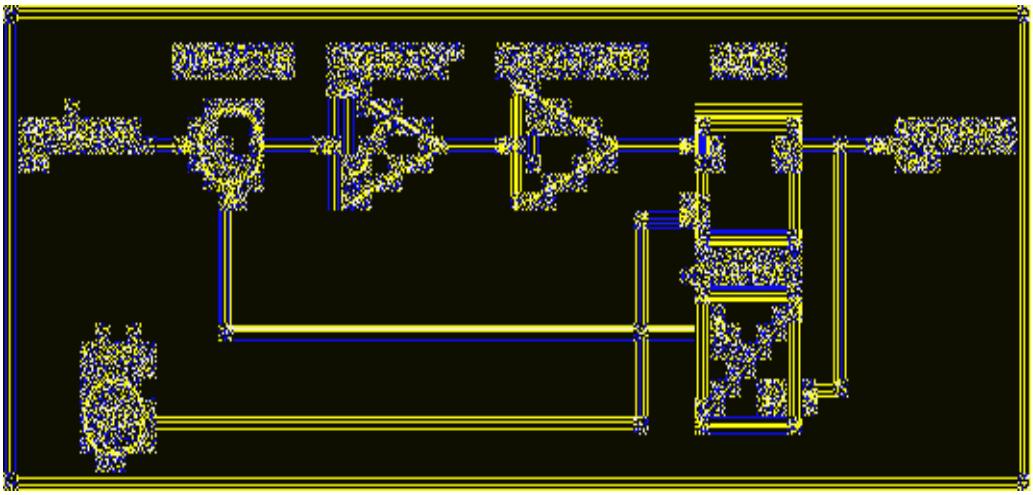


Figure 2.3: First order Delta Sigma Modulator (*Ref: http://www.beis.de*)

The difference block computes the error waveform, which comes as a result of the subtraction of the analog input signal and the output of the 1---bit bitstream passed through the DAC. Then it gets integrated and compared with the threshold reference level to give either a high level (1) or a low level (0) bitstream. The bitstream is usually higher than the data rate of the ADC. The averaging of the bitstream is done after the modulator section through digital processing to get the digital equivalent of the input analog signal. The SNR depends on the order of the modulator and also on the OSR ratio.

2.4. PERFORMANCE METRICS:

There are different performance metrics used in an ADC to explain its quality in many different ways. These performance metrics are broadly classified into two major divisions namely

- Static Characteristics
- Dynamic Characteristics

The category of Static Characteristics is again classified into four different types namely

- Differential Non Linearity (DNL)
- Integral Non Linearity (INL)
- Offset Error
- Missing Codes

The category of Dynamic Characteristics is compromised of four major performance parameters namely

- Signal to Noise Ratio (SNR)
- Signal to Noise and Distortion Ratio (SNDR)
- Spurious Free Dynamic Range (SFDR)

- Effective Number of Bits (ENOB)

2.4.1. STATIC CHARACTERISTICS:

Static Characteristics of an ADC explains the deviation of the transfer characteristics of an ADC from the ideal characteristics. As mentioned above, the four performance parameters DNL, INL, Missing codes and Offset error comprises in this category.

2.4.1.1 DIFFERENTIAL NON---LINEARITY (DNL):

Differential Non linearity is one of the important performance parameter in the static characteristics. It explains the difference in code width of one LSB level from the ideal width of one LSB level. If for example the code width for the code 10 is 0.25 LSB longer than the ideal width of it, which is 1LSB, then the DNL error is +0.25 LSB. In the same way, if the code width is 0.25 LSB shorter than the ideal code width, then the DNL error is ---0.25 LSB. During the measurement of DNL and also INL, the offset error and the full---scale error are considered negligible. The positive DNL error can be computed from widest code and the negative DNL can be computed from the narrowest code.

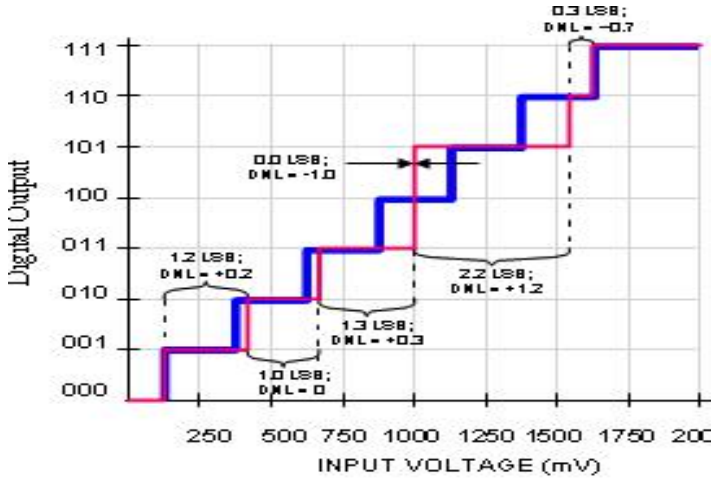


Figure 2.4: DNL Characteristics for a 3---bit converter (XX)

2.4.1.2 INTEGRAL NON---LINEARITY (INL):

Integral Non Linearity is again one important static performance parameter, which is a lot similar to DNL in terms of its measurement process. It explains the deviation from the ideal straight line shaped transfer characteristics. It actually explains the cumulative nature of the DNL property of the mentioned system. The size and distribution of DNL errors decide the nature of INL of the converter. The dotted line in the diagram represents the ideal characteristics whereas the bold line represents the actual characteristics.

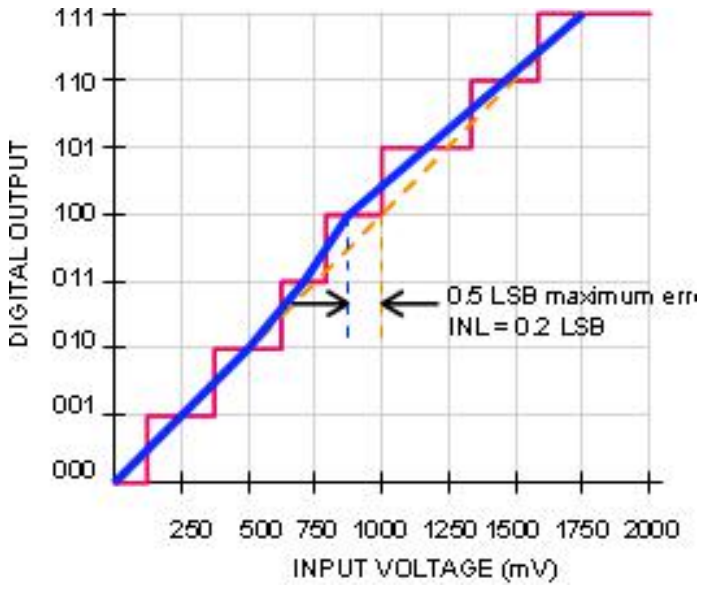


Figure 2.5: INL Characteristics for a 3---bit converter (XX)

2.4.1.3 OFFSET (ZERO) ERROR AND FULL SCALE ERROR:

Offset Error is the difference between the beginning of the first actual code transition point and the ideal code transition point present in the ideal characteristics. The full---scale error is the difference between the beginning of the actual last code transition point and the point where the last code transition point starts for an ideal ADC.

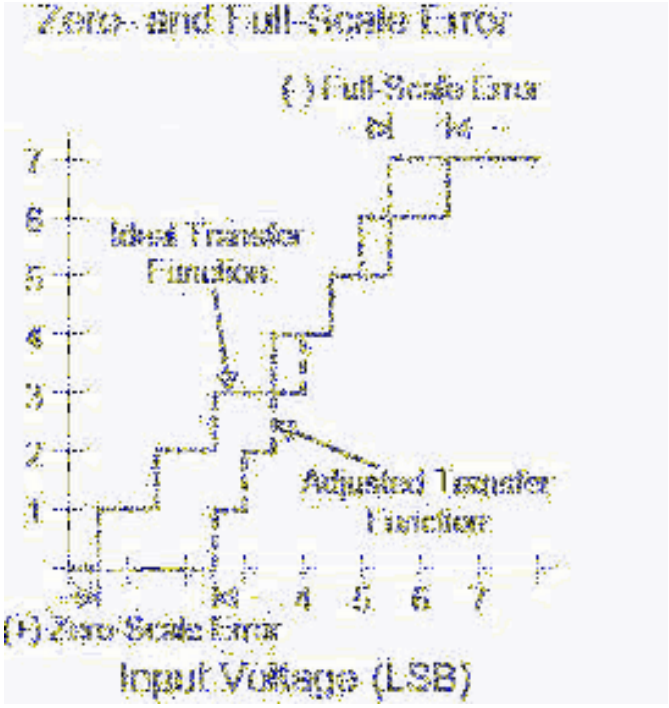


Figure 2.6: Zero/Full Scale Error for a 3---bit converter (XX)

2.4.1.4 MISSING CODES:

Missing Codes are the ones that are missing from the transfer characteristics of an ADC mainly either due to the masking of that specific code by the lower transition code or by the upper transition code. The code, which gets missed, gives out a DNL of ---1 LSB. So if there is an appearance of ---1 in the DNL graph, then that's a sign to prove in one way that there is a missing code in the system during the conversion process.

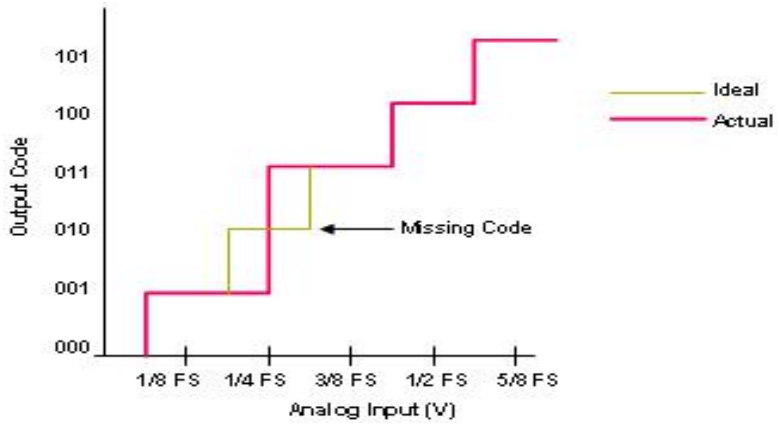


Figure 2.7: Missing codes plot for a 3---bit converter (XX)

2.4.2 DYNAMIC CHARACTERISTICS:

The Static Characteristics are tested by a DC input whereas the dynamic characteristics are measured by the response of the ADC for a sinusoidal input. It is used to compute the frequency response of the system. This analysis is used to know more information about noise and also about other high frequency effects. These performance metrics are exhibited by the parameters like SNR, SNDR, SINAD, SFDR and ENOB.

2.4.2.1 SIGNAL TO NOISE RATIO (SNR):

The SNR can be defined as the ratio of the power of the signal and total noise power generated by quantization process. Usually the signal, which is referred here, is a sinusoidal signal. This dynamic property accounts for the whole noise present in the entire Nyquist range. Its value depends on the magnitude of the input signal and it proportionately decreases with the reduction in the signal amplitude. The value of SNR is given by

SNR = ((6.02*Resolution) + 1.76).

2.4.2.2 SIGNAL TO NOISE AND DISTORTION RATIO (SNDR):

SNDR can be defined as the root mean square of the power of the signal in the Nyquist range and the noise power due to quantization process and also due to the other noise sources (except dc noise) including the non---linear distortion sources.

2.4.2.3 SPURIOUS FREE DYNAMIC RANGE (SFDR):

SFDR can be defined as the ratio of the root mean square of the signal amplitude and the root mean square value of the highest spurious spectral component that could possibly present in the first Nyquist interval.

2.4.2.4 EFFECTIVE NUMBER OF BITS (ENOB):

The Effective Number of bits (ENOB) is a parameter, which stands out to show the accuracy of the ADC for a specific input signal given at a specific sampling rate. It can be computed by the following expression, which is as follows

$$ENOB = \frac{SINAD\ (dB) - 1.76\ (dB)}{6.02\ (dB/bit)}$$

2.5 SUCCESSIVE APPROXIMATION (SAR) CONVERTERS:

Among various advantages copyrighted to itself by its own architecture, the simple implementation is also a big plus for SAR converter. The whole system can be divided into four main subsystems namely

- Sample (Track) and Hold Circuit
- Digital to Analog (DAC) Converter
- Comparator
- SAR Logic Block

The main operation of the SAR works on Binary search algorithm. The operation is assumed to have a digital value equal to half of the full---scale value at the digital registers present in the SAR logic block. This condition leaves us with the logic 1 as MSB and rest of all the bits to be logic 0. The corresponding switches to this mentioned condition gets activated in the DAC block to have the necessary capacitors connected to the actual operation. This gives away the necessary voltage from the DAC block to the comparator input where this voltage level is compared with the input voltage.

If the input voltage is less than the DAC voltage level, then the comparator outputs a logic 0 and logic 1 if it's the other way around. This output value is stored in one of the SAR logic block's registers and the next comparison is done in the comparator with the newly generated next DAC voltage level to get the correct digital level interpretation of the analog input voltage level. Usually the sampling frequency of the input signal is N (number of bits) times lesser than the clock frequency of the system clock as the internal clock has to be N times faster than the input clock to convert all the bits successfully. The capacitor stage in the DAC block have also got a dummy capacitor next to the LSB stage in order to make the total amount of capacitance to a power of 2 which makes the analysis better and sensible.

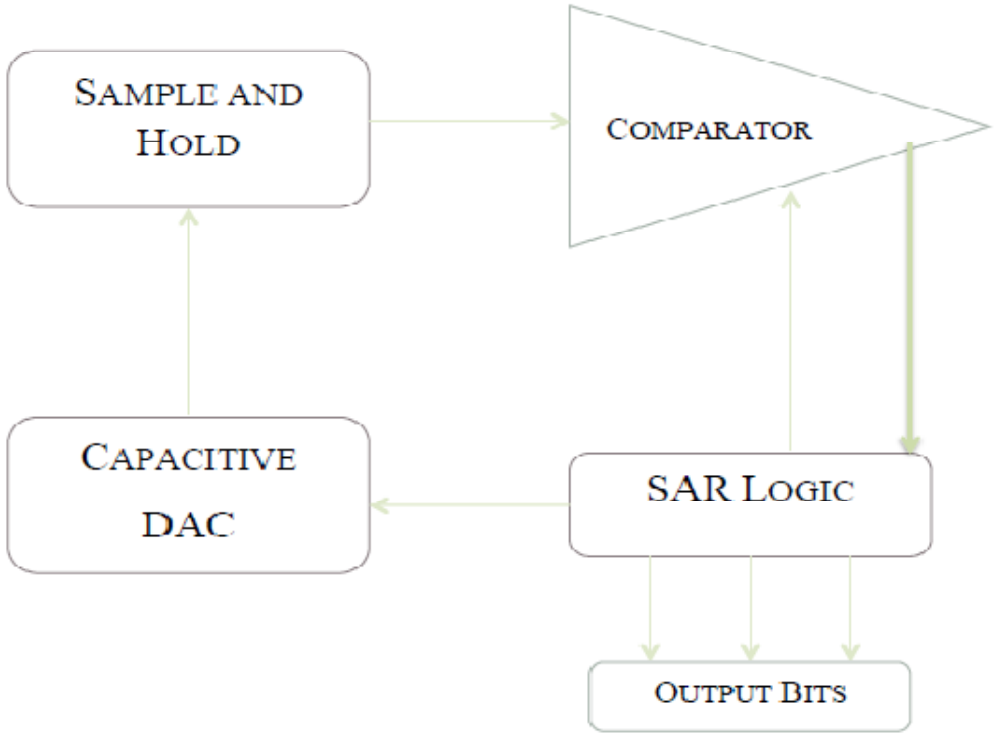


Figure 2.4: General block diagram of SAR ADC

2.6 **WHY SAR AND NOT OTHER ARCHITECTURES**?

SAR architecture has only one comparator block, which is relatively a low power---consuming block. It also reduces the power hungry requirement by not having an opamp block in its system and hence an appreciable power consumption factor can be achieved in comparison with other architectures.

The power dissipation capacity gets scaled with the sample rate associated with the system unlike Flash ADCs in which the power dissipation is independent of the sample rate. In this project, the signal frequency is maintained at 200 Hz and the sampling rate is around 2 KS/s. The frequency of the internal clock is maintained at the rate of 22 KHz.

Chapter 3

LITERATURE SURVEY

[1] a 0.4 v, sub-nw, 8-bit 1 ks/s sar adc in 65 nm cmos for wireless sensor applications, prposed in dec-15 with 65nm technology and 1ks/s sampling rate results the adc achieves satisfactory dynamic and static performance and maintains almost constant sndr over the entire signal bandwidth. it is sourced with 0.4volts supply and consumes 717pwatt power.

[2] a 2.02–5.16 fj/conversion step 10 bit hybridcoarse-fine sar adc with time-domainquantizer in 90 nm cmos which needs 0.4-0.7 v supply having 200nw power consumptions, also has the 90nm technology and 250 ks/s to 4 ms/s sampling rate was brought in feb-2016 under sar archtitecture which gives the measurement results show a power-efficient adc solution appropriate for biomedical and internet of things (iot)

[3] Gregor Tretter, Mohammad Mahdi Khafaji, David Fritsche, Corrado Carta, *Member, IEEE,* And Frank Ellinger published Design and Characterization of a 3-bit 24-GS/s Flash ADC in 28-nm Low-Power Digital CMOS in april-2016 concludes the result of a design that aims at the highest possible sampling rate for a single ADC core. In order to achieve this goal, the bandwidth requirements for the ADC input stages have been investigated and evaluated in the form of simple math equations for efficient circuit implementation.

[4] a technical paper named A 10 bit 90 MS/s SAR ADC in a 65 nm CMOS Technology, introduced by author Johannes Digel, Markus Gr¨ozing And Manf red Berroth presents an asynchronous SAR ADC with10 bit resolution and a sampling rate of 90 MS/s. The sampling rate can be varied in a wide range. The ADC doesn't require any calibration and operates with the supply as reference voltage. Hence it doesn't require any external control signals or temporarily known input signals. The chip is fabricated in a 65 nm CMOS technology without the need for any special process option.

[5] The proposed 12-bit ADC, which achieves an ENOB of 11 bit and an energy efficiency of 11.7 fJ/conversion-step, is useful for high-performance sensor

applications which is proposed by Yung-Hui Chung, Chia-Wei Yen, and Meng-Hsuan Wuwith named as A 24-μW 12-bit 1-MS/s SAR ADC With Two-Step Decision DAC Switching in 110-nm CMOS in year 2016.

[6] IEEE Transactions on Circuits and Systems proposedA 0.95-mW 6-b 700-MS/s Single-Channel Loop-Unrolled SAR ADC in 40-nm CMOS by Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and Nan Sun in year 2016 presented a high-speed and low-power singlechannel loop-unrolled SAR ADC. It proposed a simple method to calibrate the comparator offsets. The proposed switching technique allows the designers to control comparator input common-mode voltage for comparator offset and speed optimization. It can be easily time-interleaved (TI) for even higher speed applications.

[7] a Very Large Scale Integration (VLSI) Systems, IEEE International Symposium proposed paper in year 2016 by author James W. Haslett brought up 5-bit 5-GS/s Noninterleaved Time-Based ADC in 65-nm CMOS for Radio-Astronomy Applications which includes on-chip foreground calibration and achieves an ENOB of 4.7 bit at low frequencies and 4.1 bit at high frequencies. The proof-of-concept TB-ADC demonstrates an FoM of 0.17-pJ/conversion-step at a sampling rate of 5 GS/s.

Chapter 4

PROBLEM STATEMENT

There is a need for low power analog-to-digital converters, especially in portable systems with a limited power budget. In order to better understand the power dissipation of ADCs knowledge of the fundamental limits is necessary.

The ADC is often designed so that the quantization noise dominates over thermal noise which means that the power dissipation is unnecessarily large. When scaling down parameter of CMOS the power, current levels and the noise power will start to dominate further if the design is not done carefully, the signal to noise degradation will be large, which will in turn degrade the performance of ADC.

Chapter 5

DESIGN METHODOLOGY

5.1. DIFFERENTIAL AMPLIFIER

CIRCUIT DIAGRAM:

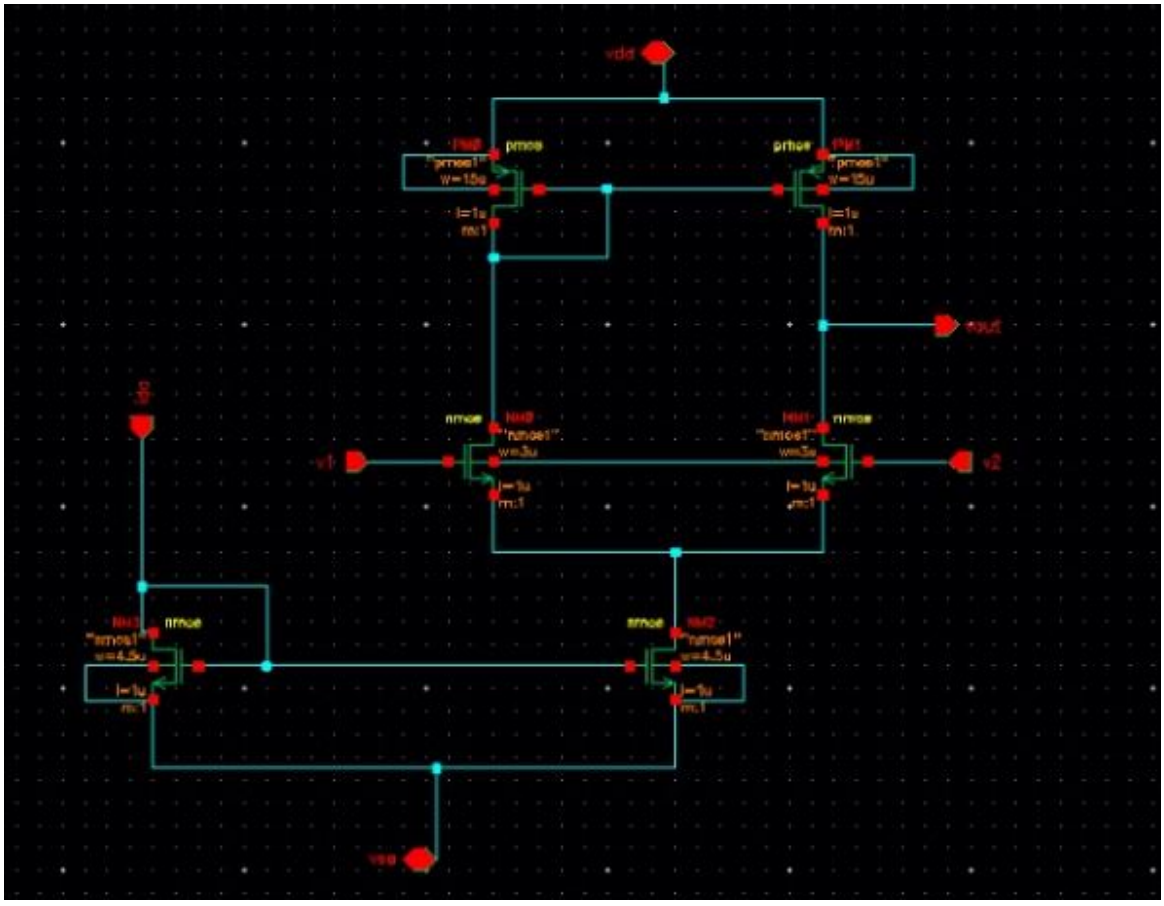


Figure 5.1(a): Circuit diagram of differential amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

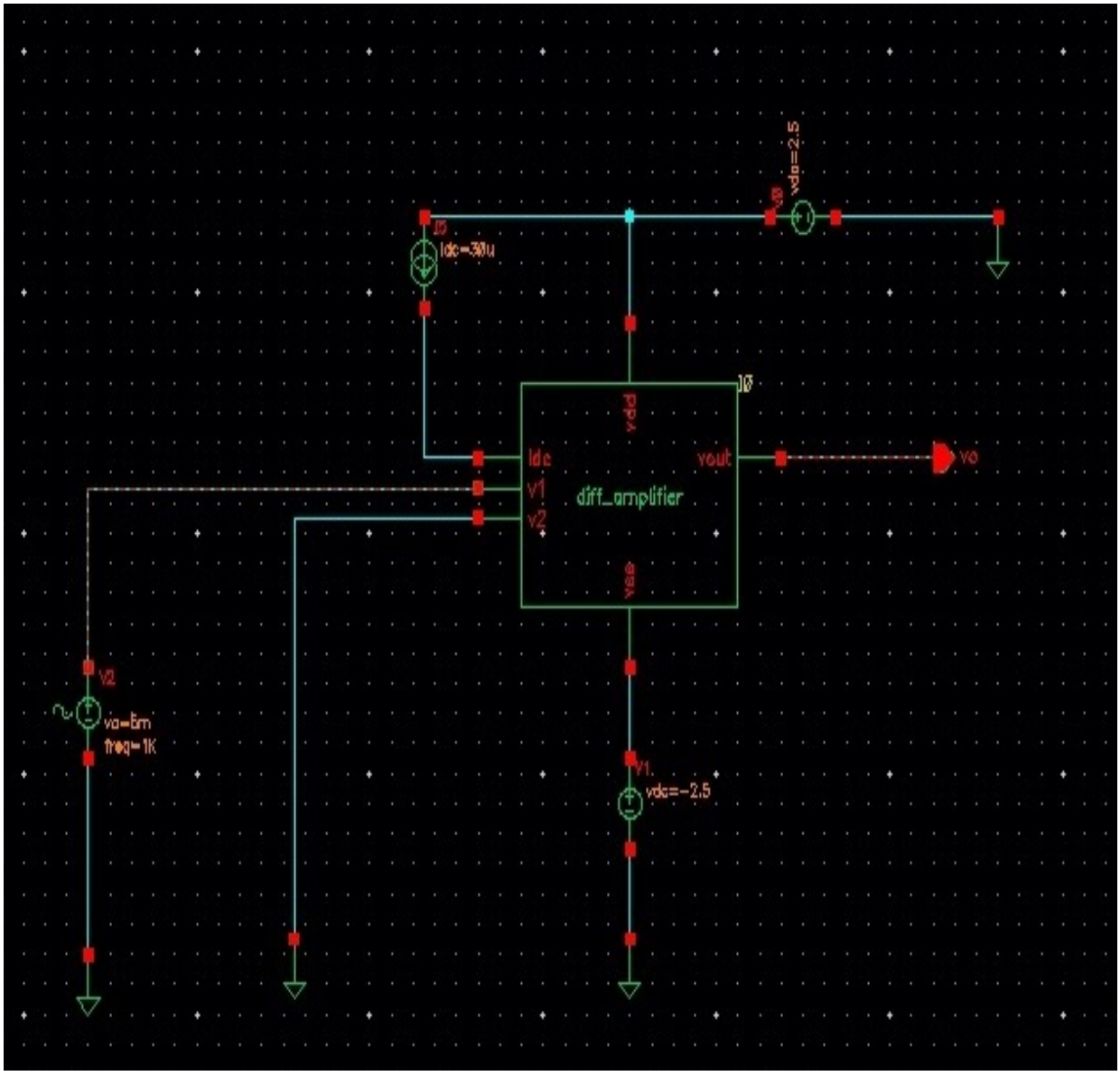


Figure 5.1(b): Schematic diagram of differential amplifier

5.2. SAMPLE AND HOLD CIRCUIT:

CIRCUIT DIAGRAM:

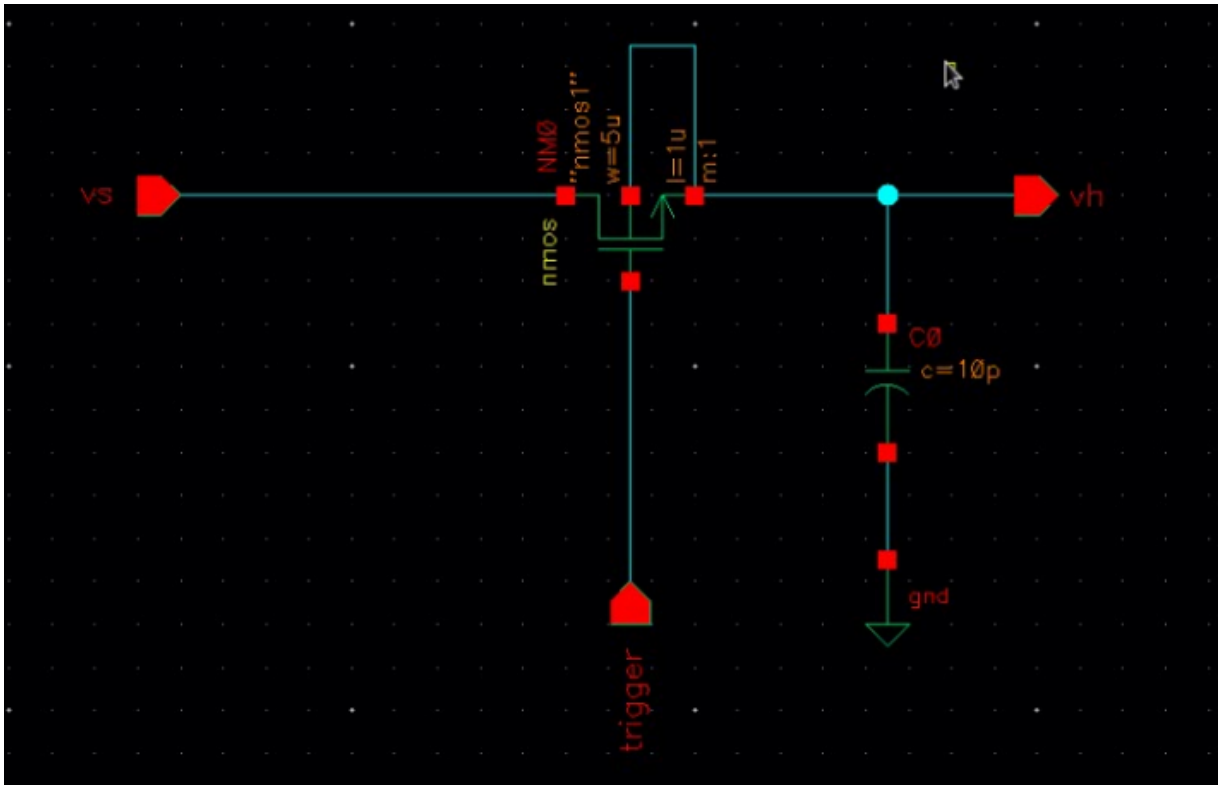


Figure 5.2(a): Circuit diagram of sample and hold circuit

SCHEMATIC DIAGRAM:

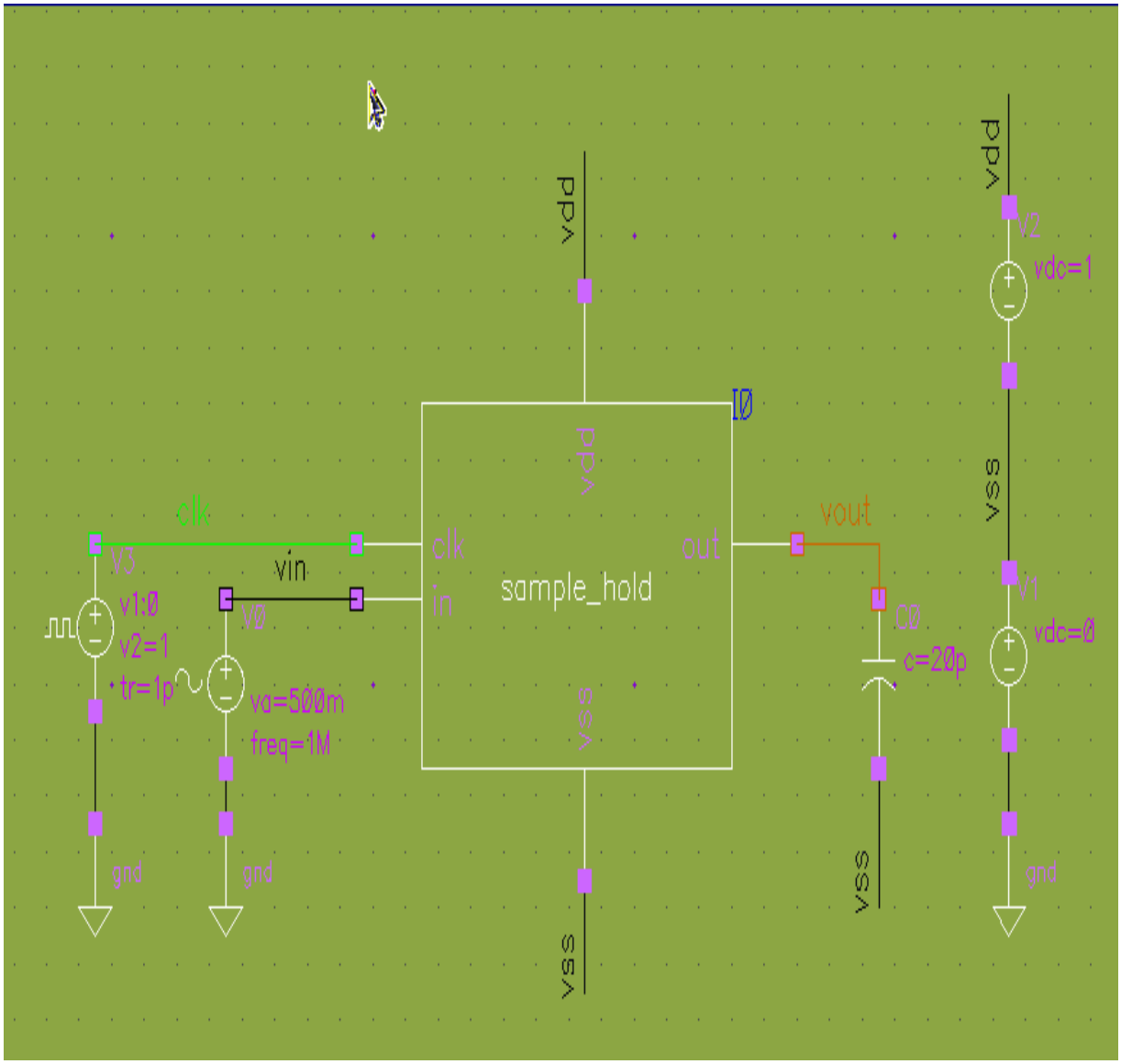


Figure 5.2(b): Schematic diagram of sample and hold circuit

5.3. DIGITAL TO ANALOG CONVERTOR:

CIRCUIT DIAGRAM:

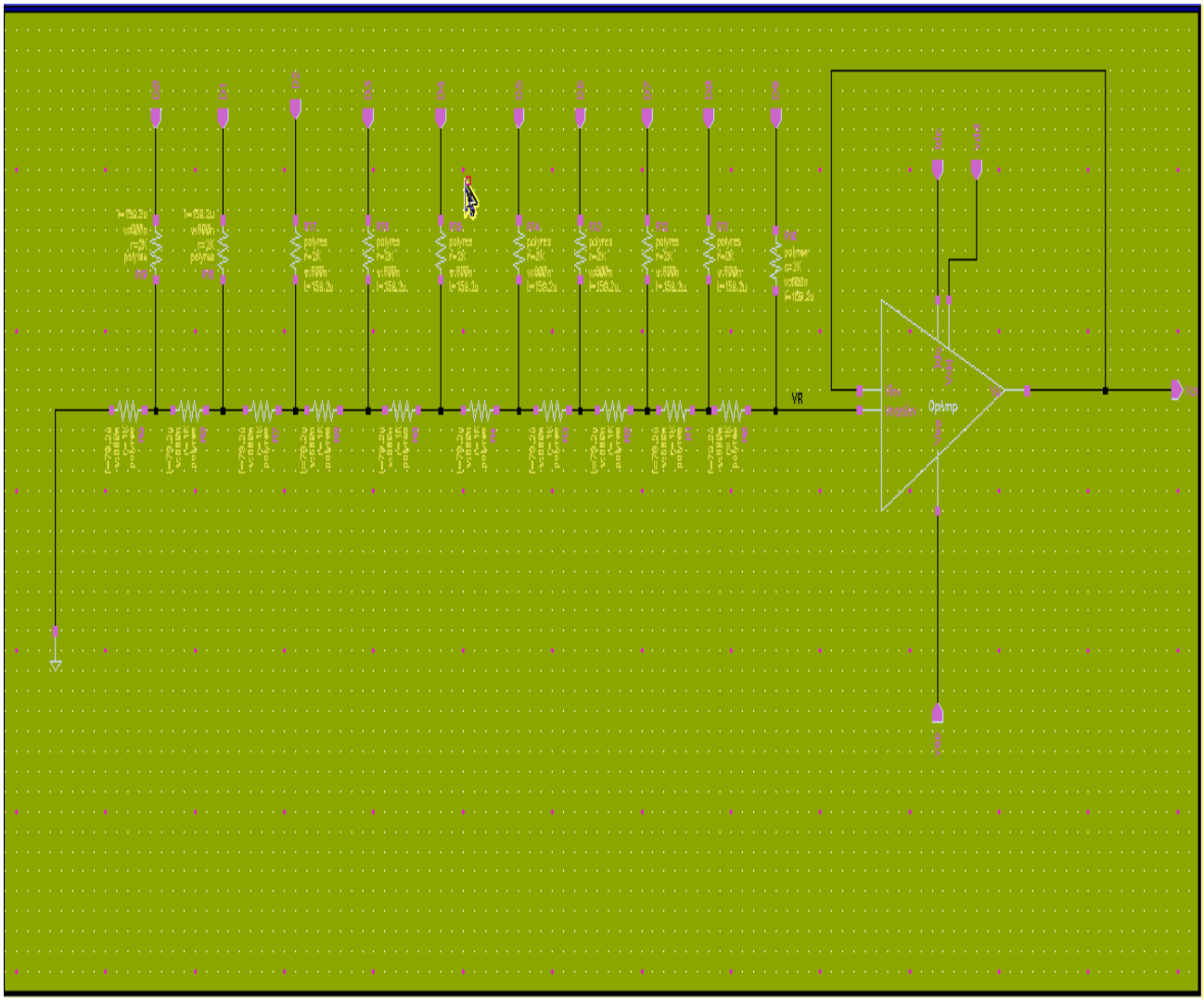


Figure 5.3(a): Circuit diagram of DAC

SCHEMATIC DIAGRAM:

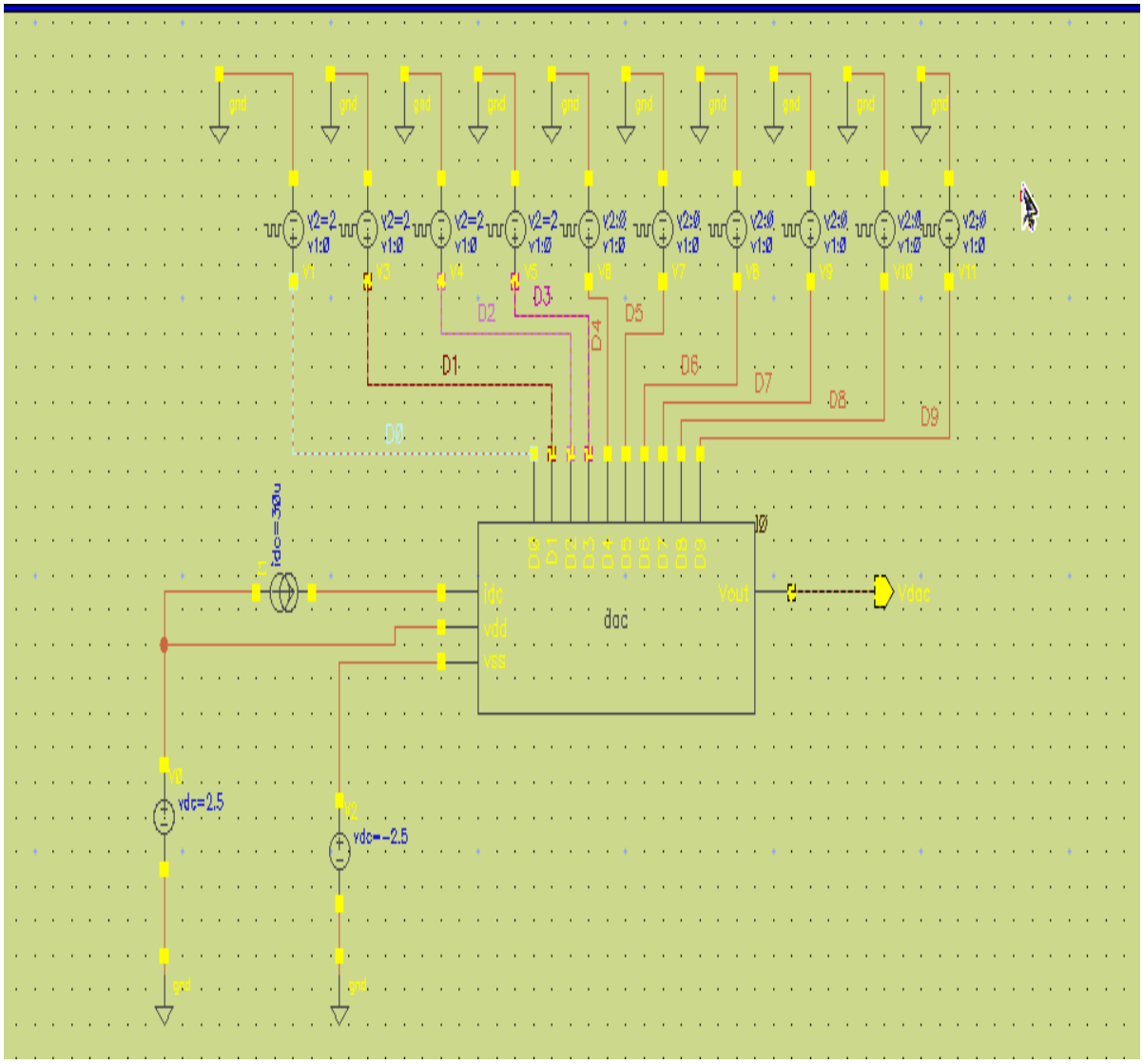


Figure 5.3(b): Schematic diagram of DAC

5.4. SUCCESSIVE APPROXIMATION REGISTER LOGIC:

SCHEMATIC DIAGRAM:

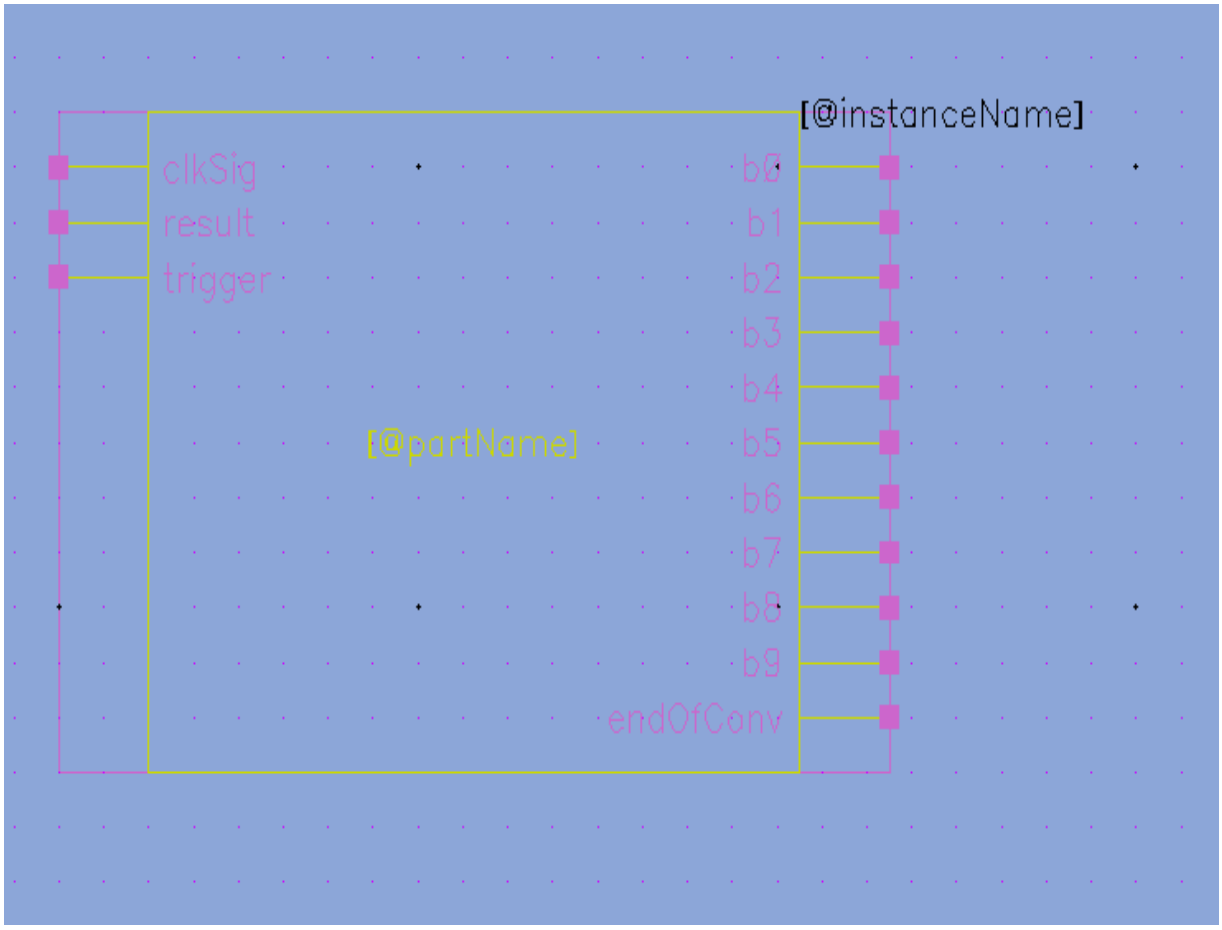


Figure 5.4: SAR logic diagram

5.5. VERILOG CLOCK:

SCHEMATIC DIAGRAM:

Figure 5.5: Verilog Clock Diagram

Chapter 6

RESULT AND DISCUSSION

6.1. DIFFERENTIAL AMPLIFIER:

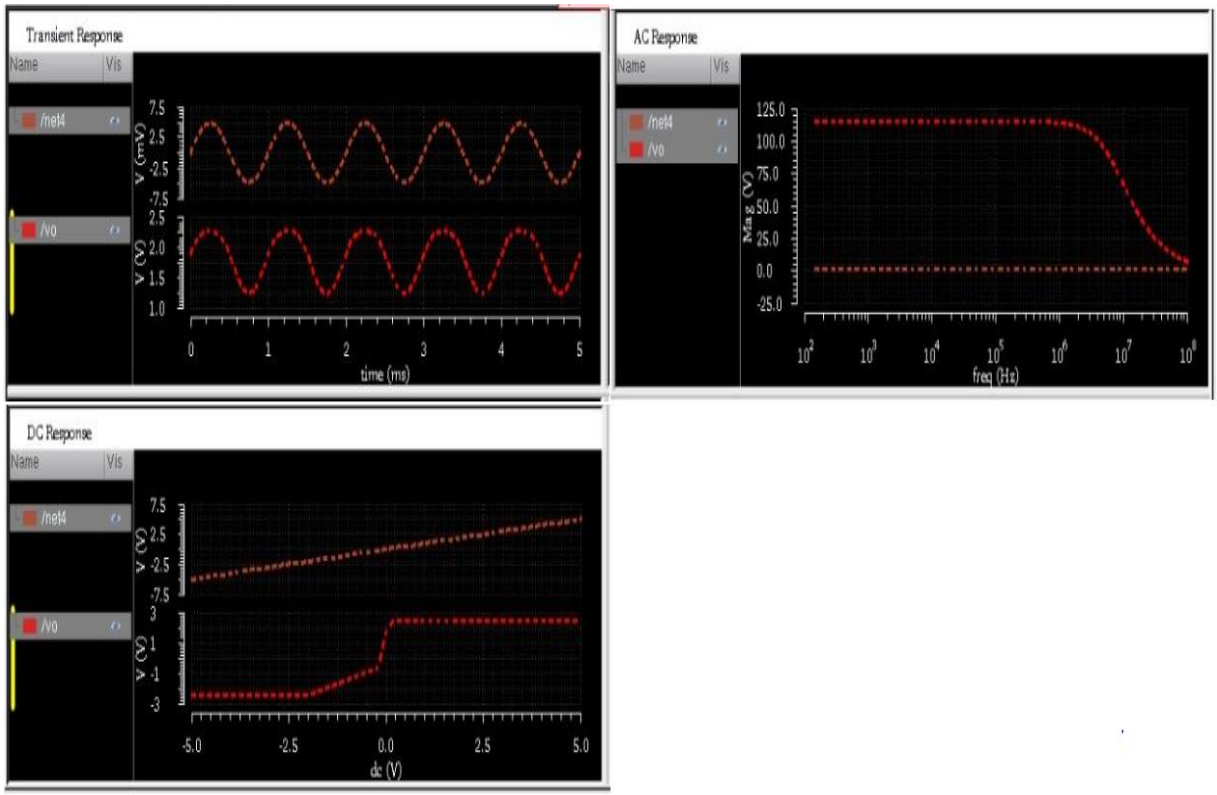


Figure 6.1: Output of differential amplifier

From the above figure, the input to the differrential amplifier is 5mv and the amplified output voltage is 2.5Volts. The bandwidth of the amplifier is 1MHz

6.2. SAMPLE AND HOLD CIRCUIT:

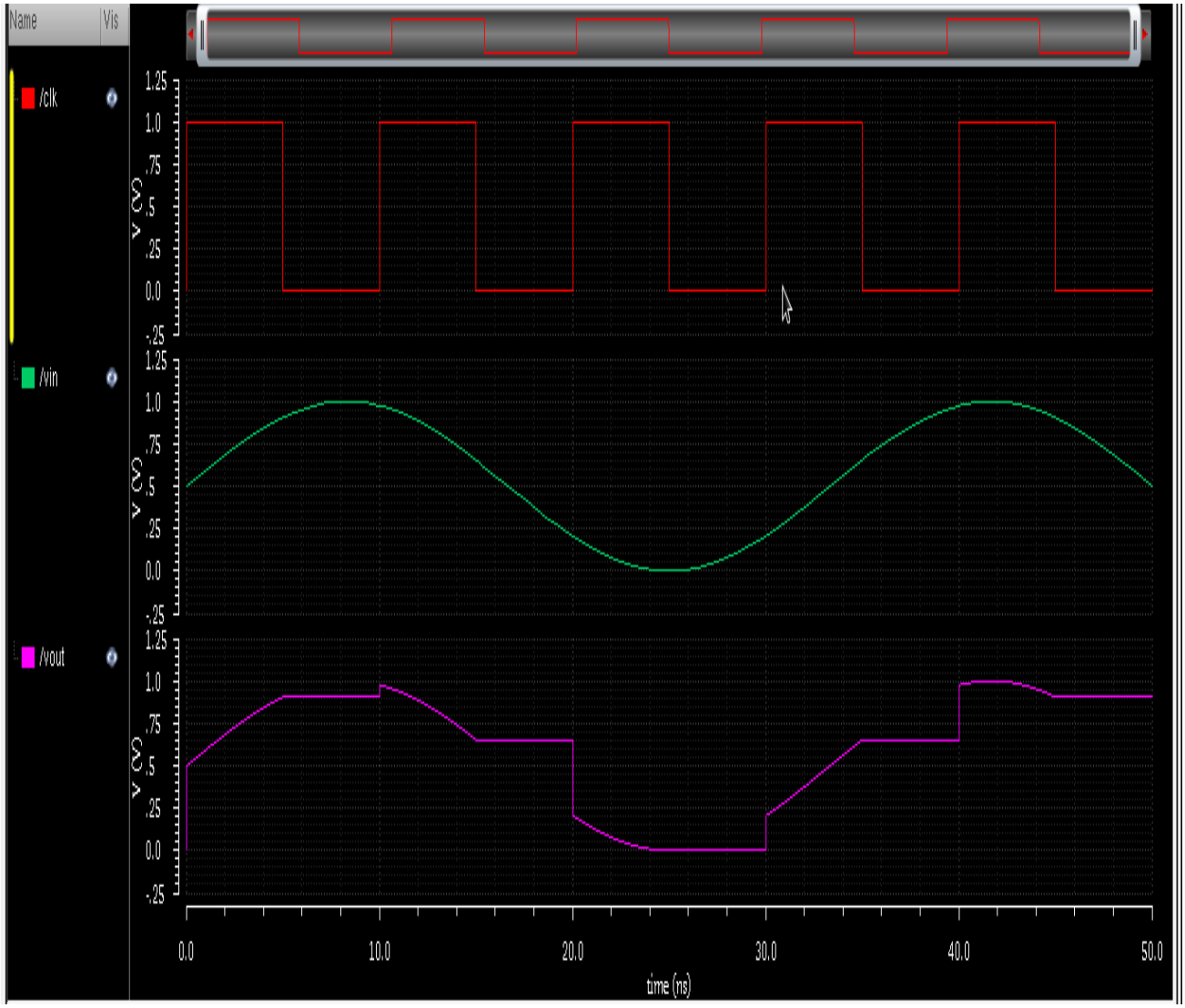


Figure 6.2: Output of sample and hold circuit

Above figure shows the accurate output response of sample and hold circuit.

6.3. DIGITAL TO ANALOG CONVERTOR:

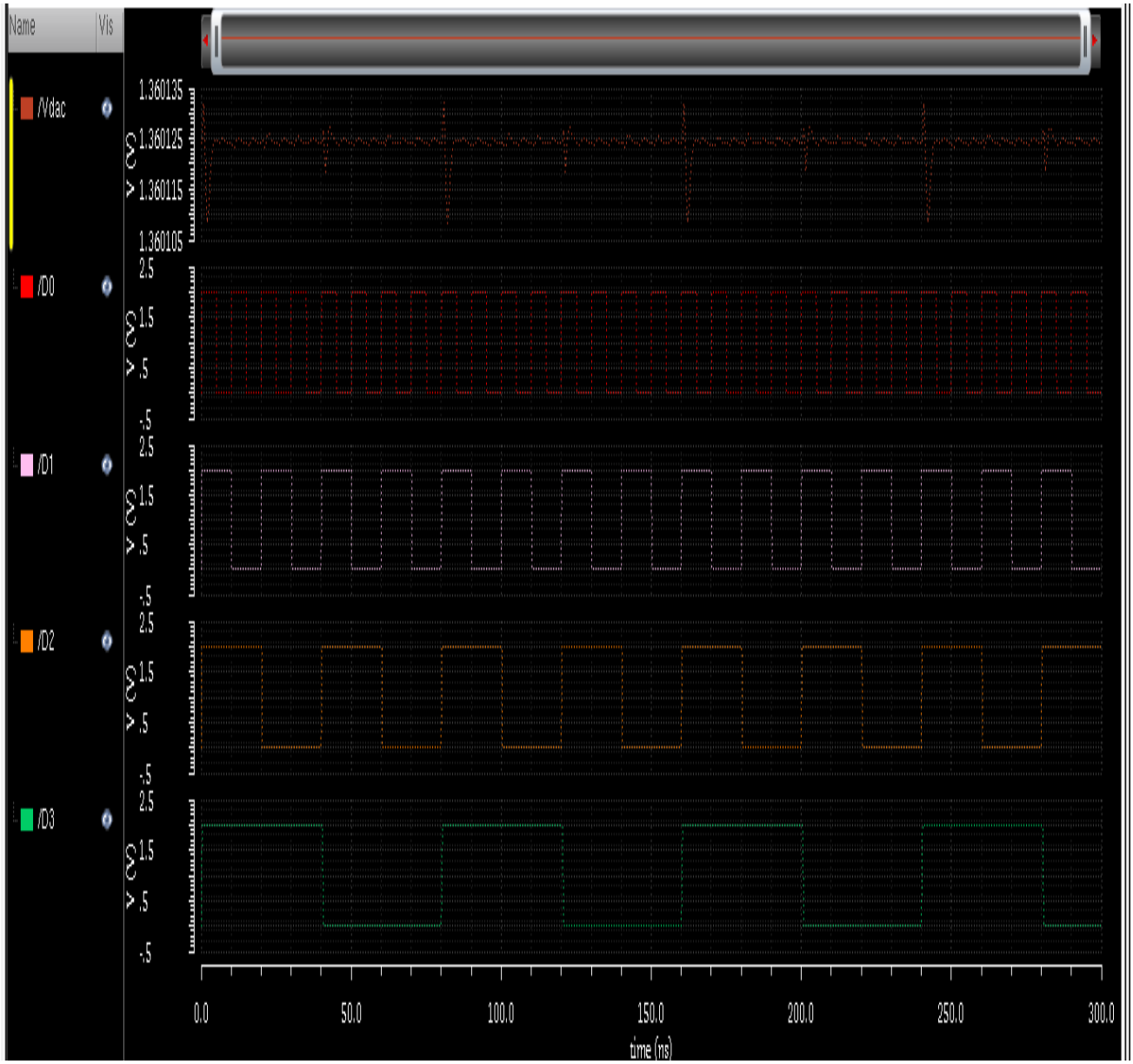


Figure 6.3: Output of DAC

Above figure shows the analog output fot the respective digital input signal.

6.4. EXPERIMENT ON BANDWIDTH

N0=N1=P1=15μ				
P0	Vin	V0	Ad	BW
1 μ	5mV	2.47V	494	2.48MHz
3 μ	5mV	2.46V	492	4.74 MHz
4 μ	5mV	2.45 V	490	4.96 MHz
5 μ	5mV	2.44 V	488	5.02 MHz
6 μ	5mV	2.44 V	488	5.97 MHz

NO=N1=P1=15µ

&

P0=1µ

CIRCUIT DIAGRAM:

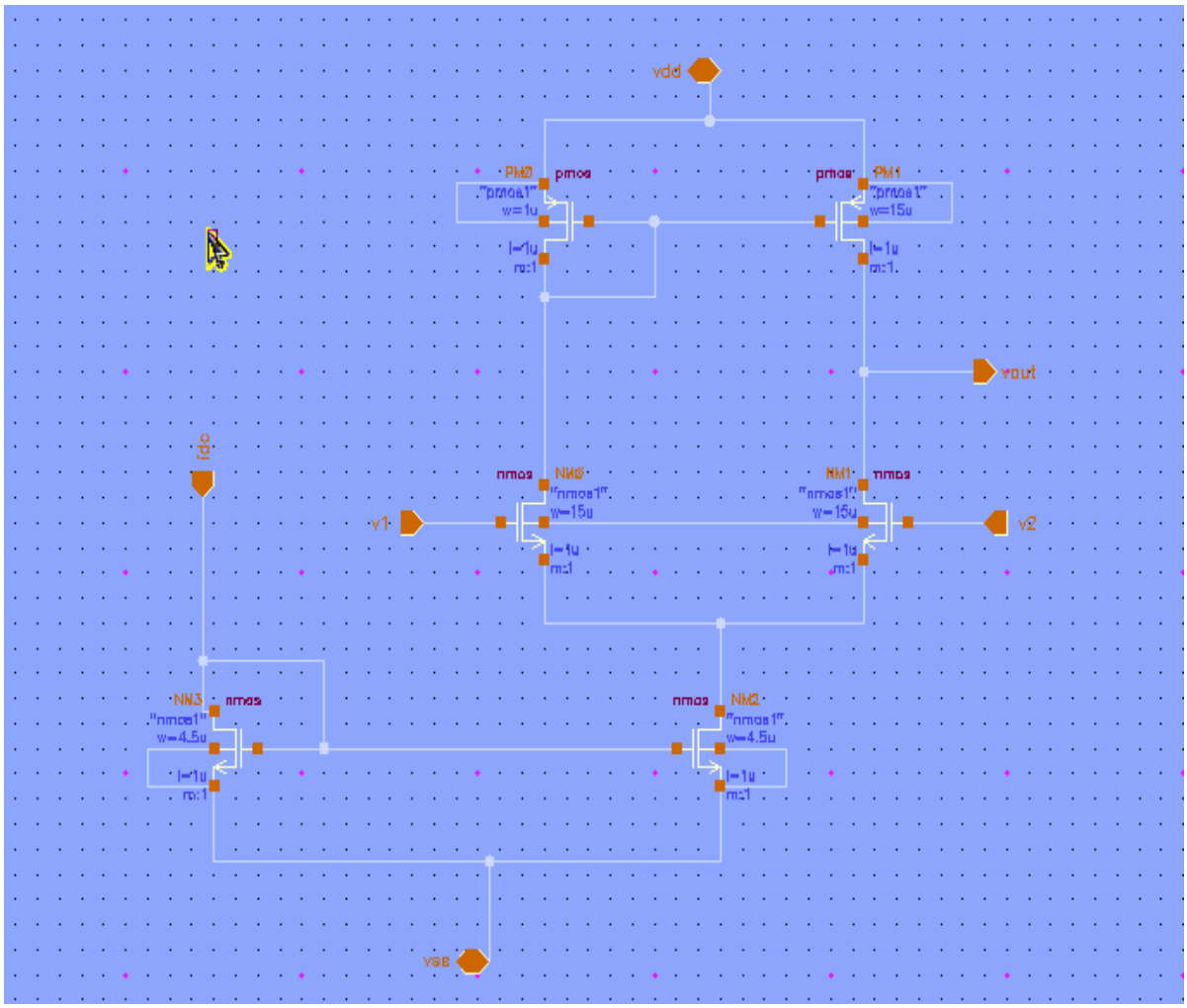


Figure: Circuit Diagram of Differential Amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

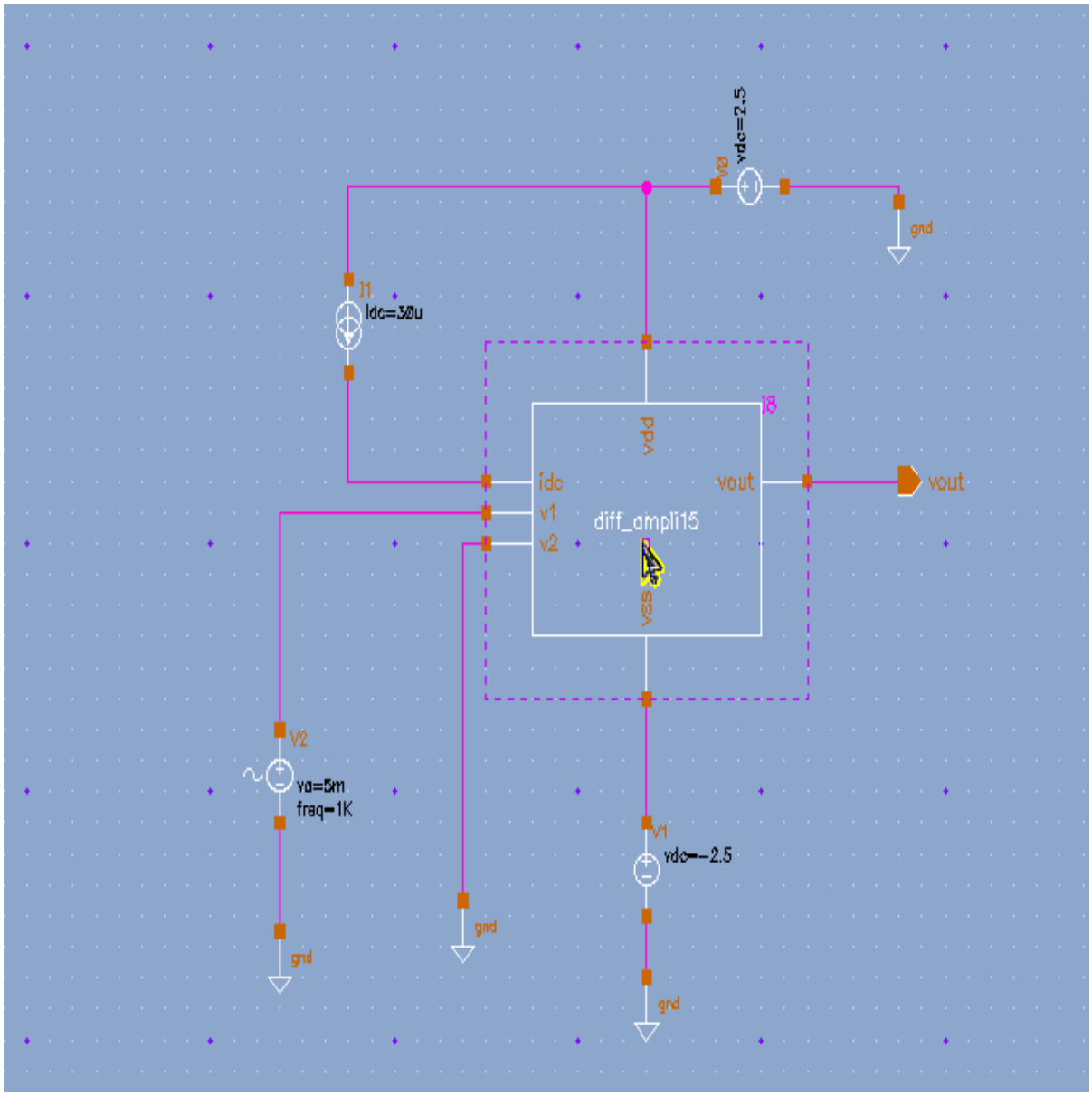


Figure: Schematic diagram of Differential amplifier

Figure shows the schematic diagram of dual input unbalanced output with active load and constant current source differential amplifier.

OUTPUT:

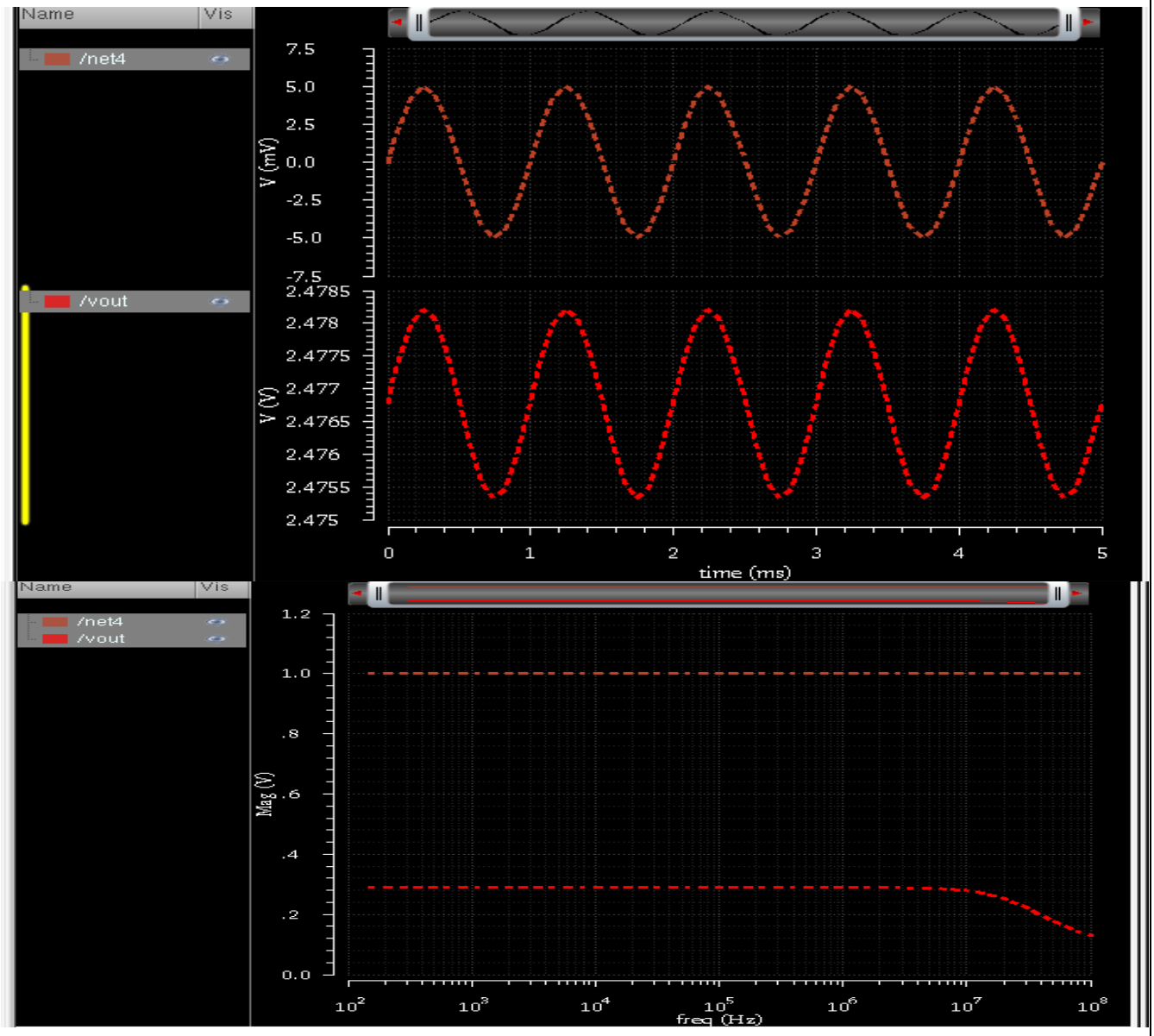


Figure: Output of Differential Amplifier

For the P0 channel width of 1 µm the output voltage is 2.47V and bandwidth is 2.48 MHz with the gain of 494.

NO=N1=P1=15µ

&

P0=3µ

CIRCUIT DIAGRAM:

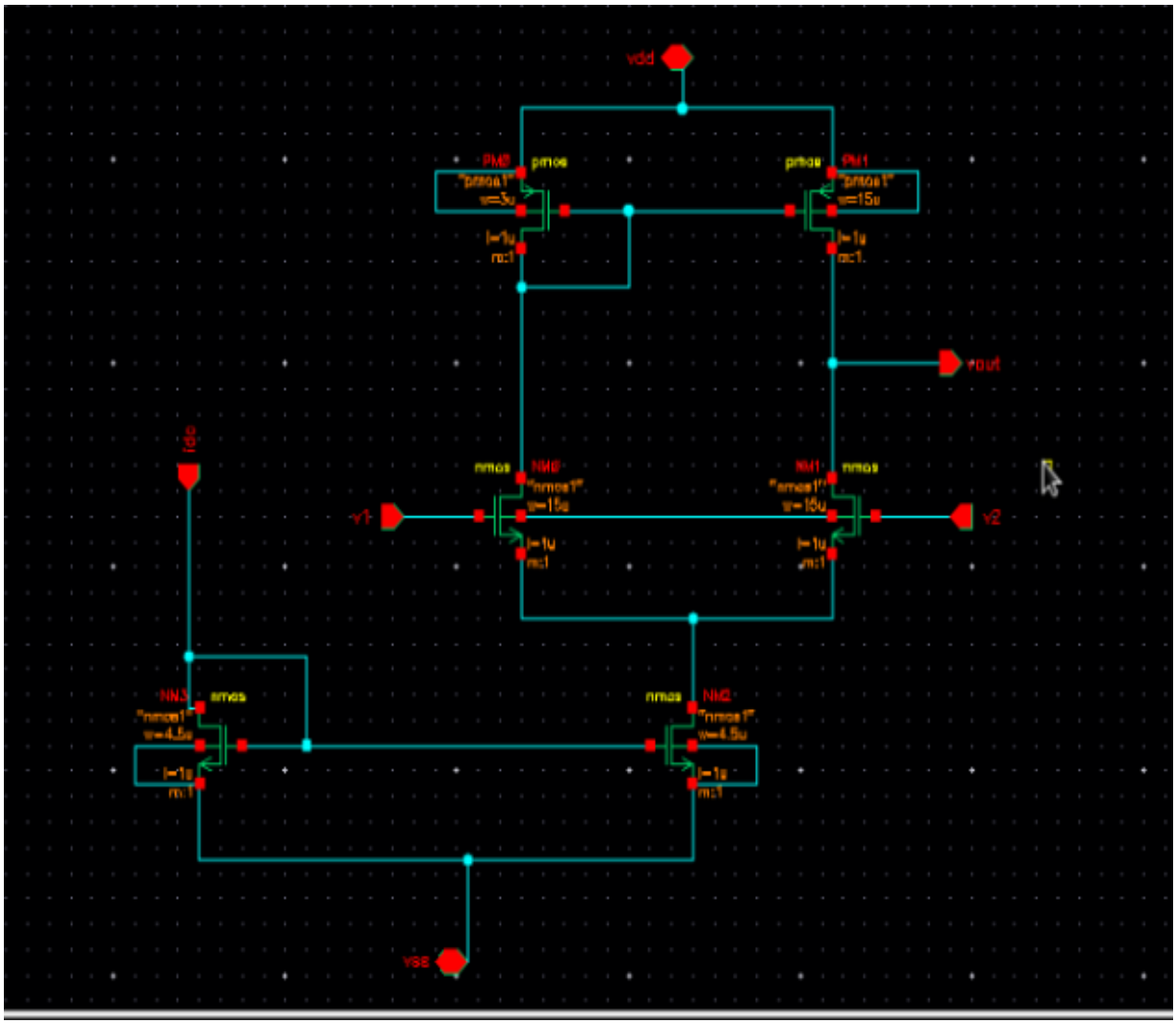


Figure: Circuit Diagram of Differential Amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

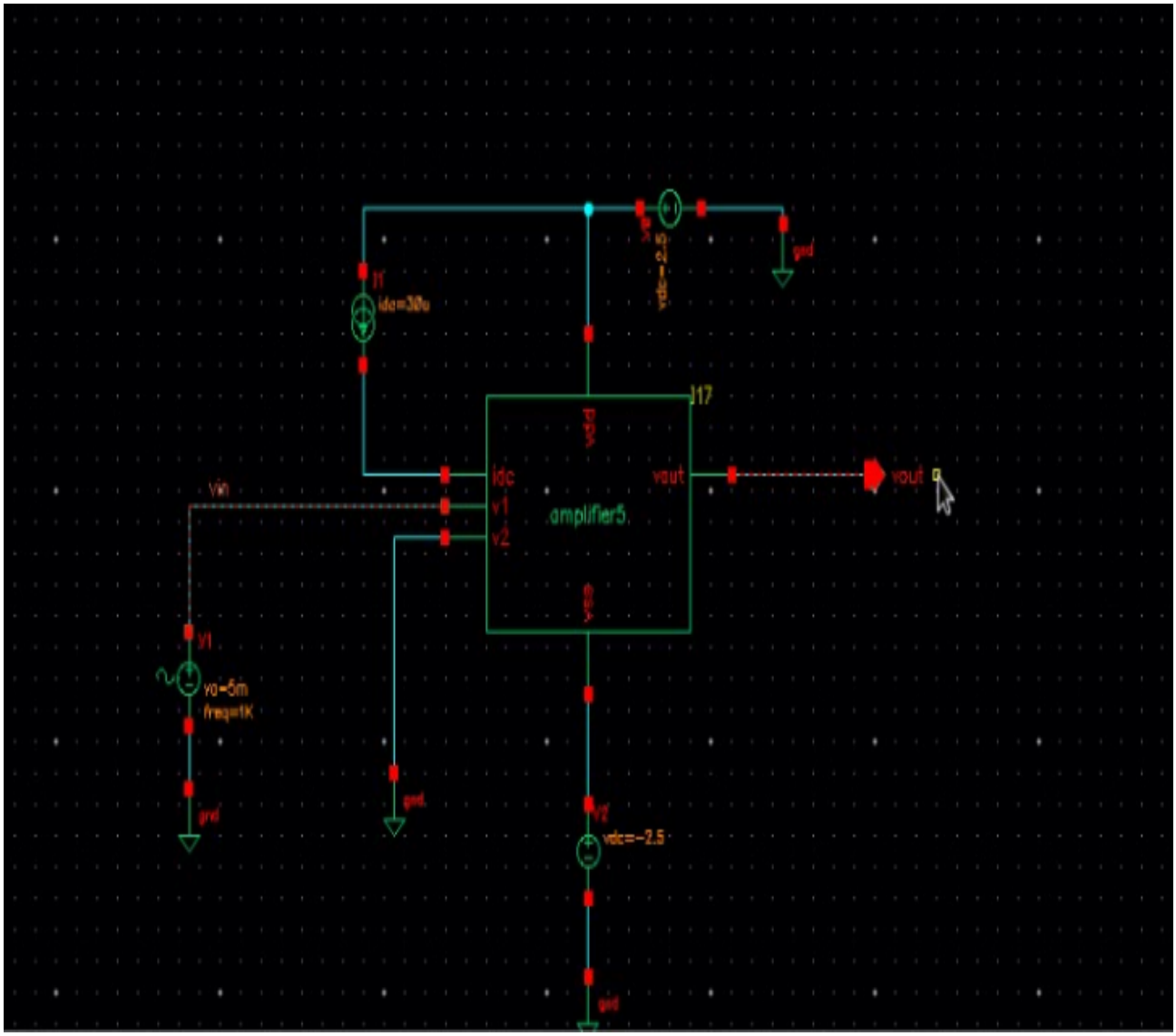


Figure: Schematic diagram of Differential amplifier

Figure shows the schematic diagram of dual input unbalanced output with active load and constant current source differential amplifier.

OUTPUT

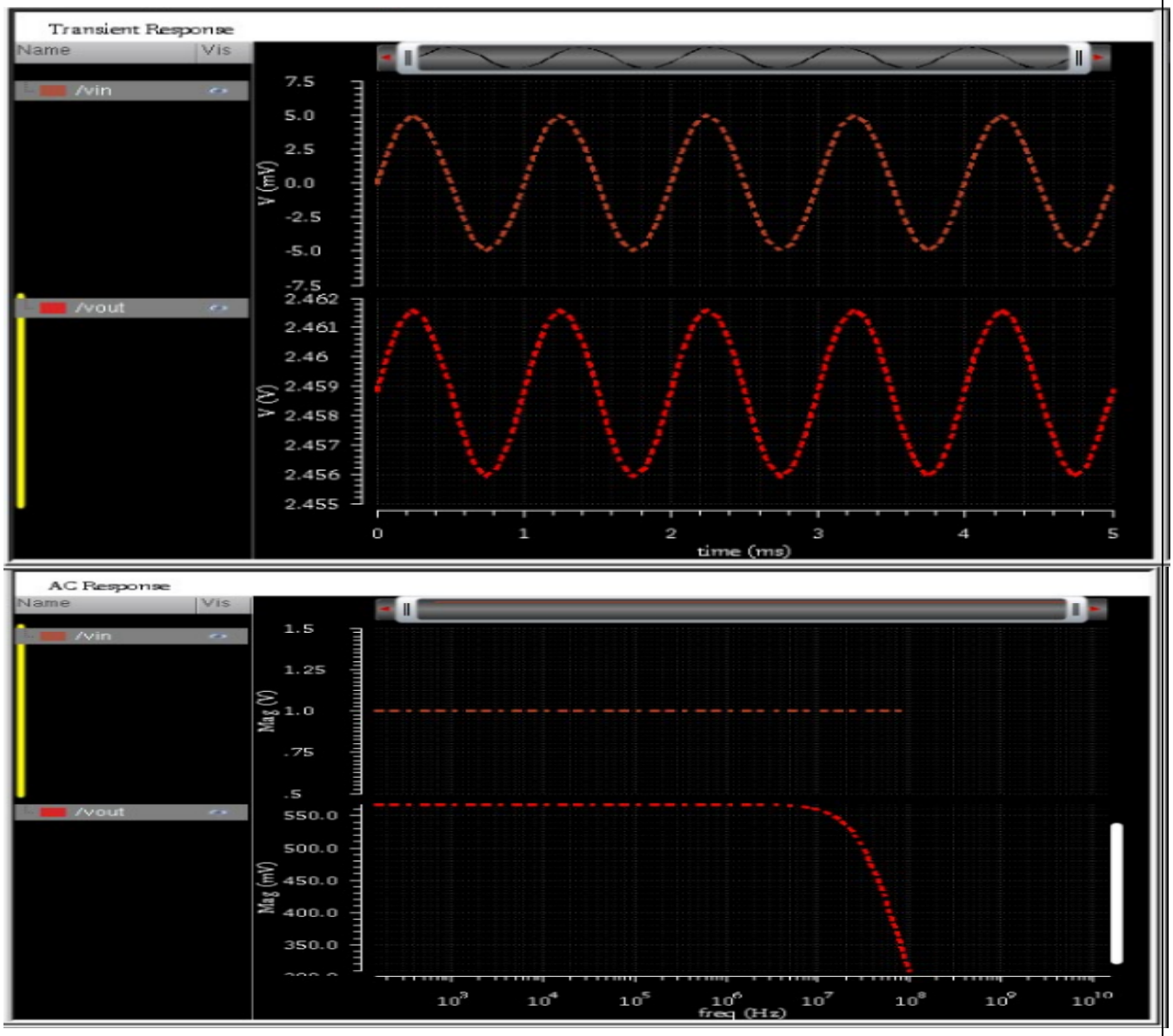


Figure: Output of Differential Amplifier

For the P0 channel width of 3 µm the output voltage is 2.46V and bandwidth is 4.47 MHz with the gain of 492.

NO=N1=P1=15µ

&

P0=4µ

CIRCUIT DIAGRAM:

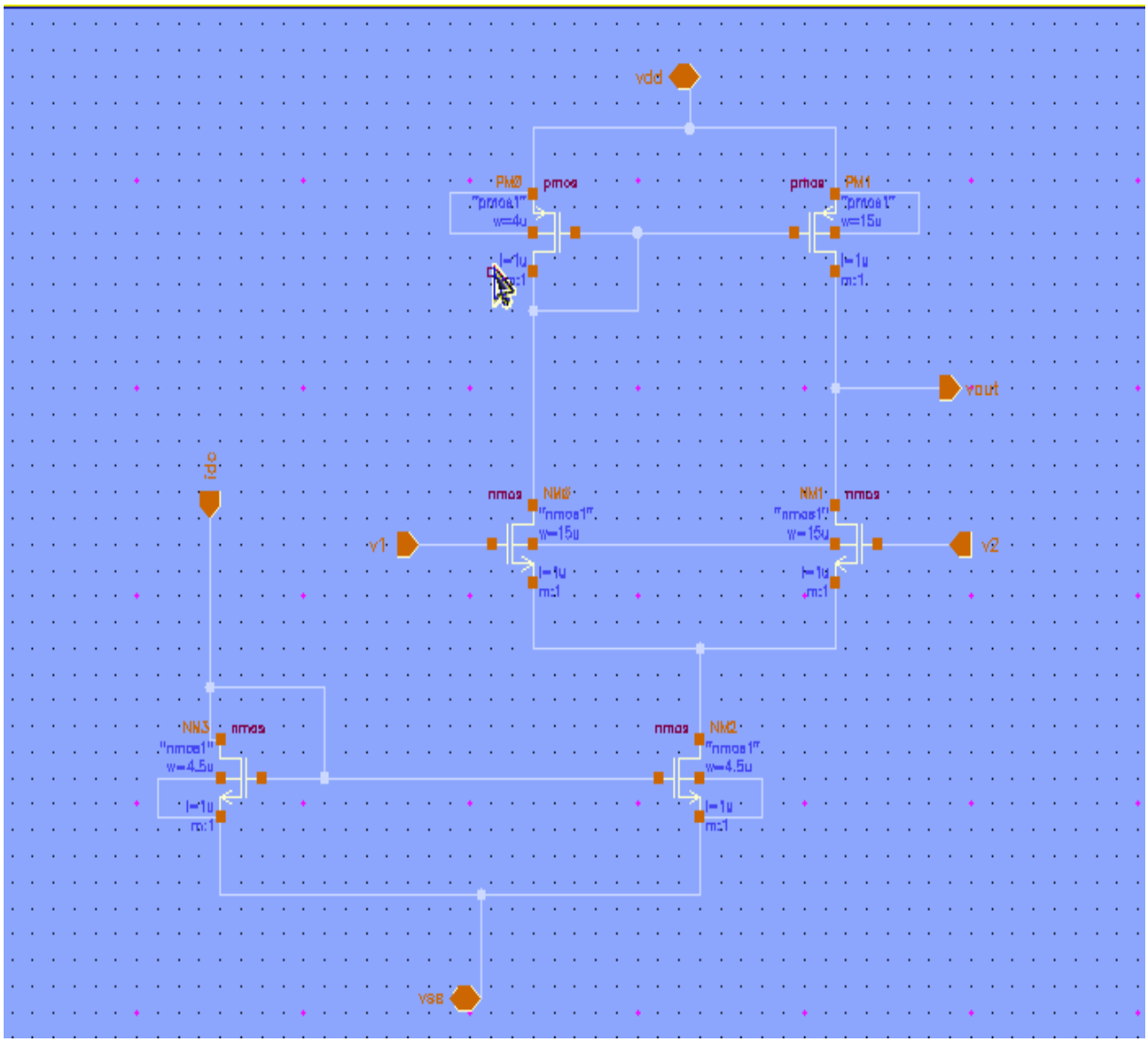


Figure: Circuit Diagram of Differential Amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

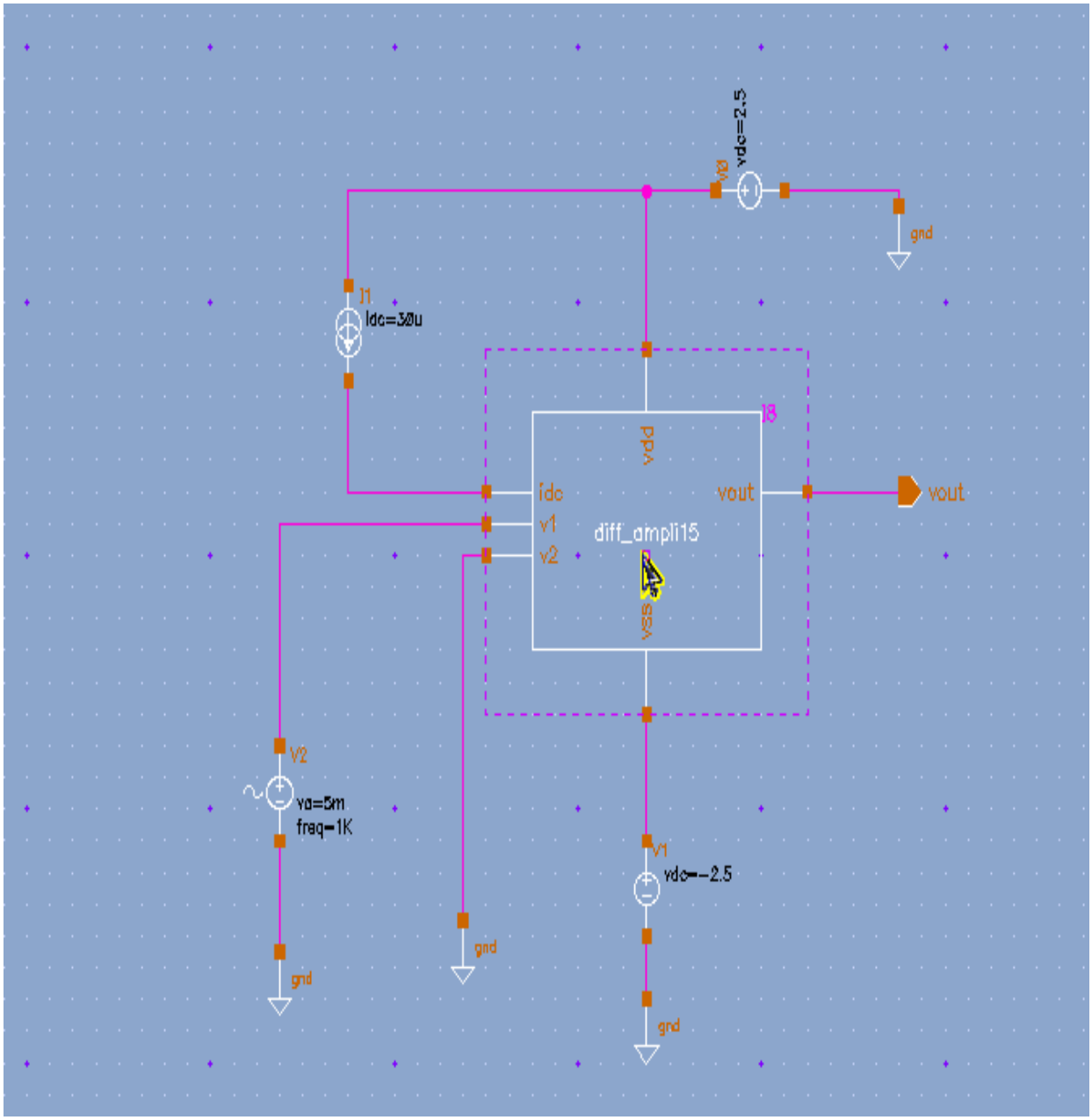


Figure: Schematic diagram of Differential amplifier

Figure shows the schematic diagram of dual input unbalanced output with active load and constant current source differential amplifier.

OUTPUT:

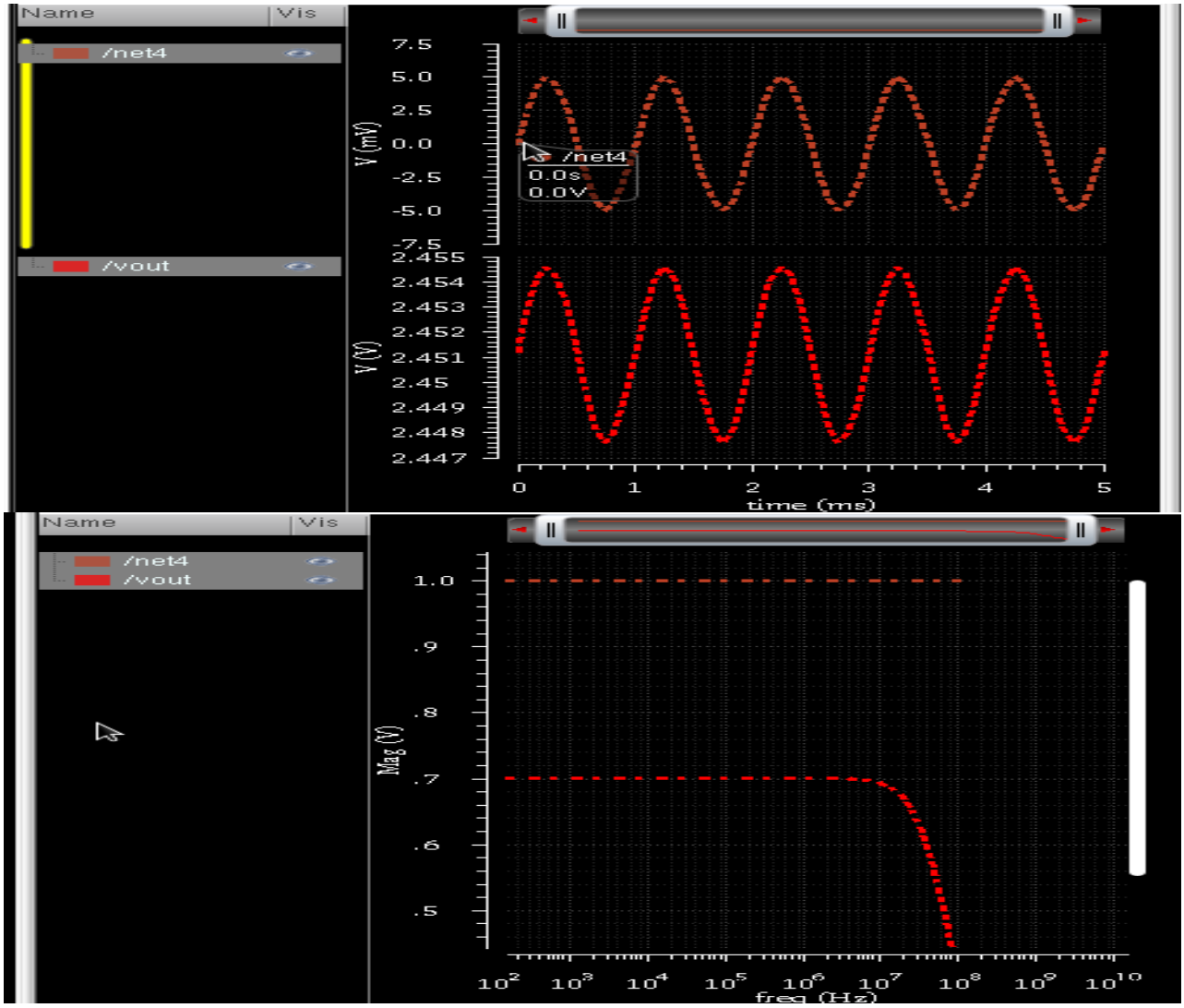


Figure: Output of Differential Amplifier

For the P0 channel width of 4 µm the output voltage is 2.45V and bandwidth is 4.96 MHz with the gain of 490.

NO=N1=P1=15µ

&

P0=5µ

CIRCUIT DIAGRAM:

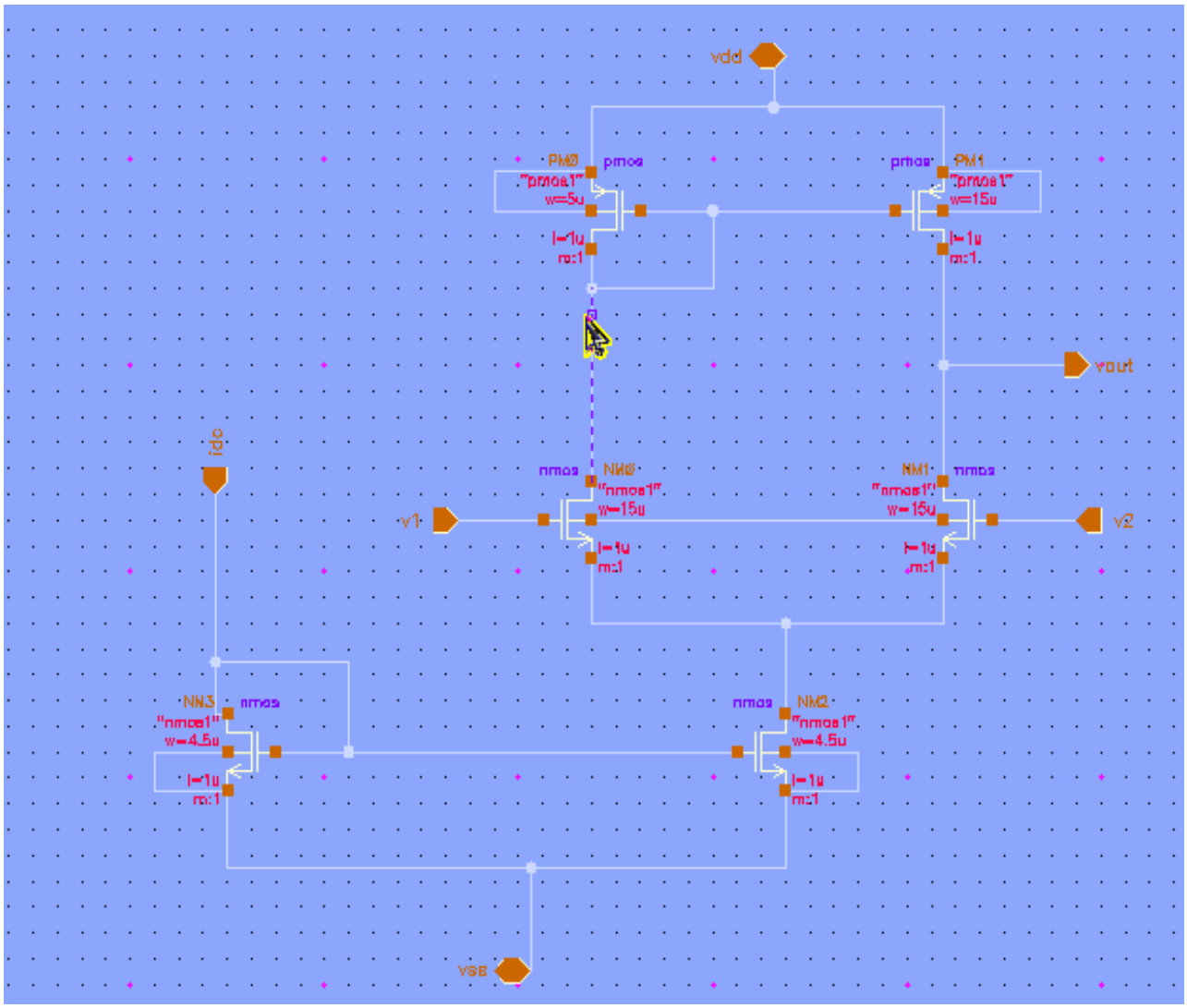


Figure: Circuit Diagram of Differential Amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

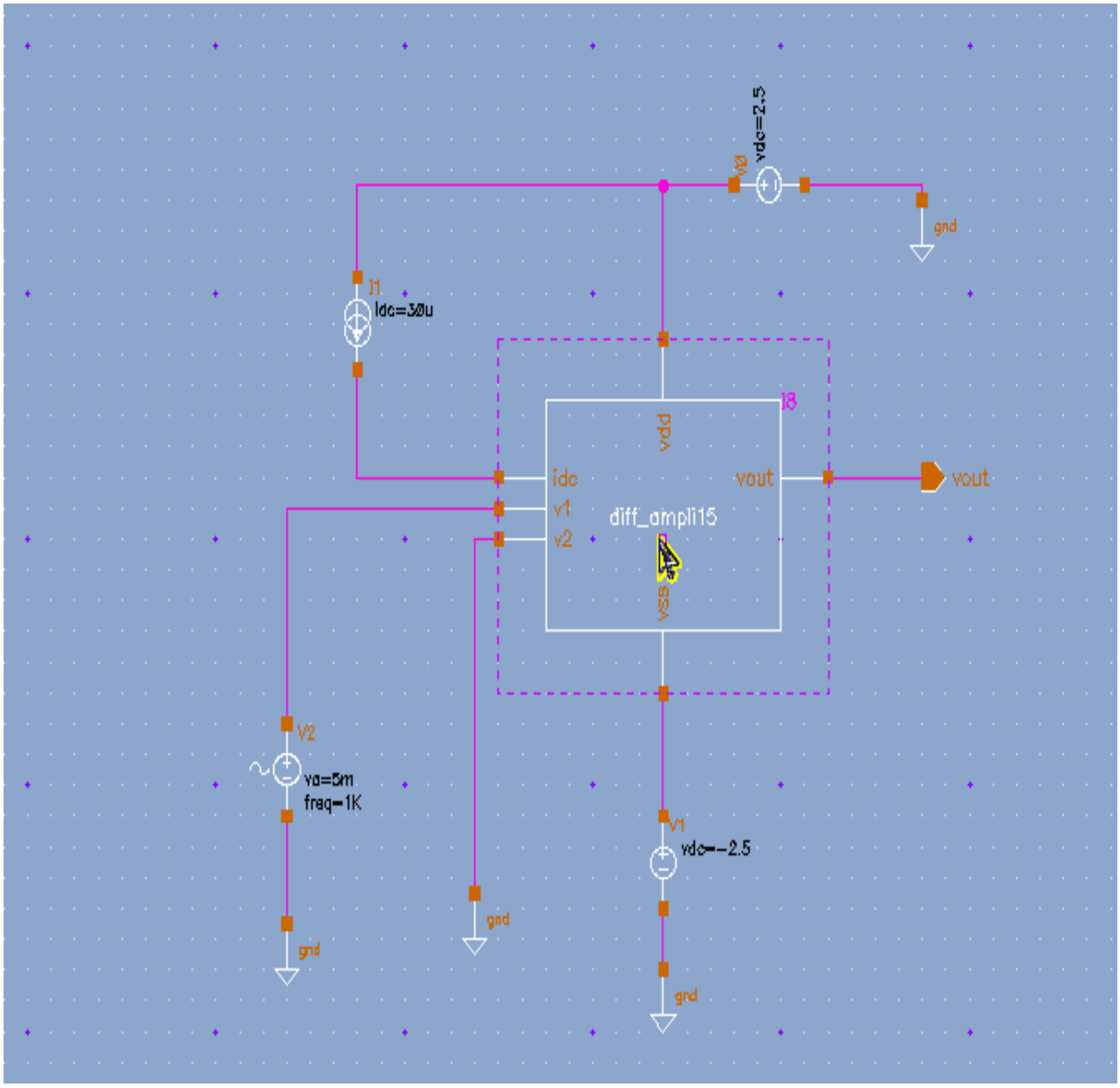


Figure: Schematic diagram of Differential amplifier

Figure shows the schematic diagram of dual input unbalanced output with active load and constant current source differential amplifier.

OUTPUT:

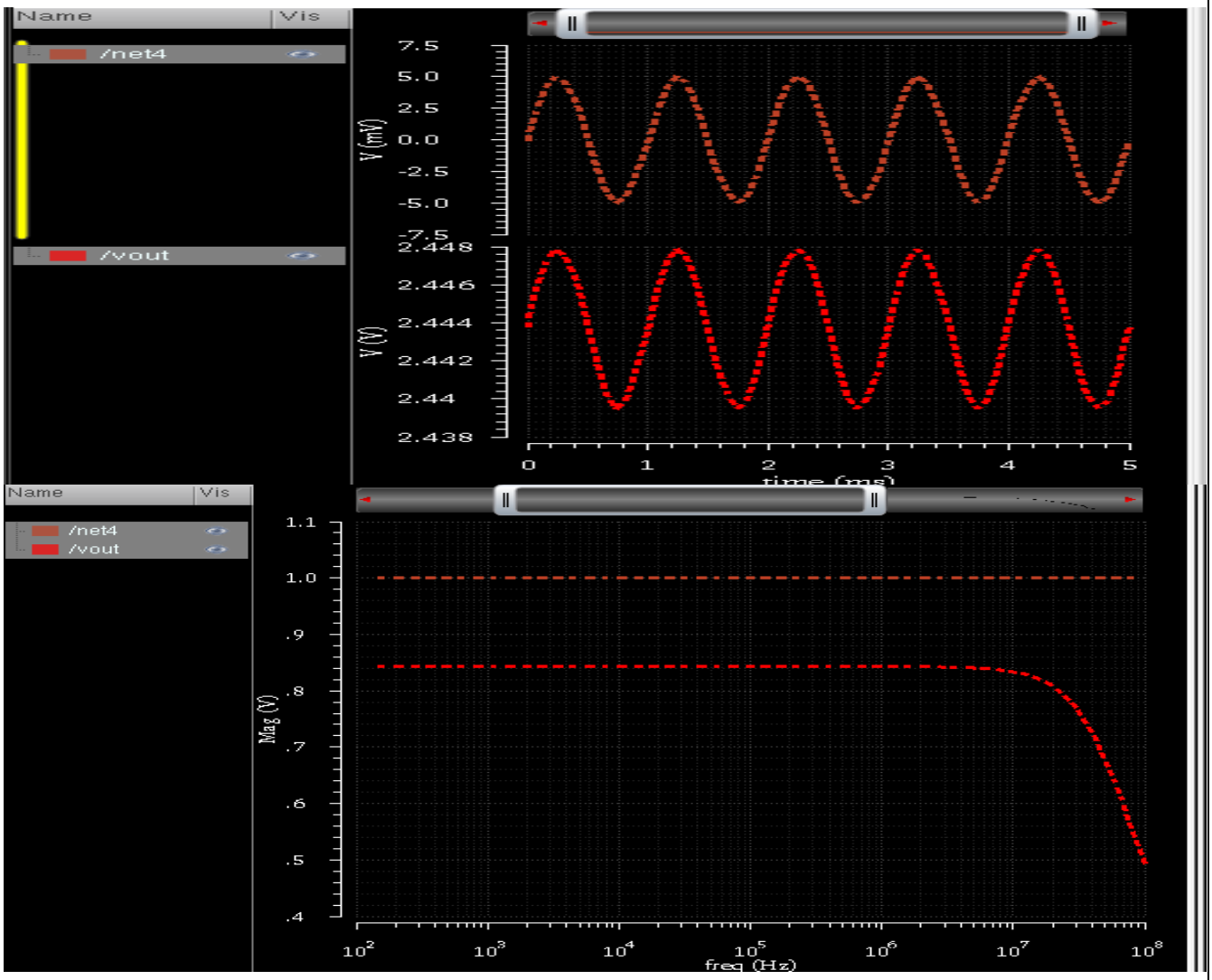


Figure: Output of Differential Amplifier

For the P0 channel width of 5 µm the output voltage is 2.44V and bandwidth is 5.02 MHz with the gain of 488.

NO=N1=P1=15µ

&

P0=6µ

CIRCUIT DIAGRAM:

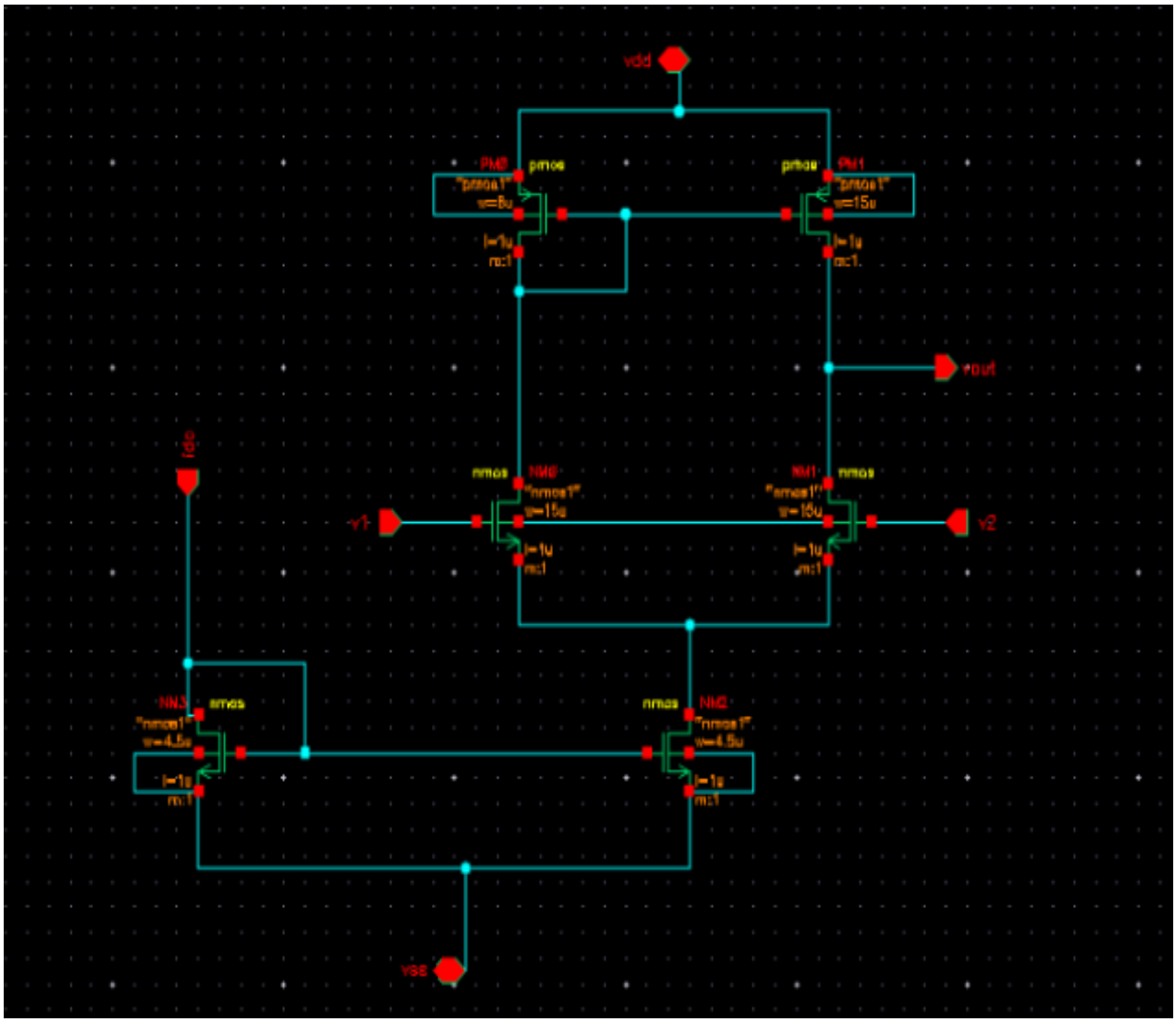


Figure: Circuit Diagram of Differential Amplifier

Figure shows the circuit diagram of dual input unbalanced output with active load and constant current source differential amplifier.

SCHEMATIC DIAGRAM:

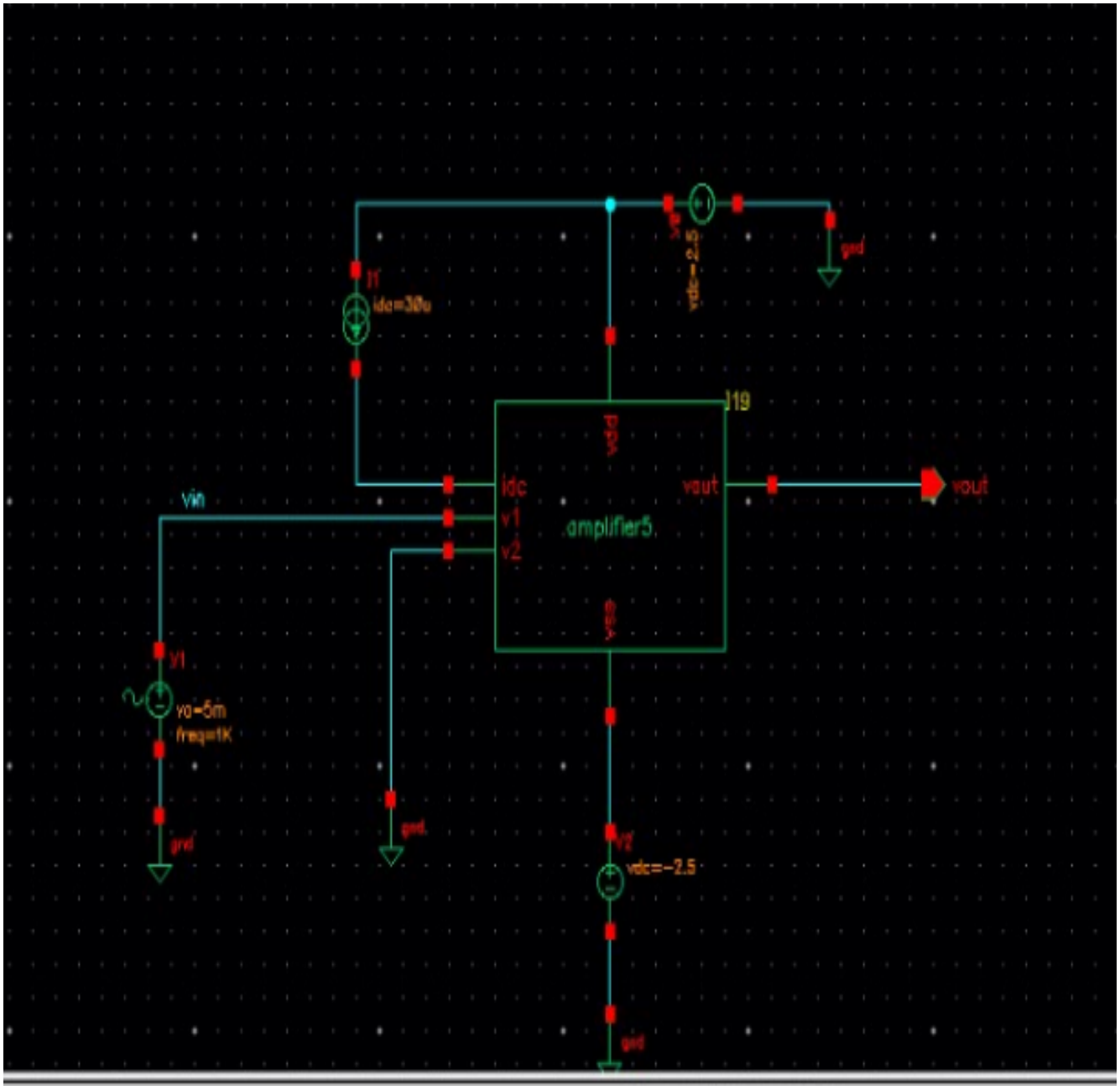


Figure: Schematic diagram of Differential amplifier

Figure shows the schematic diagram of dual input unbalanced output with active load and constant current source differential amplifier.

OUTPUT:

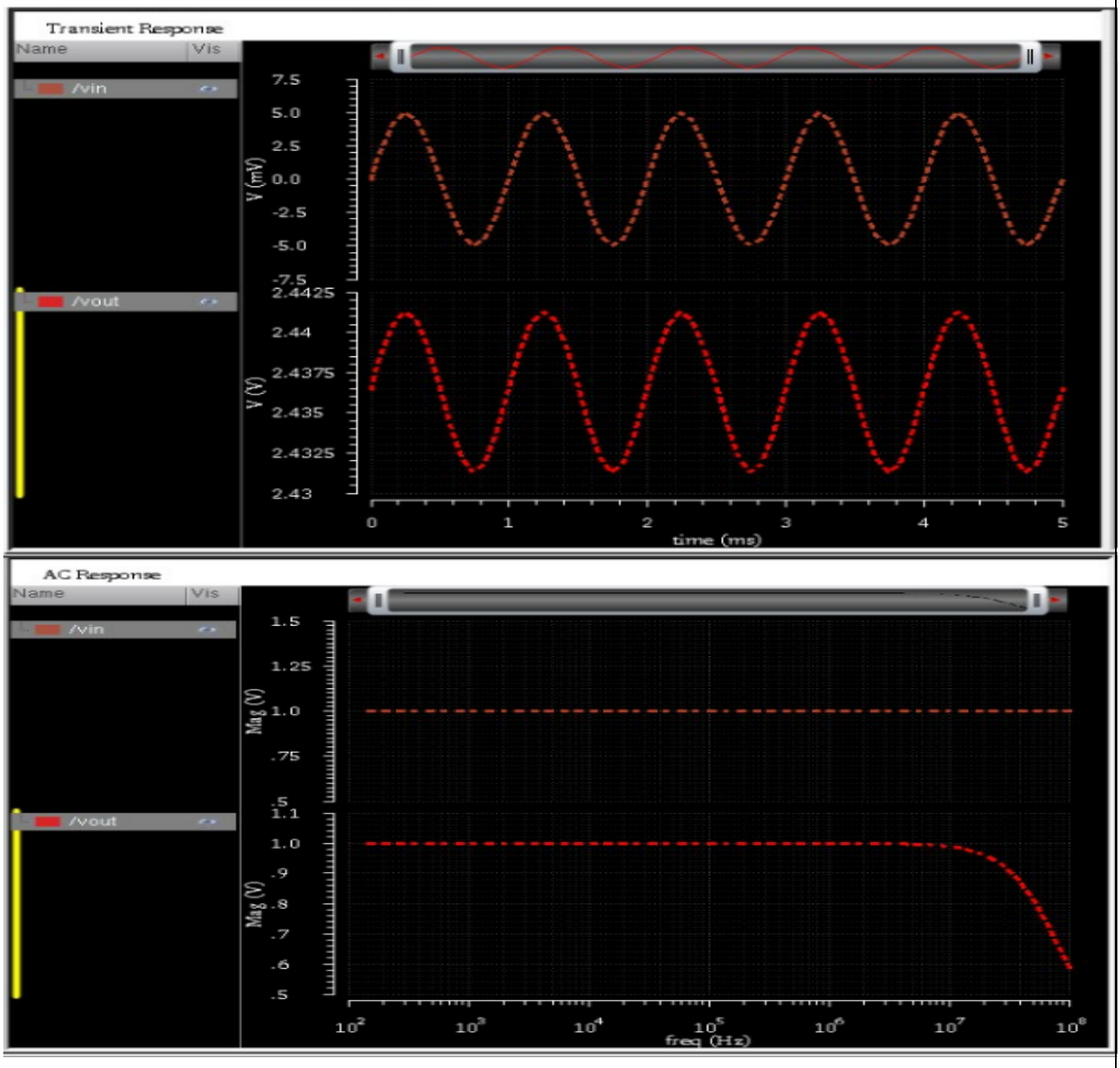
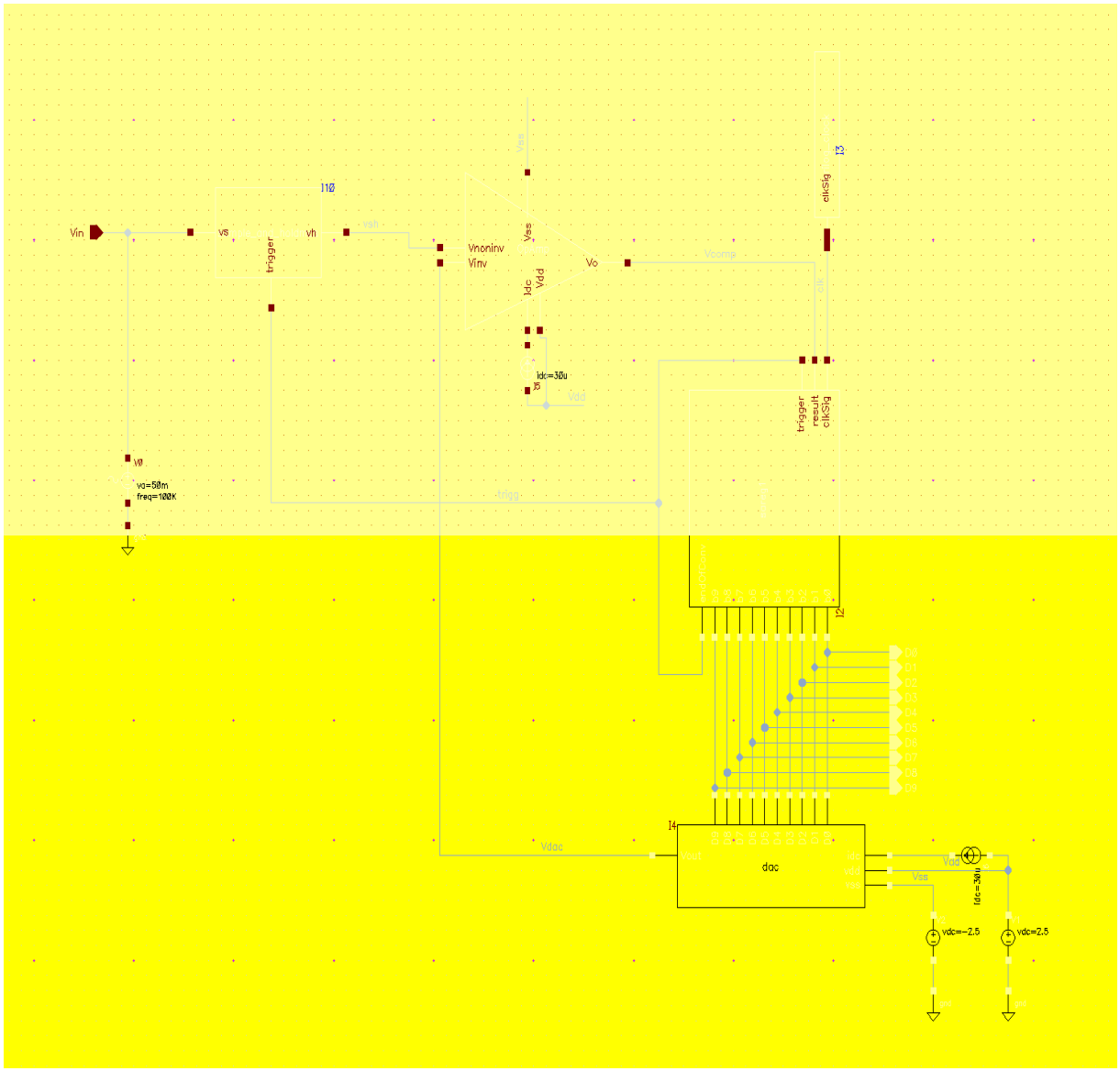


Figure: Output of Differential Amplifier

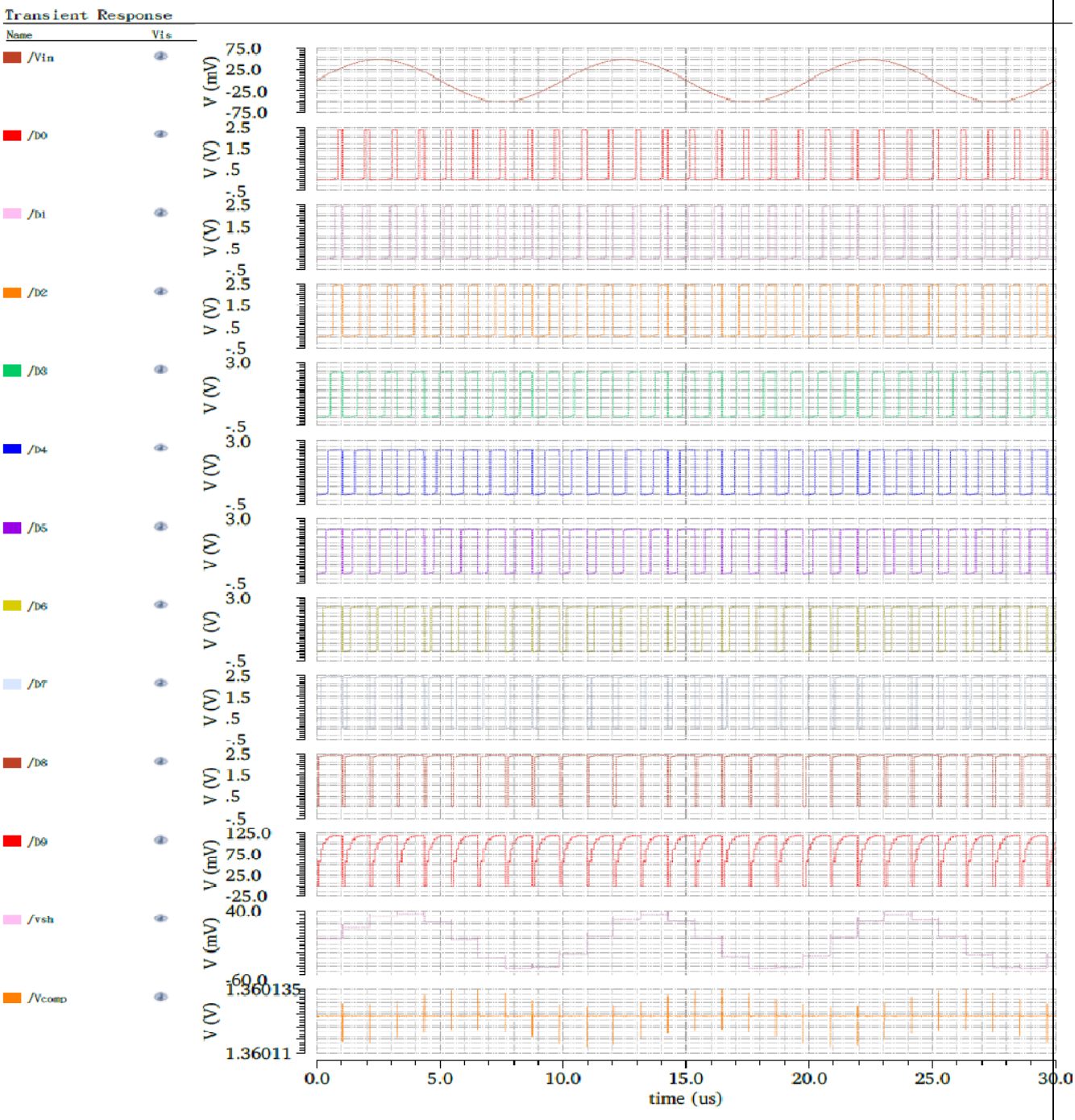
For the P0 channel width of 6µm the output voltage is 2.44V and bandwidth is 5.97 MHz with the gain of 488.

6.5 ANALOG TO DIGITAL CONVERTER

6.5.1 SCHEMATIC DIAGRAM:



6.5.2 OUTPUT:


Transient Response
Name
Vis
/Vin
/D0
/D1
/D2
/D3
/D4
/D5
/D6
/D7
/D8
/D9
/vsh
/Vcomp
V (mV)
V (V)
75.0
25.0
-25.0
-75.0
2.5
1.5
.5
-.5
3.0
125.0
40.0
-60.0
1.360135
1.36011
0.0
5.0
10.0
15.0
20.0
25.0
30.0
time (us)

Chapter 7

CONCLUSION & FUTURE SCOPE

Hence we have successfully designed 10 bit Successive Approximation Register (SAR) Analog to Digital Converter with 2.5 volts power supply at 180 nm technology using cadence. In wireless communication Bandwidth is an important parameter. Initially the bandwidth of a differential amplifier was 1 MHz, but after doing research from various IEEE papers on the bandwidth, we increased the bandwidth from 1MHz to 5MHz with slightly decrease in gain. By increasing the channel width of the NMOS transistor, bandwidth increases but the gain decreases.

Power dissipation is an important factor in increasing the efficiency of wireless devices. Furthermore, the implementation can be done to reduce the power dissipation. Power dissipation can be reduced by using single capacitor unit in the place of many capacitor switches which are present in capacitive DAC. In the current project we are using R2R ladder DAC which requires more space in chip designing while capacitors require less space as compare to resistor. This will further improve the efficiency and reduce the size of the ADC. The power dissipation mainly comprises by capacitor and comparator. The tri level comparator can be used to reduce the power dissipation.

Chapter8

REFERRENCE

[1] Prakash Harikumar, *Student Member, IEEE, J Jacob Wikner, Member, IEEE,* and Atila Alvandpour, "A 0.4 V, sub-nW, 8-bit 1 kS/s SAR ADC in 65 nm CMOS for Wireless Sensor Applications ," IEEE Transactions on Circuits and Systems, 2015.

[2] Yan-Jiun Chen, Kwuang-Han Chang, and Chih-Cheng Hsieh, "A 2.02–5.16 fJ/Conversion Step 10 Bit Hybrid Coarse-Fine SAR ADC With Time-Domain Quantizer in 90 nm CMOS, IEEE Journal Of Solid-state Circuits, VOL. 51, NO. 2, February 2016.

[3] Gregor Tretter, Mohammad Mahdi Khafaji, David Fritsche, Corrado Carta*, Member, IEEE,* And Frank Ellinger, "Design And Characterization Of A 3-bit 24-GS/S Flash ADC In 28-nm Low-power Digital CMOS," IEEE Transa-ctions On Microwave Theory And Techniques, VOL. 64, No. 4, April 2016.

[4] Johannes Digel, Markus Gr¨ozing And Manf red Berroth, "A 10 Bit 90 MS/S SAR ADC In A 65 Nm CMOS Technology," IEEE Transac tions On Very Large Scale Integration (VLSI) Systems 2016.

[5] Yung-Hui Chung*, Chia-Wei Yen, and Meng- Hsuan Wu*, "A 24-*μW 12-bit 1-MS/s SAR ADC With Two-Step* Decision DAC Switching in 110-nm CMOS," IEEE Transactions On Very Large Scale Integration (VLSI) Systems

[6] Long Chen, Kareem Ragab, Xiyuan Tang, Jeonggoo Song, Arindam Sanyal, and Nan Sun, "A 0.95-mW 6-b 700-MS/s Single-Channel Loop-Unrolled SAR ADC in 40-nm CMOS," IEEE Transactions on Circuits and Systems, 2016.

[7] James W. Haslett, "5-bit 5-GS/s Noninterleaved Time-Based ADC in 65-nm CMOS for Radio-Astronomy Applications." Very Large Scale Integration (VLSI) Systems, IEEE International Symposium, 2016.

Appendix A

Verilog code for verilog clock:

```
// Created by ihdl

module Verilog_clock (clkSig);

output clkSig;

reg clkSig;

initial

clkSig= 0;

always

 #50 clkSig =~clkSig;

endmodule
```

Verilog code for SAR logic:

```
// Created by ihdl

`timescale 1ns/100ps

module sareg1(clkSig, b0, b1, b2, b3, b4, b5, b6, b7,  b8, b9, trigger,
endOfConv,result);

  input result;

  input clkSig;

  input trigger;

  output endOfConv;

  output  b0, b1, b2, b3, b4, b5, b6, b7,  b8, b9;

  reg  b0, b1, b2, b3, b4, b5, b6, b7,  b8, b9;

  reg endOfConv;

  wire clkSig;

//  logic  b0, b1, b2, b3;
```

```
// logic result;

  integer position;

        initial begin

                position = 9;

                endOfConv = 0;

                b0 = 0;

                b1 = 0;

                b2 = 0;

                b3 = 0;

                b4 = 0;

                b5 = 0;

                b6 = 0;

                b7 = 0;

                b8 = 0;
```

```
        b9 = 0;
end
always begin
        @(posedge(trigger)) begin
        #5 position = 9;
        endOfConv = 0;
        b0 = 0;
        b1 = 0;
        b2 = 0;
        b3 = 0;
        b4 = 0;
        b5 = 0;
        b6 = 0;
        b7 = 0;
```

```
        b8 = 0;
        b9 = 0;
        end
end
always begin
@(posedge(clkSig)) begin
            if(position == 9) begin
              b8 = 1;
              if(result==0) begin
                    b9 = 0;
              end
    end
        else if(position == 8) begin
              b7 = 1;
```

```
        if(result==0) begin
                b8 = 0;
        end
 end
else if(position == 7) begin
        b6 = 1;
        if(result==0) begin
                b7 = 0;
        end
 end
else if(position == 6) begin
        b5 = 1;
        if(result==0) begin
                b6 = 0;
```

```
        end
    end
    else if(position == 5) begin
        b4 = 1;
        if(result==0) begin
            b5 = 0;
        end
    end
    else if(position == 4) begin
        b3 = 1;
        if(result==0) begin
            b4 = 0;
        end
    end
```

```
else if(position == 3) begin
        b2 = 1;
        if(result==0) begin
                b3 = 0;
        end
 end
else if(position == 2) begin
        b1 = 1;
        if(result==0) begin
                b2 = 0;
        end
end
else if(position == 1) begin
        b0 = 1;
```

```
        if(result==0) begin
                b1 = 0;
        end
end
else if(position == 0) begin
        // no bit to set
        if(result==0) begin
                b0 = 0;
        end
        #100 endOfConv = 1;
end
if(position >=0)
        position = position - 1;
end
```

```
        end

endmodule
```