Low Power High Speed Operational Amplifier Design Using Cadence

Submitted in partial fulfillment of the requirements

of the degree of

Bachelor of Engineering

in

Electronics and Telecommunication

by

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2019-2020

CERTIFICATE

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It is our great pleasure to present this report, a written testimonial of a fruitful experience. It would be unethical on my art to claim complete credit for the project. We therefore take this opportunity to express acknowledgement to all those individuals who helped in making our project a success. First and foremost, we would like to thank **Prof. Afzal Shaikh (HOD-Electronics & Telecommunication Department)** working with whom is a delightful and wholesome learning experience highly indebted to **Prof. Zarar Khan** for guidance and constant supervision as well as for providing necessary information regarding the project.

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Abstract

This paper presents a new approach to design 0f low power high speed operational Amplifier. The amplifying cell consist of two parts, differential amplifier and common source Amplifier. We are design a two stage CMOS operational amplifier which operate at 1.8Vpower supply and whose input is dependent on bias current. The supply voltage has been scaled down in order to reduced the overall power consumption of the system. The main aim of our work is to increase the slew rate of the op-amp without decreasing the gain of the amplifier. At large supply voltage, there is a trade-off among speed, power, GBW and gain but this op-amp has very low power consumption with a high driving capacity. The op-amp provide a gain pf 60dB and bandwidth of 30Mhz and 2pf load capacitor and output slew rate is 20V/μs.

Keywords:-Slew rate, GBW, PM, gain and bandwidth.

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1.INTRODUCTION

Operational amplifier is a voltage amplifier used to perform different mathematical operation. Op-amp is a monolithic semiconductor chip design with VLSI technology using epitorial method. The operational principle of operational amplifier is the conversion of differential voltage to a current at the output. Hence it is a voltage controlled current source (VCCS). In the single stage differential amplifier we are not able to get the high gain and bandwidth, So we are cascading the differential amplifier and common source amplifier to get the high gain There are two poles after cascading. P1=(1/r01c1), P2=(1/r02c2). So the minimum Phase Margin (PM) is 45º for stability thus to maintain this we have to shift the pole1 towards left. Now due to "Miller effect" the pole i.e. P1=(1/r1[c1+Cc(1+A)])

The mosfet1(M1) and the mosfet2(M2) are the identical and similarly the mosfet3(M3) and mosfet4(M4) are identical. We are going to find the (W/L) ratio of the each MOSFET which are help to increase the slew rate and gain value.

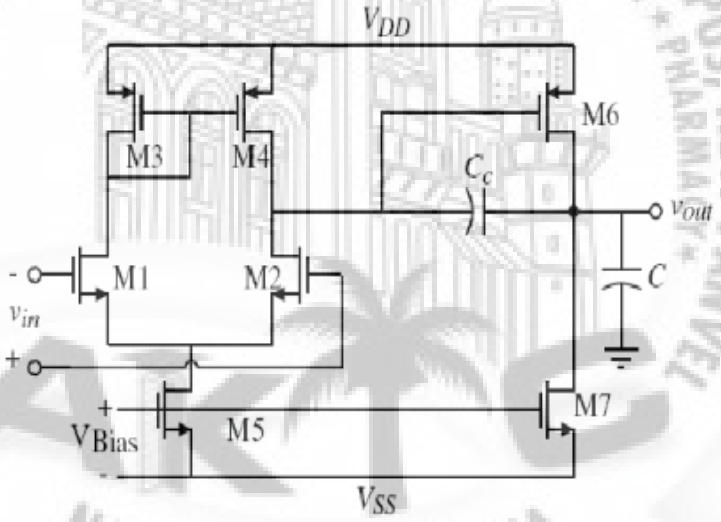

Fig1:-Two stage op-amp

In the above figure there are two type of amplifier are combine after drawing the small signal model of the op-amp we have to calculate the P1, P2, GBW, PM. To find this first of all find the transfer function (TF).

TF=gm1R1gm2(1-

SCc/gm2)/S^2[R1R2(C1C2+C1Cc+C2Cc)]+S[R2(Cc+C2)+R1(Cc+C1)+Ccgm2R1R2]+1

But we know that the general expression of the TF is given below

TF=K(1-S/Z)/(1+S/P1)(1+S/P2)

The first pole is given by

P1=(1/gm2R1R2Cc)

The second pole is given by

P2=gm2/C2

Zero(Z)=gm2/C2

Now to find the Dc gain

K=gm1R1gm2R2

GBW=gm1/Cc

A basic op-amp consists of 4 main blocks:

a. Current Mirror

b. Differential Amplifier

c. Level shift, differential to single ended gain stage

d. Output buffer

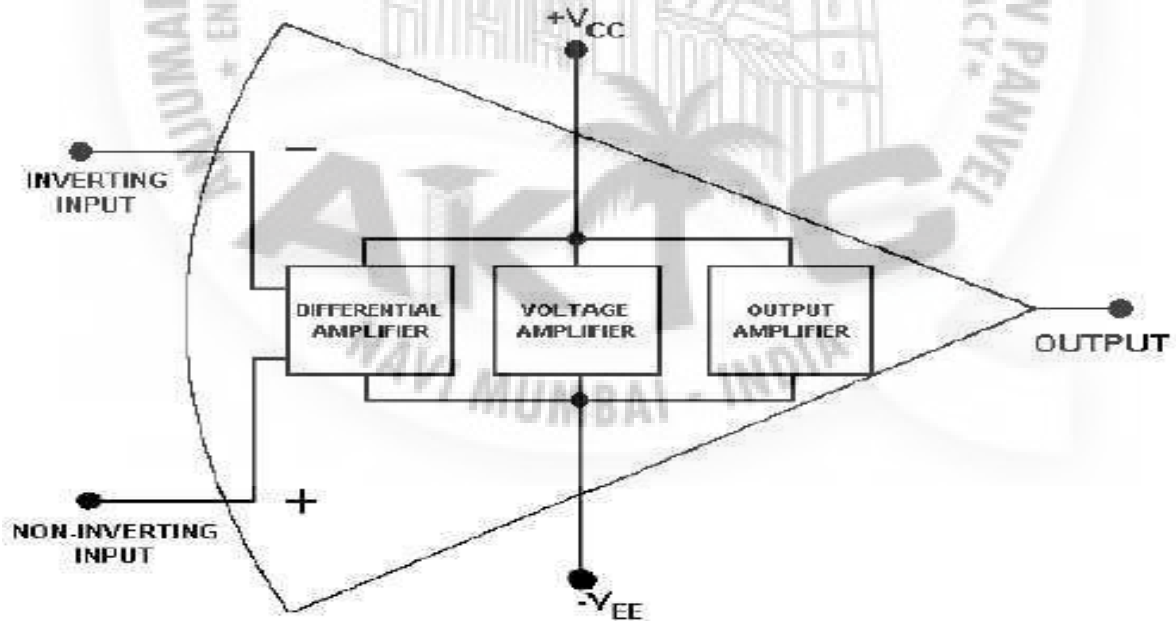

Figure 1 amplifier basic block diagram of operational amplifier

The Two Stage op-amp shown in fig 2 is widely used because of its structure and robustness. Our aim is to create the physical design and fabricate a low power Op-amp .An ideal op-amp having a single-ended out is characterized by a differential input, infinite voltage gain, infinite input resistance and zero output resistance. In a real op-amp however these characters cannot be generated but their performance has to be sufficiently good for the circuit behavior to closely approximate the characters of an ideal op-amp in most applications. With the introduction of each new generation of CMOS technologies design of op-amps continues to pose further challenges as the supply voltages and transistor channel lengths scale down

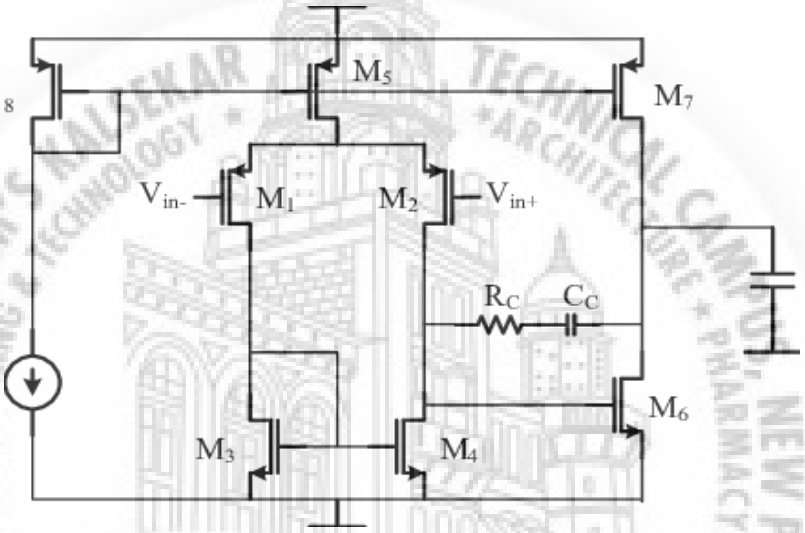

Figure 2 typical two stage operationale amplifire

1.2 MOTIVATION

The design of complex systems with analog, digital, and switched-capacitor building blocks integrated on one chip suffers from large signal variations on the power supply lines. Especially in those cases where low-level signals have to be measured, the use and development of high performance amplifiers are necessary. In analog building blocks, the main building blocks are operational transconductance amplifiers (OTA's). For this reason the performance of such amplifiers must be studied and analyzed as function of the power supply variations. The performance of a system influenced by power supply variations can be described by the power supply rejection ratio (PSRR)Performance of an op amp depends on numerous electrical characteristics, e.g., gain-bandwidth, slew rate common-mode range output swing offset etc. Two stage operational amplifiers (op amps) are often used to achieve both high dc gain and large output voltage swing.

1.3 Objective

To design a two stage cmos opamp with gain bandwidth product of 1MHZ, a view rate of V/μsec and CMRR of at least 60. It should operate at low voltage of the ±3V range

1.4 Scope

The project aims at coming up with a design of a two stage cmos opam such that mathematical calculations followed by a simulation using pspice lead us to check if we meet specifications.

Chapter 2

Literature Review

Paper Title: A) Low Power High Speed Operational Amplifier Design Using Cadence

2.1 Enhancement type MOSFET

The enhancement type MOSFET (Metal-Oxide-Semiconductor-field Effect transistor is a type of Field Effect Transistor (FET) where current is cut off until the input voltage between its input terminals reaches a specific magnitude. The input voltage is actually reverse biased with no direct contact between the input gate and the conducting channel, with only the charge accumulated controlling the current flow. This is due to insulation at its input. Current is conducted by only type of carrier – elections or holes. The fact that an input voltage can control its output current without direct contact makes Field Effect Transistors very popular. In fact the E-MOSFET (Enhancement type MOSFET) is the most widely used FET.

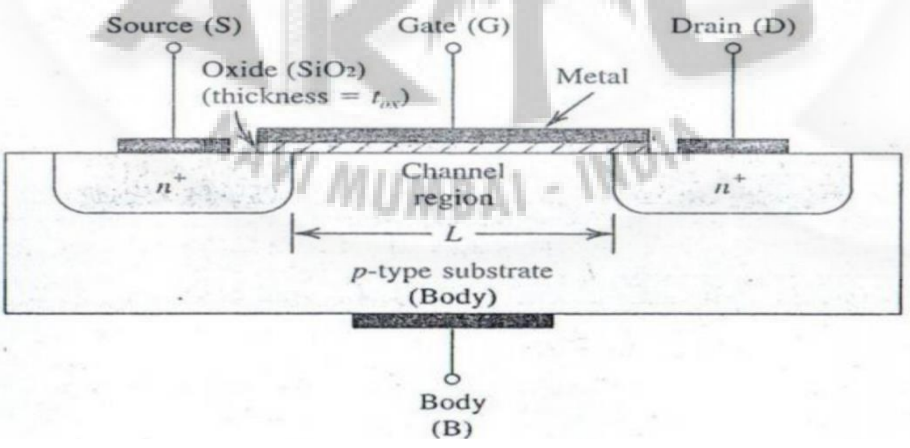

Figure 1 NMOS

The construction of the n-channel enhancement – type MOSFET is provided in figure 2.1/ a slab of p-type material is formed from a silicon base. This slab is at times called the substance or body.

The substrate at times can be connected to the source. The drain and source are two heavily doped regions created in the substrate. A thin layer of silicon dioxide – an insulator is grown on the body. Finally metal is deposited on the SiO2(silicon dioxide) layer to form the gate metallic platform from the region between the drain and source. Between the metallic contacts and the body is the p-type substrate.

2.3 Design of two stage operational amplifier

The designed op-amp has been simulated to find the different characteristics of the designed op-amp. The total design performed in Cadence tool. Different test benches have been created and extracted design has been then simulated with the parasitic values and compared with the schematic. Later in the chapter we also have compared the obtained parameters of the device through simulation to the specifications for the device.

2.3.1 Design Issues

Typical specs	Design factors
! DC Gain (Av)	Frequency Response
! Unity Gain Bandwidth.	Phase Margin
! Power Dissipation	Load Capacitance
! Slew Rate	Compensation
! Input Offset Voltage	Device Dimensions
! PSRR	
! Output Voltage Swing	
! ICMR	
! CMRR	

2.3.1 Steps in designing a CMOS opamp

1) Choosing or creating the basic structure of the op amp.
2) Decide on a suitable configuration determination of the type of compensation. needed for meeting the specification
3) Selection of the dc currents and transistor sizes.
4) Physical implementation of the design.
5) Fabrication
6) Measurement

The design process involves the two major steps, the first is the conception of design and second one is optimization of design. The conception of the design has been accomplished by proposing an architecture to meet the given specifications. This step is normally done by using hand calculations in order to maintain the

2.4 Common Mode Rejection Ratio (CMRR)

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common mode voltage will produce changes in output. The op amp common-mode rejection ratio (CMRR) is the ratio of the common-mode gain to differential-mode gain. For example, if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1 V, then the CMRR is X/Y. When the common-mode rejection ratio is expressed in dB, it is generally referred to as common-mode rejection (CMR)—please note that there is very little consistency in this throughout the semiconductor industry with regards to the use of dB or ratio values for CMR or CMRR.

Typical low frequency CMR values can be between 70 dB and 120 dB, but at higher frequencies, CMR deteriorates. In addition to a CMRR numeric specification, many op amp data sheets show a plot of CMR versus frequency, as shown in Figure 1 for the OP177 precision op amp.

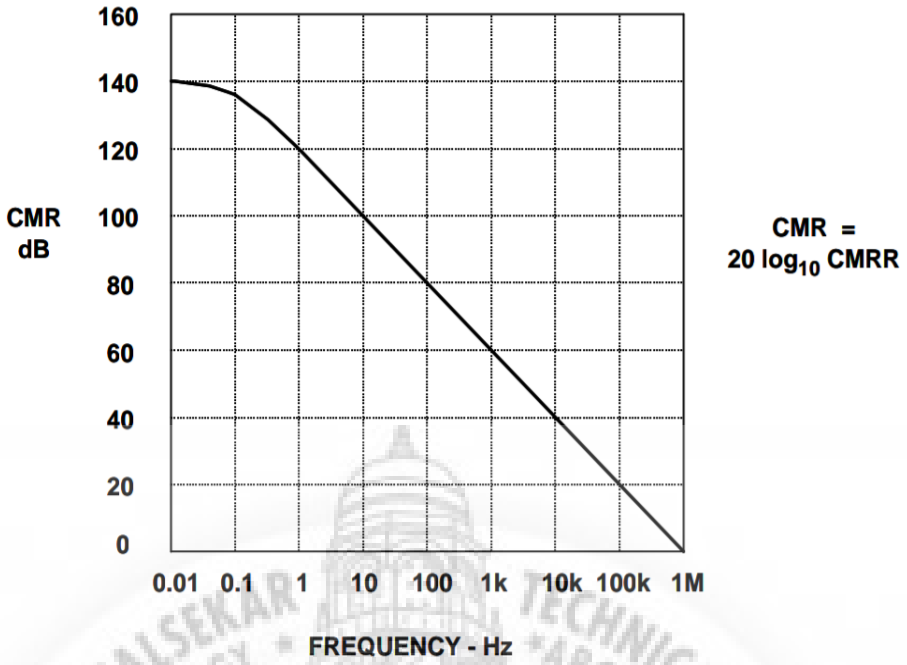

Figure 2: CMRR for the OP177

CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 2. Note inverting mode operating op amps will have less CMRR error. Since both inputs are held at a ground (or virtual ground), there is no CM dynamic voltage.

2.4.1 Measuring of common mode rejection ratio

Common-mode rejection ratio can be measured in several ways. The method shown in Figure 3 below uses four precision resistors to configure the op amp as a differential amplifier, a signal is applied to both inputs, and the change in output is measured—an amplifier with infinite CMRR would have no change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp. A mismatch of 0.1% between resistor pairs will result in a CMR of only 66 dB—no matter how good the op amp! Since most op amps have a low frequency CMR of between 80 dB and 120 dB, it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring the matching of the resistors!).

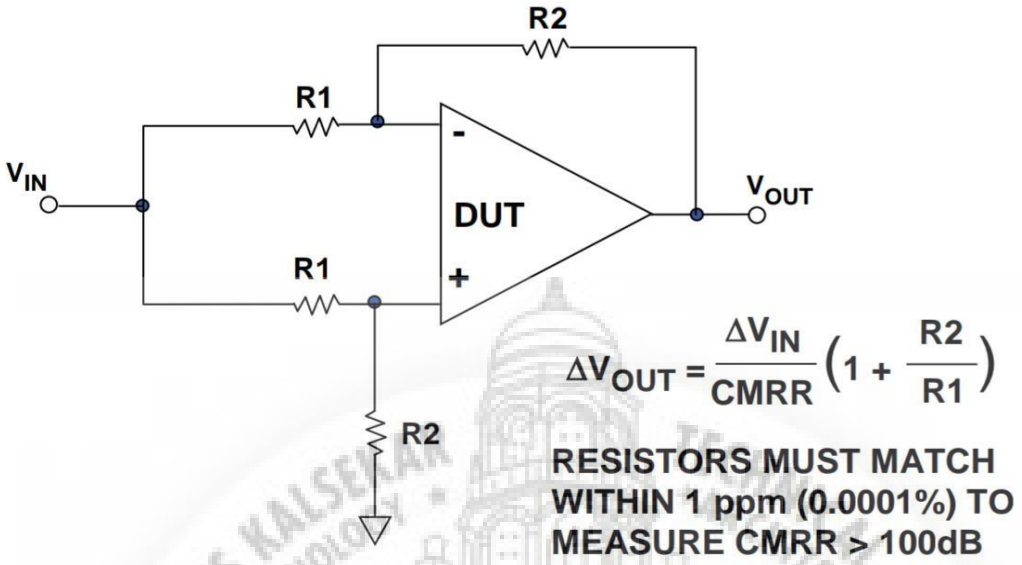

Figure 3. Simple CMRR Test ckt

2.5 Power supply rejection ratio

If the supply of an op amp changes, its output should not, but it typically does. If a change of X volts in the supply produces an output voltage change of Y volts, then the PSRR on that supply (referred to the output, RTO) is X/Y. The dimensionless ratio is generally called the power supply rejection ratio (PSRR), and Power Supply Rejection (PSR) if it is expressed in dB. However, PSRR and PSR are almost always used interchangeably, and there is little standardization within the semiconductor industry.

PSRR or PSR can be referred either to the output (RTO) or the input (RTI). The RTI value can be obtained by dividing the RTO value by the amplifier gain. In the case of the traditional op amp, this would be the noise gain. The data sheet should be read carefully, because PSR can be expressed either as an RTO or RTI value. PSR can be expressed as a positive or negative value in dB, depending on whether the PSRR is defined as the power supply change divided by the output voltage change, or vice-versa. There is no accepted standard for this in the industry, and both conventions are in use. If the

amplifier has dual supplies it is customary to express PSR separately for each. This is very useful for amplifiers that can be used in either dual or single-supply applications. It is extremely important to remember that PSR is very much a function of ripple or noise frequency as shown

in the plot for the OP1177 op amp. In most cases, the corner frequency of the roll-off follows that of the open-loop gain, and the slope is approximately 6 dB per octave (20 dB per decade). Typical PSR for the OP1177 is shown in Figure 4 below.

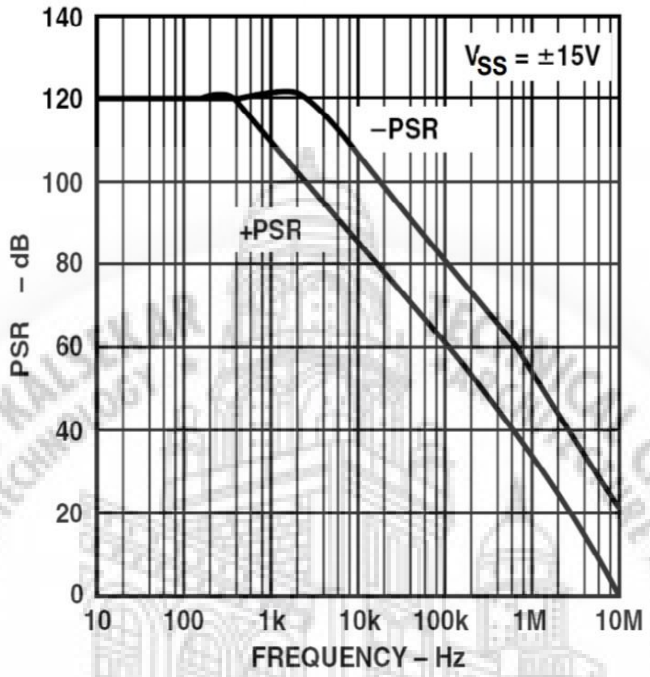

Figure 4 PSRR

A test setup used to measure PSRR is shown in Figure 5 below. Note that it is similar to the test setup used to measure CMRR

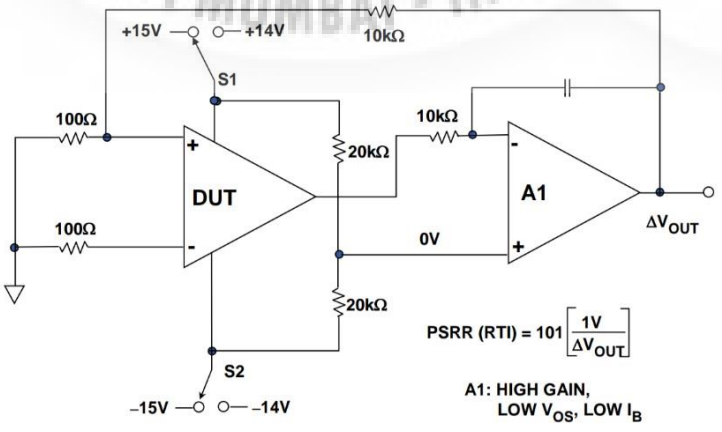

Fig.5 Test setup Measuring PSRR

2.6 slew Rate

The slew rate for the single stage differential amplifier is very less so that to increase that we are using the two stage differential amplifier. slew rate can be calculated by two cases as shown in the fig6 and fig7

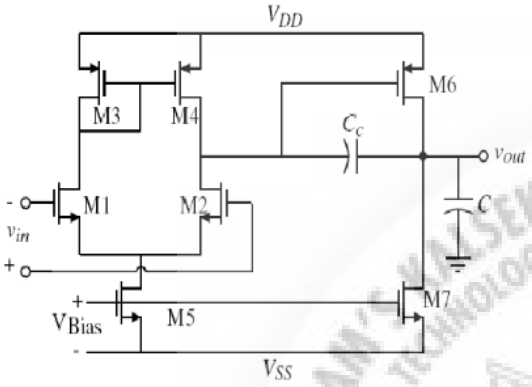

Fig no.6 Two stage op-amp

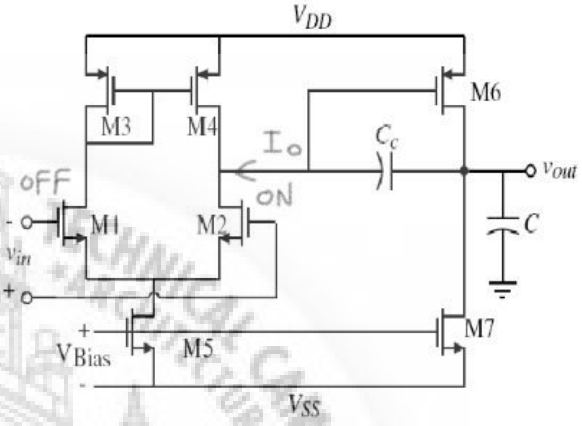

Fig no.7 When positive voltage is high

If we increase the voltage across the positive terminal of the mosfet2 then the mosfet 2 is ON and the mosfet1 is OFF therefore the current (Io) are not flowing through the mosfet3 and mosfet4, So the current flow through only coupling capacitor (Cc) as shown in the fig2. The current (Io) coming from the coupling capacitor is going through the mosfet5 (M5) and M5 and M6 are the identical mosfet so that the formula for the slew rate is given below SR=Io/Cc If we use the less value of the capacitor the slew rate is increase. there are many methods to increase the slew rate but we are using this method. If we increase the current(Io) ,we can increase the slew rate but the gain of the amplifier is reduced hence to increase the slew rate we have to decrease the coupling capacitor(Cc).We are going to find the value of the capacitor for which the slew rate is increase and gain will not decrease If we increase the voltage across the negative terminal of the mosfet1 then the mosfet 1 is ON and the mosfet2 is OFF therefore the current (Io) are flowing through the mosfet3 and mosfet4, So the Io/2 current flow through mosfet3, mosfet4 and coupling capacitor(Cc) as shown in the fig6.

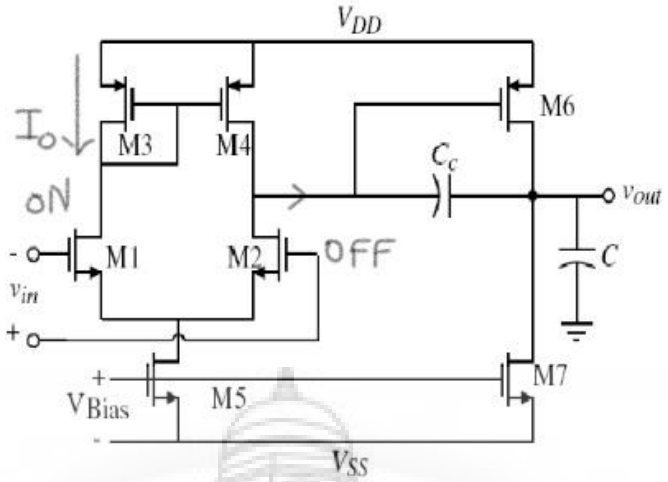

Fig8:-When negative voltage is high

The current (Io) going to the coupling capacitor through the mosfet5 (M4) and M5 and M6 are the identical mosfet so that the formula for the slew rate is given below

SR=Io/Cc

If we use the less value of the capacitor the slew rate is increase. there are many methods to increase the slew rate but we are using this method. If we increase the current(Io) ,we can increase the slew rate but the gain of the amplifier is reduced hence to increase the slew rate we have to decrease the coupling capacitor(Cc).We are going to find the value of the capacitor for which the slew rate is increase and gain will not decrease.

2.6.1 Slew Meaning and More About Calculating It

The slew rate is often used as a measure of how fast an amplifier is or how fast a digital logic circuit will switch from a low voltage state to a high voltage state. In an electronic circuit, such as a digital logic circuit, the time to switch from a low to high voltage state can be as low as a billionths of a second. Because of this, expect to find slew rate specifications that are in the range of a million volts per second to a billion volts per second For precise slew rate calculations, electronic designers don't use the very highest and very lowest voltage values. Instead they use a high voltage value that is 90 percent of the highest voltage and a low voltage that is 10 percent of the highest value. The time between the 10 percent and the 90 percent point is often called the rise time or fall time.

2.7 Phase Margin

The phase margin states the stability of the operational amplifier as above we know that the minimum phase margin should be 45º.To calculate the phase margin we have to draw the bode plot which is shown in the Fig9.

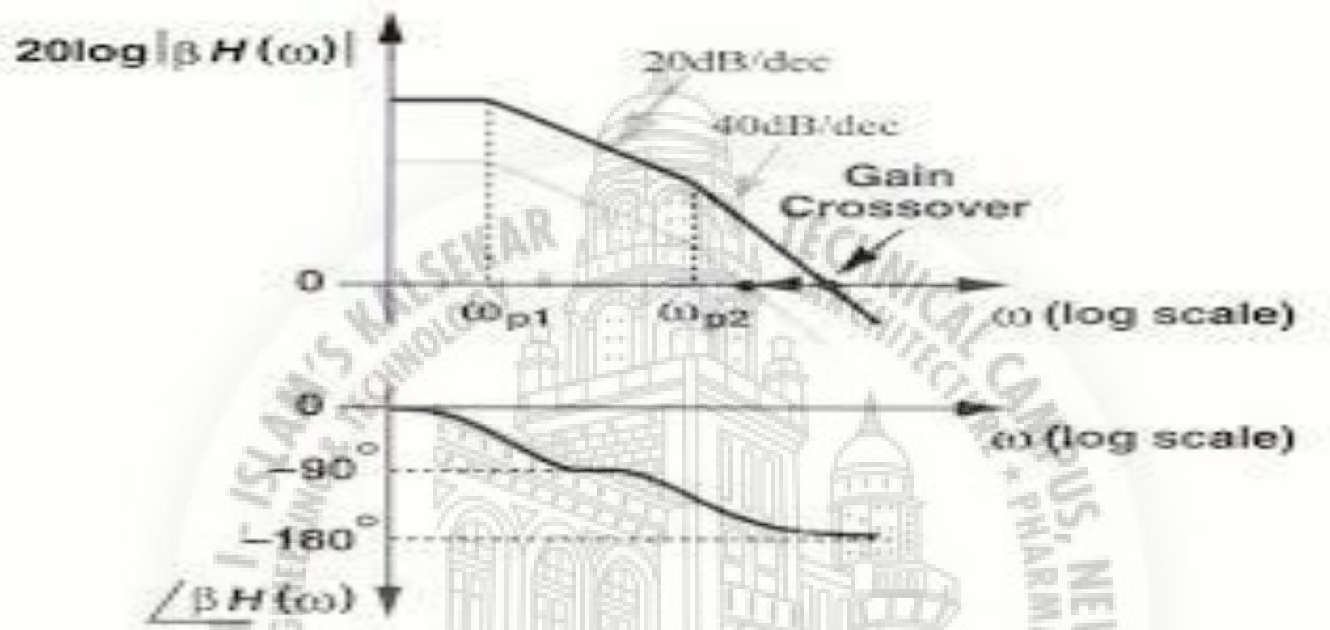

Fig9:-Bode plot

We can obtained the phase margin (PM) with the help of the bode plot. after simplifying the angle of the transfer function phase margin is given by

PM= 84.29-tan^-1(GBW/P2)

If we take the phase margin is 60º then

60=84.29-tan^-1(GBW/P2)

Tan^-1(GBW/P2)=24.29

P2=GBW/0.4513

P2=2.2*GBW

Therefore we can calculate the pole 2 and we get the relation between the GBW and P2 the P2 must be greater than and equal to the 2.2 of GBW. Similarly if the phase margin is 45º then the pole 2 is 1.22*GBW.

P2=2.2GBW

gm2/C2=2.2gm1/Cc ..... (1)

Assume the zero is ten times the GBW

Z=10GBW

gm2/Cc=10gm1/Cc

gm2=10gm1 ..... (2)

by using (1) and (2) we can calculate the value of the coupling capacitor as shown below

gm2/Cl=2.2gm1/Cc

10gm1/Cl>=2.2gm1/Cc

10/Cl>=2.2/Cc

Cc>=0.22Cl for the phase margin = 60º

To calculate the value of coupling capacitor we must know the value of the load capacitor and it is 0.22 times the load capacitor.

2.8 Limitation

The main limitations of this method come in picture during circuit design such as there is a limited common mode voltage range and some parameters like slew rate, input impedance, phase shift, etc. are not as per calculations.

Chapter 3

Technical Details

3.1 Design Examples And Simulation

To verify the above proposed approach, we decided to design a low power high speed operational amplifier. The amplifier is designed by or the process are used is 180nm.The following process parameters are used for preliminary calculations. The device gain is 1000(60dB), we consider the phase margin is 60º and ICMR(+) is 1.6V,ICMR(-) is 0.8V, The load capacitor value is 2pF the power used in the designing process must be less than or equal to 300µW. The gain bandwidth product is 30Mhz was taken as well. We used Vdd=1.8V.

The minimum channel length should be 180nm.It was decided to use the device length L=500nm for all mosfet .We can design the value of the mosfet1(M1) and mosfet2(M2) with the help of gain bandwidth product (GBW).For calculating the value of M3 and M4 we are using the maximum input common mode range (ICMR+),similarly for calculating the value of M5 and M7 we are using the minimum input common mode range. We can calculate the value of the coupling capacitor by using the phase margin of the system, the slew rate is depending on the value of I5. As we already know that Cc=0.22*Cl by using this we get Cc=800fF.Then we can calculate the slew rate as shown below

$$SR=I5/Cc$$

$$I5=Io=20\mu A$$

Now we calculate the gain of the first mosfet by using the formula ($gm1=GBW*Cc*2\pi$) and then we get gm1=160µA.So we can calculate the (W/L) ratio by using the drain current equation.

$$(W/L) = gm1\text{^}2/\mu nCoI5$$

We get the W/L ratio for the mosfet1 and mosfet2 is 5 so we get all the value. The operational amplifier was simulated using Cadence design system. The results of this simulation are shown in the Fig 1,2 and 3.

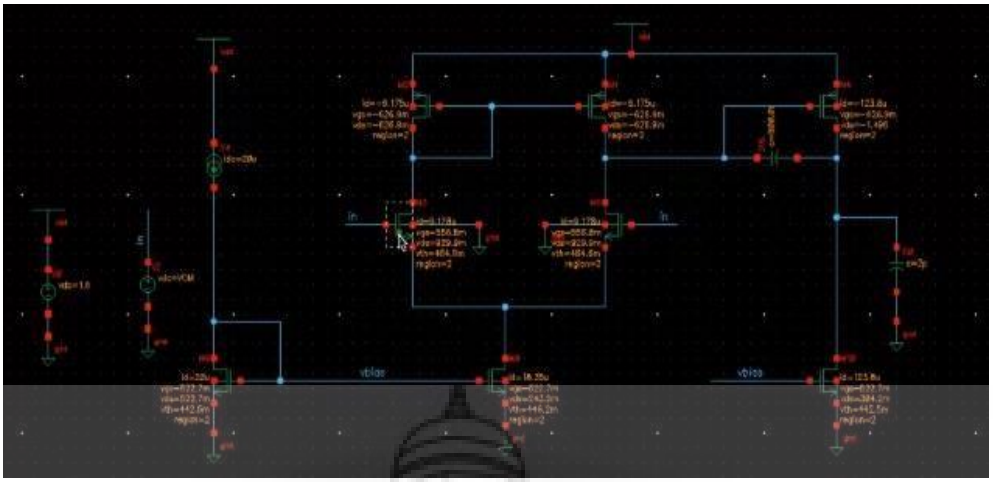

Fig1:-Circuit Diagram

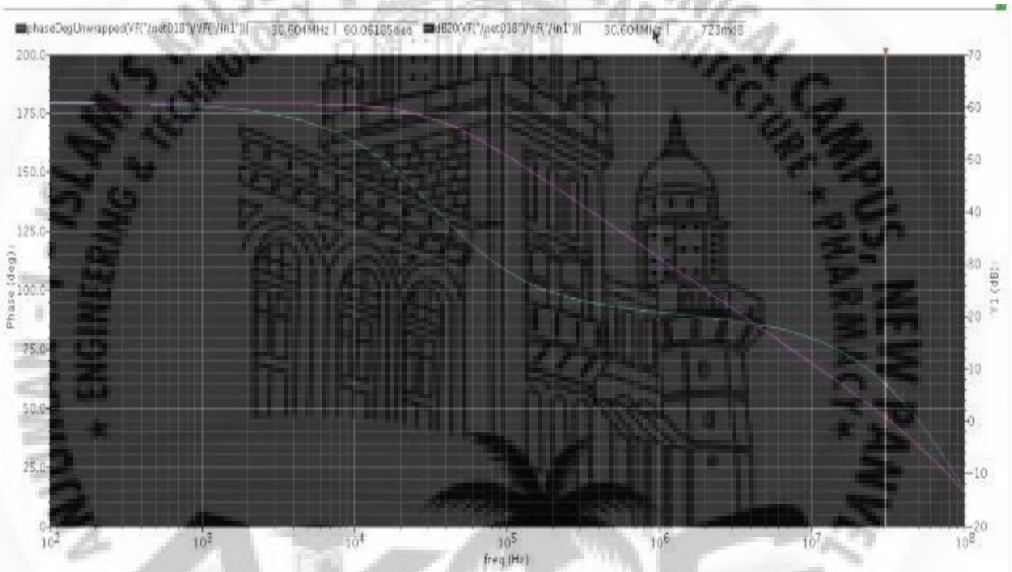

Fig2:- AC Gain and Phase plot for Vcd=0.8V

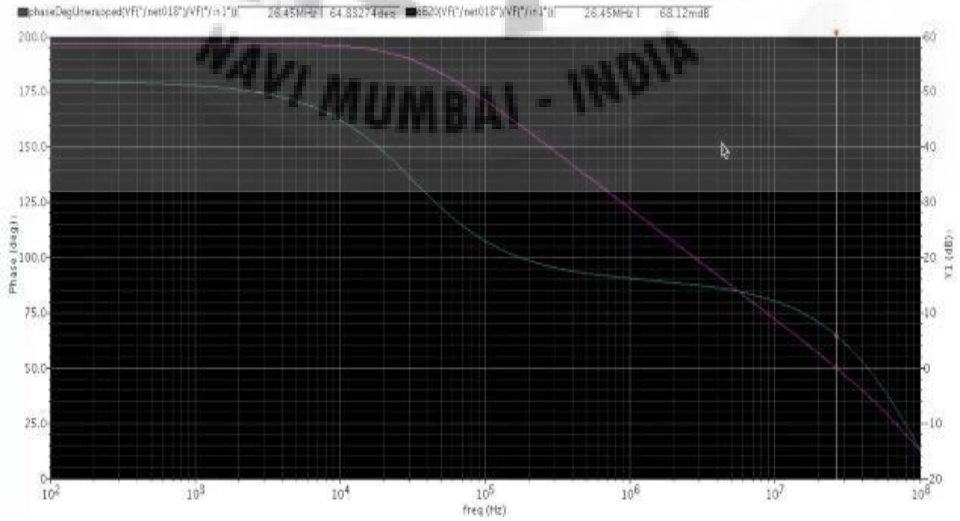

Fig3:- AC Gain and Phase plot for Vcd=1.6V

The simulation gives gain value,

phase margin and gain bandwidth product.it gives the gain of 60dB, GBW=30Mhz and phase margin is 60º.The phase characteristic of the op-amp is more complicated. As a result of these complications we are reducing the value of coupling capacitor and also reduced the gain of the mosfet

3.2 Methodology

1. In this project we are going to design two stage differential amplifier and improve its parameter by using cadence simulation software.

2. we learn all the four stages of cadence for designing of schematic diagram, Symbol designing, layout designing and post layout simulation.

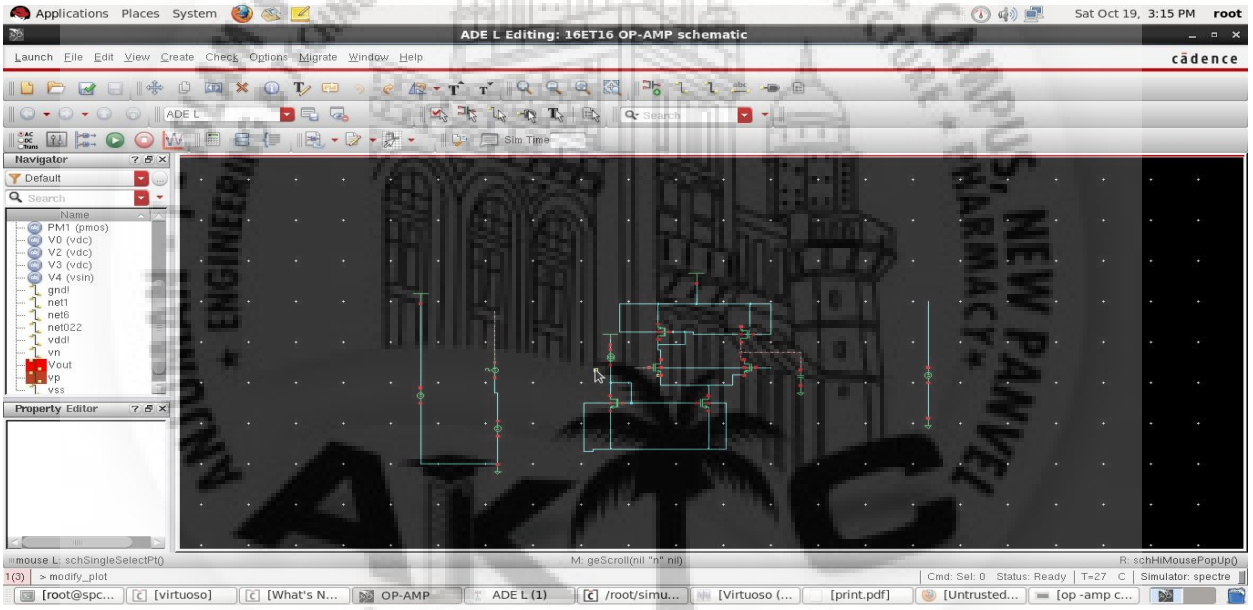

Figure 4 schematic diagram two stage opamp

3. To achieve this, we first do the theoretical design of operational amplifier that how we can improve the parameters of op amp

4.Through theoretical design we get the W/L ration of MOSFETs coupling capacitor and drain current across the MOSFET.

Which are as follows:-

I5=20u

Cc=800*10^-15 farad

M1 M2=6 ===> 0.35/500n

M3 M4=14 ====> 7/0.5

M5 M6=12====> 6/0.5

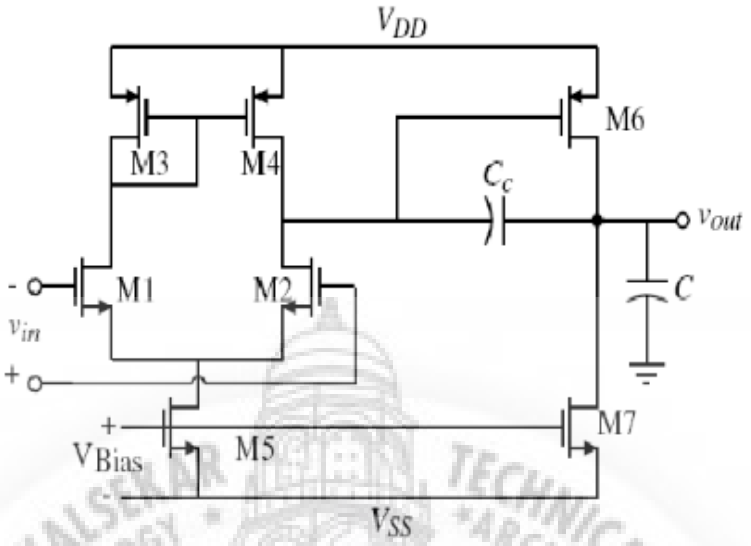

Figure 5 two stage opamp

5.Using cadence simulation software we are implement our theoretical design.

6.After simulation on cadence we design its layout and fabricate it to make IC.3.2 Project Requirements

3.2.1 Software Requirements

- Cadence
- Red hat operating system for security purpose

3.2.1.1 Hardware Requirements

- Quad core Intel Core i5 Skylake or higher (Dual core is not the best for this kind of work, but manageable)
- 8GB of RAM (8GB is okay but not for the performance you may want and or expect)

- M.2 PCIe or regular PCIe SSD with at least 256GB of storage, though 512GB is best for performance. The faster you can load and save your applications, the better the system will perform. (SATA III will get in the way of the system's performance)

3.3 Project Architecture

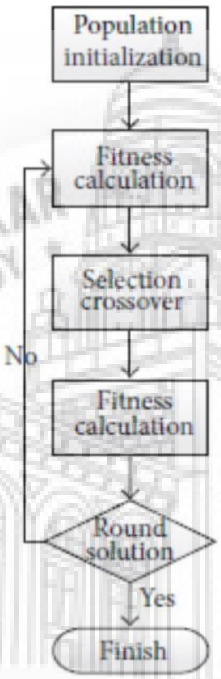

Figure 3 general algorithm Flow chart

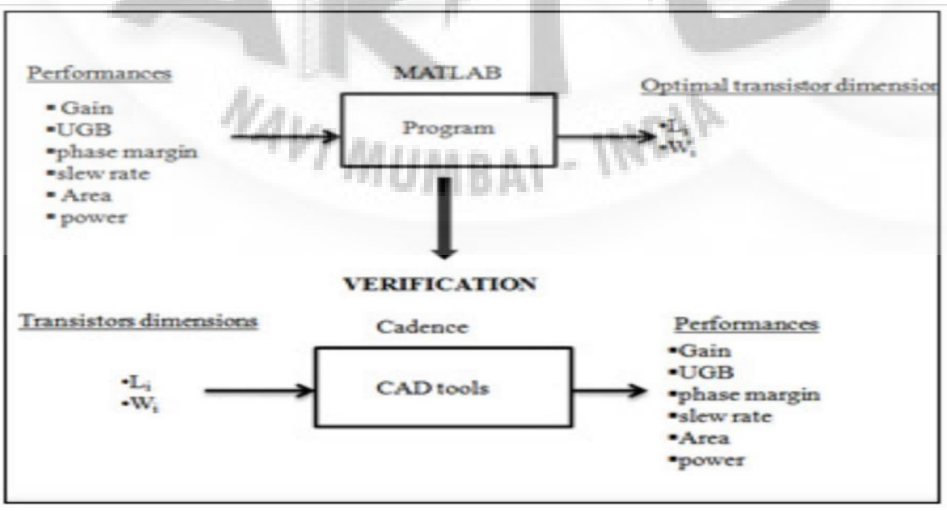

Figure opamp design flow

Chapter 4

Market Potential

4.1 Market Potential of Project

Estimated to reach two million USD in 2019 and projected to grow at the CAGR of % during the 2020-2025. The report analyses the global Operational Amplifier (op amp) market, the market size and growth, as well as the major market participants. The analysis includes Operational Amplifier (op amp) market size, upstream situation, market segmentation, market segmentation, price & cost and industry environment. In addition, the report outlines the factors driving industry growth and the description of market channels. The report begins from overview of industrial chain structure, and describes the upstream. Besides, the report analyses market size and forecast in different geographies, type and end-use segment, in addition, the report introduces market competition overview among the major companies and company's profiles, besides, Operational Amplifier (op amp) market price and channel features are covered in the report. Competitive Advantages of Project

4.2 Competitive Advantages of Project

Because of high speed and low power consumption its very useful that the transistor A transistor is a single electronic element. An operational amplifier is the equivalent of many transistors and is thus able to perform much better than a single transistor (e.g. higher input impedance, lower output impedance, higher gain, differential inputs and/**or** differential outputs, etc.)

Chapter 5

Conclusion and Future Scope

5.1 Conclusion

The operational amplifier circuit was introduced. Its cascaded with differential amplifier and common source amplifier circuits was established. It was shown how to increase the gain, phase margin and gain bandwidth product. It was demonstrated that these stages can be directly cascaded. The amplifier required to maintained the phase margin and gain bandwidth product. The most effective way to do it is the variation of the value of the coupling capacitor (Cc) and there are many more methods. The circuit requires, for gain stabilization caused by reducing the Vcd. The amplifier with less value of Cc and W/L ratio shows the gain-bandwidth and phase margin (PM)The Fig.5 has well defined gain, Slew rate and phase margin.

5.2 Future Scope

Due to the nature of the wide research topic, there are still several areas of improvement for future work in this op amp. Parameters such as the power-supply rejection ratio, mismatched offset and noise can be improved by increasing the device area while maintaining the W/L ratio constant.

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