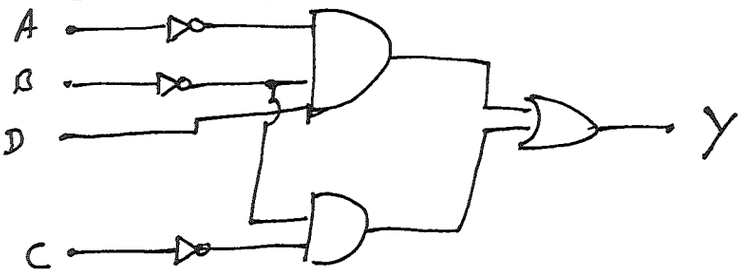
Con. 6637–13. **GS–7311**

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** out of remaining **six** questions.
(3) **Figures** to the **right** indicate **full** marks.

1. (a) Perform the following :— **5**
   (i) $(AF\ 19)_{16}$ to Binary and Octal
   (ii) $(1010)_2$ to Gray code.
   (b) Write the equation for output Y. Minimize the equation using Boolean identity. **5**



   (c) State and prove De-Morgan's theorem. **5**
   (d) What is the function of preset and clear input in flip-flop ? **5**

2. (a) Prove the following expression :— **10**
   (i) $(B+A)(B+D)(A+C)(C+D) = BC+AD$
   (ii) $A(B+C) + \overline{\overline{AB} + \overline{BC}} + \overline{A}(B+C) = B(AC+1) + C$.
   (b) Implement BCD to seven segment code converter. **10**

3. (a) Simplify the following :— **10**
   $f(A, B, C, D) = \sum m\ (0, 1, 5, 9, 13, 14, 15 + d\ (3, 4, 7, 10, 11)$
   (b) Convert :— **10**
   (i) SR to JK f/f
   (ii) SR to D f/f.

4. (a) Minimize the following expression using Quine Mc Cluskey tabular method :— **10**
   $f(A, B, C, D) = \sum m\ (1, 3, 7, 9, 10, 11, 13, 15)$
   (b) Design a twisted ring counter, using J-K. flip flop. Calculate propagation delay at last stage, if propagation delay of each F/F is 4 μsec. **10**

5. (a) Draw 8:1 multiplexer using logic gates along with its truth table. **10**
   (b) Design a 4 bit binary up-down counter using J-K flip flops. **10**

6. (a) Explain serial-in serial-out shift register using SR flip-flop. Draw the timing diagram with respect to negative edge triggered clock pulse. **10**
   (b) Explain – **10**
   (i) ECL logic family
   (ii) NOR gate using TTL logic.

7. Write short notes on (any **three**) :— **20**
   (a) IC-555 timer [Monostable state]
   (b) IC-0808
   (c) Dynamic RAM cell
   (d) Hazards in combinational circuits
   (e) Voltage regulation using IC 723.