Con. 6488-13. **GS-7017**

(3 Hours) **[Total Marks : 100**

N. B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume any **suitable** data wherever **required** but justify the **same**.
(4) **Figures** to the **right** indicate **full** marks.

1. (a) Explain capture range, lock range and pull in time with reference to PLL. **5**
(b) Explain log amplifier. **5**
(c) List ideal characteristics of op-amp. **5**
(d) Explain the working of Schmitt trigger. **5**

2. (a) Explain with neat diagram the working of IC 555 as monostable multivibrator state and explain any two applications. **10**
(b) (i) Draw and explain block diagram of CPLD. **6**
(ii) Give features of XC 9500 family. **4**

3. (a) Design a Second order KRC band reject filter with f_0 = 50 Hz and bandwidth = 6 Hz. **10**
(b) Explain in detail any two applications of Instrumentation amplifier. **10**

4. (a) Write VHDL Code for 4-bit down counter. **10**
(b) (i) Explain various documentation standards of sequential circuits. **6**
(ii) Explain switch de-bouncing. **4**

5. (a) Explain with output derivation the working of inverting and non-inverting adder circuit. **10**
(b) Draw and explain the functional block diagram of IC XR–2206. **10**

6. (a) Draw the block diagram of IC 565 PLL. Explain in detail FSK demodulation using PLL. **10**
(b) Design a sequence detector to detect a serial input sequence of 1010. Use JK Flip-flops. **10**

7. Write short notes on :— **20**
(a) Dual slope A/D Converter
(b) LM 380 audio amplifier
(c) General architecture of FPGA
(d) V to I converter using grounded load.